

N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

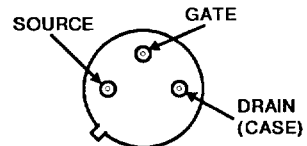
- 8.0A, 100V
- $r_{DS(on)} = 0.18\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Description

The 2N6796 is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

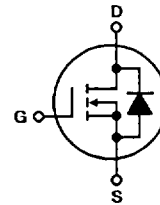
The 2N6796 is supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

Package

 TO-205AF
BOTTOM VIEW


Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^\circ\text{C}$) Unless Otherwise Specified

	2N6796	UNITS
Drain-Source Voltage (Note 1)	V_{DS} 100*	V
Drain-Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	V_{DGR} 100*	V
Continuous Drain Current		
$T_C = +25^\circ\text{C}$	I_D 8.0*	A
$T_C = +100^\circ\text{C}$	I_D 5.0*	A
Pulsed Drain Current (Note 2)	I_{DM} 32*	A
Gate-Source Voltage	V_{GS} $\pm 20^*$	V
Continuous Source Current (Body Diode)	I_S 8.0*	A
Pulse Source Current (Body Diode) (Note 2)	I_{SM} 32*	A
Maximum Power Dissipation		
$T_C = +25^\circ\text{C}$ (See Figure 14)	P_D 25*	W
Linear Derating Factor (See Figure 14)	0.20*	W/ $^\circ\text{C}$
Inductive Current, Clamped	I_{LM} 32	A
(L = 100 μH)		
Operating and Storage Junction Temperature Range	T_J, T_{STG} -55 to +150*	$^\circ\text{C}$
Maximum Lead Temperature for Soldering	T_L 300*	$^\circ\text{C}$
(0.063" (1.6mm) from case for 10s)		

*JEDEC registered values

NOTES:

1. $T_J = +25^\circ\text{C}$ to +150 $^\circ\text{C}$
2. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Specifications 2N6796

Electrical Characteristics @ $T_C = 25^\circ\text{C}$ (Unless Otherwise Specified)

Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS} Drain - Source Breakdown Voltage	100*	—	—	V	$V_{GS} = 0V, I_D = 0.25\text{ mA}$
$V_{GS(th)}$ Gate Threshold Voltage	2.0*	—	4.0*	V	$V_{DS} = V_{GS}, I_D = 0.5\text{ mA}$
I_{GSS} Gate - Source Leakage Forward	—	—	100*	nA	$V_{GS} = 20V, V_{DS} = 0V$
I_{GSS} Gate - Source Leakage Reverse	—	—	100*	nA	$V_{GS} = -20V, V_{DS} = 0V$
I_{DSS} Zero Gate Voltage Drain Current	—	—	250*	μA	$V_{DS} = 100V, V_{GS} = 0V$
			1000*	μA	$V_{DS} = 80V, V_{GS} = 0V, T_C = 125^\circ\text{C}$
$V_{DS(on)}$ On-State Voltage (2)	—	—	1.56*	V	$V_{GS} = 10V, I_D = 8.0A$
$R_{DS(on)}$ Static Drain-Source On-State Resistance (2)	—	0.14	0.18*	Ω	$V_{GS} = 10V, I_D = 5.0A, T_C = 25^\circ\text{C}$
			0.35*	Ω	$V_{GS} = 10V, I_D = 5.0A, T_C = 125^\circ\text{C}$
V_{SD} Diode Forward Voltage (2)	0.75*	—	1.5*	V	$T_C = 25^\circ\text{C}, I_S = 8.0A, V_{GS} = 0V$
g_{fs} Forward Transconductance (2)	3.0*	5.5	9.0*	S(1)	$V_{DS} = 5V, I_D = 5.0A$
C_{iss} Input Capacitance	350*	600	900*	pF	$V_{GS} = 0V, V_{DS} = 25V, f = 1.0\text{ MHz}$
C_{oss} Output Capacitance	150*	300	500*	pF	See Fig. 10
C_{rss} Reverse Transfer Capacitance	50*	100	150*	pF	
$t_{d(on)}$ Turn-On Delay Time	—	—	30*	ns	$V_{DD} = 30V, I_D = 5.0A, Z_\theta = 50^\circ$
t_r Rise Time	—	—	75*	ns	See Fig. 15
$t_{d(off)}$ Turn-Off Delay Time	—	—	40*	ns	(MOSFET switching times are essentially independent of operating temperature.)
t_f Fall Time	—	—	45*	ns	
SOA Safe Operating Area	25	—	—	W	$V_{DS} = 80V, I_D = 310\text{ mA}$, See Fig. 16.
	25	—	—	W	$V_{DS} = 3.12V, I_D = 8.0A$, See Fig. 16.

Thermal Resistance

$R_{\theta JC}$ Junction-to-Case	—	—	5.0*	$^\circ\text{C/W}$	
$R_{\theta JA}$ Junction-to-Ambient	—	—	175	$^\circ\text{C/W}$	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr} Reverse Recovery Time	300	ns	$T_J = 150^\circ\text{C}, I_F = 8.0A, di_F/dt = 100A/\mu\text{s}$
Q_{RR} Reverse Recovered Charge	1.5	μC	$T_J = 150^\circ\text{C}, I_F = 8.0A, di_F/dt = 100A/\mu\text{s}$
t_{on} Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.		

① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

*JEDEC registered value

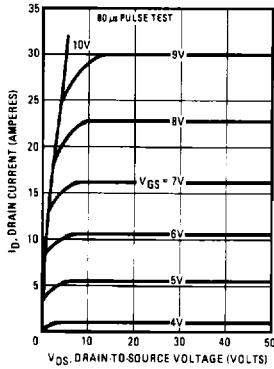


Fig. 1 - Typical Output Characteristics

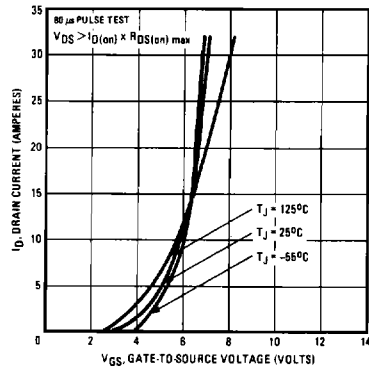


Fig. 2 - Typical Transfer Characteristics

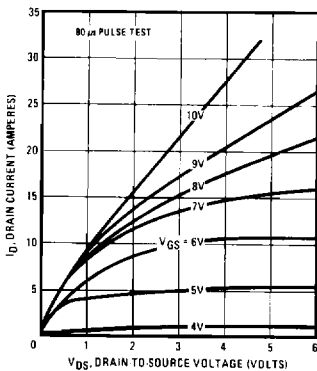


Fig. 3 - Typical Saturation Characteristics

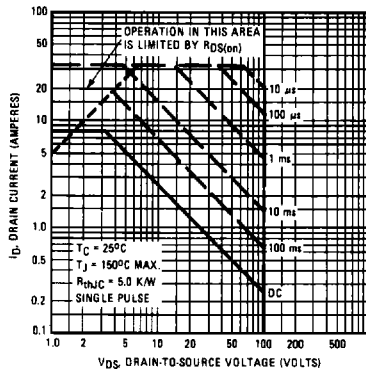


Fig. 4 - Maximum Safe Operating Area

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POWER MOSFET'S

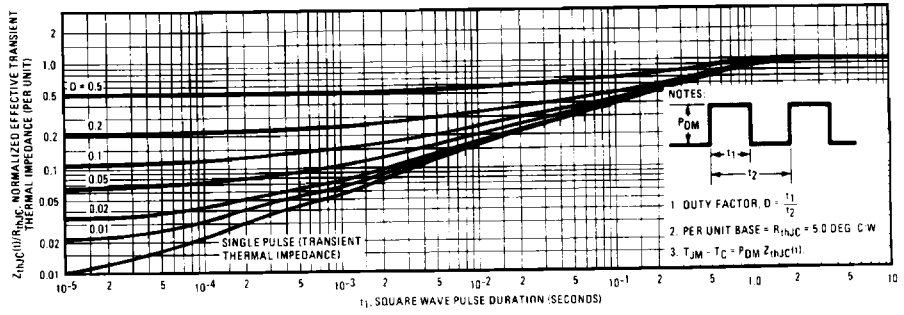


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

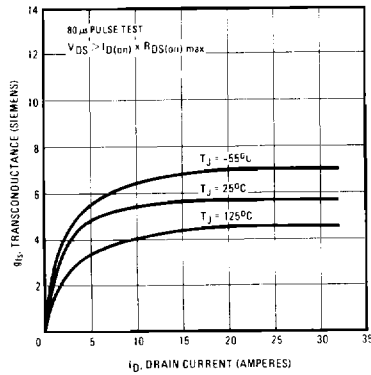


Fig. 6 – Typical Transconductance Vs. Drain Current

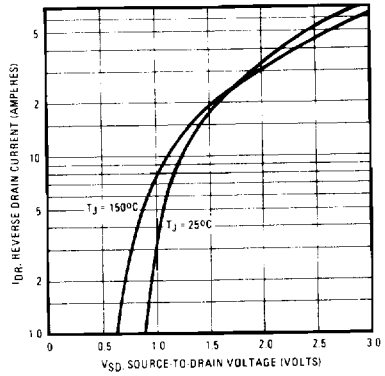


Fig. 7 – Typical Source-Drain Diode Forward Voltage

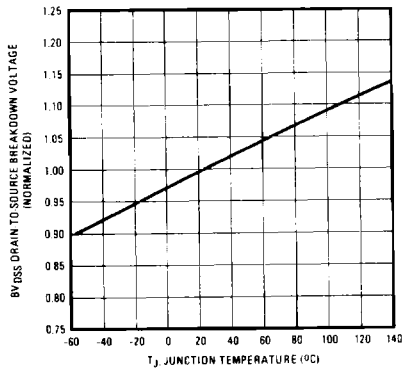


Fig. 8 – Breakdown Voltage Vs. Temperature

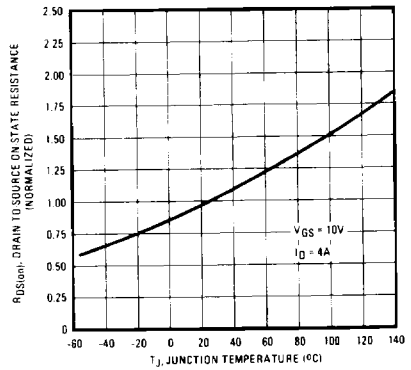


Fig. 9 – Normalized On-Resistance Vs. Temperature

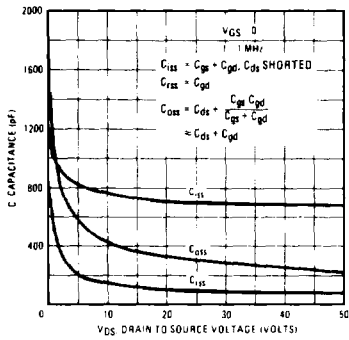


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

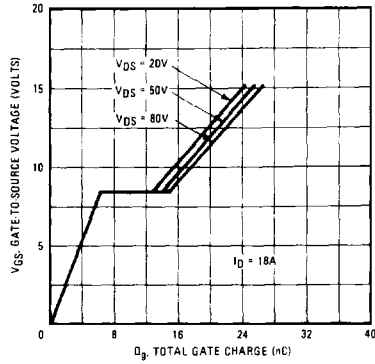


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

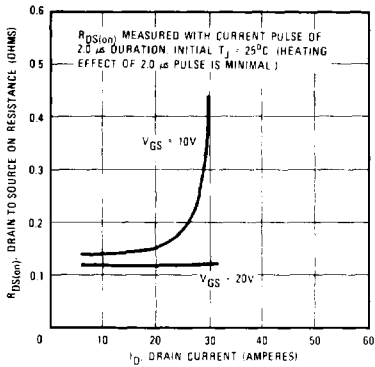


Fig. 12 - Typical On-Resistance Vs. Drain Current

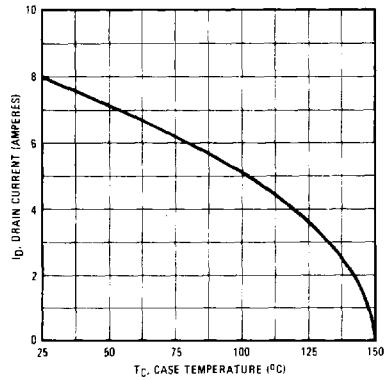


Fig. 13 - Maximum Drain Current Vs. Case Temperature

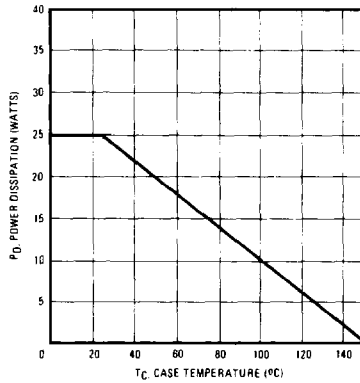
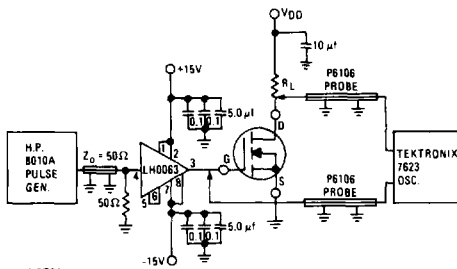
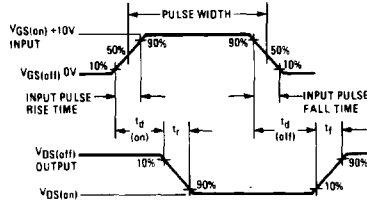


Fig. 14 - Power Vs. Temperature Derating Curve

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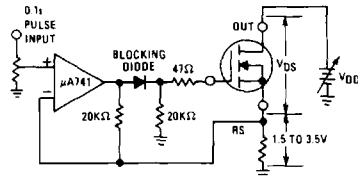


- NOTES:
1. LHM063 CASE GROUNDED.
 2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD.
 3. PULSE WIDTH = 3 μs, PERIOD = 1 ms, AMPLITUDE = 10V.



- NOTES:
- WHEN MEASURING RISE TIME, $V_{GS(on)}$ SHALL BE AS SPECIFIED ON THE INPUT WAVEFORM. WHEN MEASURING FALL TIME, $V_{GS(off)}$ SHALL BE SPECIFIED ON THE INPUT WAVEFORM. THE INPUT TRANSITION AND DRAIN VOLTAGE RESPONSE DETECTOR SHALL HAVE RISE AND FALL RESPONSE TIMES SUCH THAT DOUBLING THESE RESPONSES WILL NOT AFFECT THE RESULTS GREATER THAN THE PRECISION OF MEASUREMENT. THE CURRENT SHALL BE SUFFICIENTLY SMALL SO THAT DOUBLING IT DOES NOT AFFECT TESTS RESULTS GREATER THAN THE PRECISION OF MEASUREMENT.

Fig. 15 - Switching Time Test Circuit



- NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1μs PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
 2. SELECT R_S SUCH THAT $I_D = R_S - 2.5 + 1.0 V_{GS}$.

Fig. 16 - Safe Operating Area Test Circuit