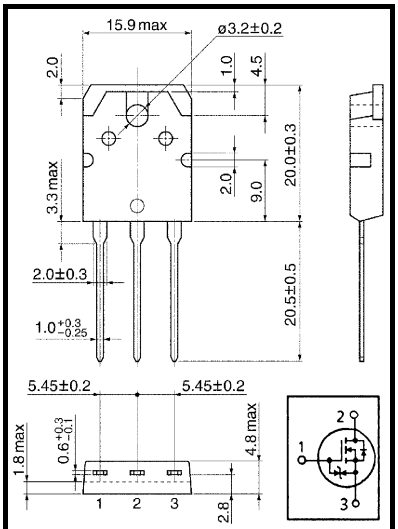
TOSHIBA Field Effect Transistor Silicon N-Channel MOS Type (MACH II π-MOS VI)

2SK3936

Switching Regulator Applications

- Small gate charge: Qg = 60 nC (typ.)
- Fast reverse recovery time: t_{rr} = 380 ns (typ.)
- Low drain-source ON-resistance: $R_{DS\ (ON)}$ = 0.2 Ω (typ.)
- High forward transfer admittance: $|Y_{fs}|$ = 16.5 S (typ.)
- Low leakage current: I_{DSS} = 500 μA (V_{DS} = 500 V)
- Enhancement mode: V_{th} = 2.0~4.0 V (V_{DS} = 10 V, I_D = 1 mA)

Unit: mm



JEDEC	—
JEITA	SC-65
TOSHIBA	2-16C1B

Weight: 4.6 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	500	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	500	V
Gate-source voltage		V_{GSS}	±30	V
Drain current	DC (Note 1)	I_D	23	A
	Pulse (Note 1)	I_{DP}	92	
Drain power dissipation (Tc = 25°C)		P_D	150	W
Single-pulse avalanche energy (Note 2)		E_{AS}	759	mJ
Avalanche current		I_{AR}	23	A
Repetitive avalanche energy (Note 3)		E_{AR}	15	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	-55~150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Characteristics

Characteristic	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th\ (ch\text{-}c)}$	0.833	°C/W
Thermal resistance, channel to ambient	$R_{th\ (ch\text{-}a)}$	50	°C/W

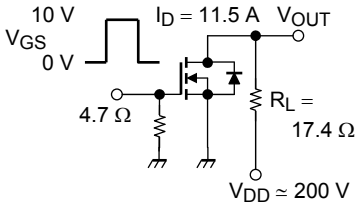
Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: V_{DD} = 90 V, T_{ch} = 25°C(initial), L = 2.44 mH, I_{AR} = 23 A, R_G = 25 Ω

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

This transistor is an electrostatic-sensitive device. Handle with care.

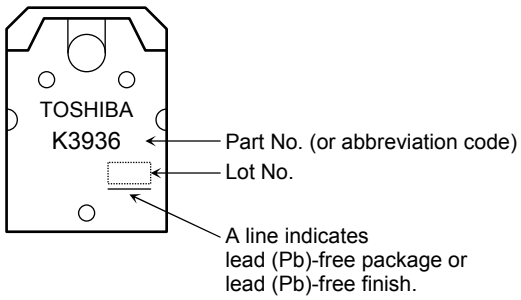
Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±25 V, V_{DS} = 0 V	—	—	±10	μA
Gate-source breakdown voltage		$V_{(BR)\ GSS}$	I_D = ±10 μA, V_{GS} = 0 V	±30	—	—	V
Drain cutoff current		I_{DSS}	V_{DS} = 500 V, V_{GS} = 0 V	—	—	500	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	500	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	2.0	—	4.0	V
Drain-source ON-resistance		$R_{DS\ (ON)}$	V_{GS} = 10 V, I_D = 11.5 A	—	0.2	0.25	Ω
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 11.5 A	8	16.5	—	S
Input capacitance		C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	—	4250	—	pF
Reverse transfer capacitance		C_{rss}		—	10	—	
Output capacitance		C_{oss}		—	420	—	
Switching time	Rise time	t_r		—	12	—	ns
	Turn-on time	t_{on}		—	45	—	
	Fall time	t_f		—	10	—	
	Turn-off time	t_{off}	Duty ≦ 1%, t_w = 10 μs	—	80	—	
Total gate charge		Q_g	V_{DD} ≃ 400 V, V_{GS} = 10 V, I_D = 23 A	—	60	—	nC
Gate-source charge		Q_{gs}		—	50	—	
Gate-drain charge		Q_{gd}		—	10	—	

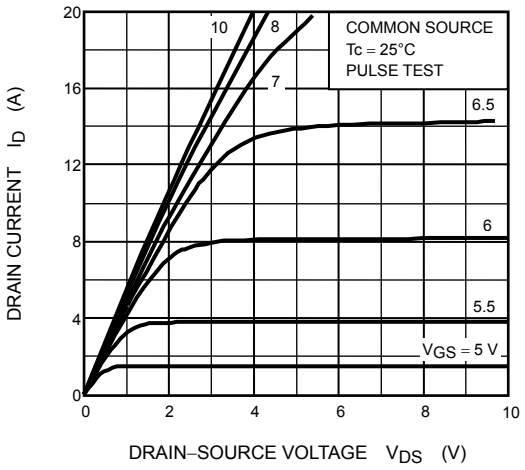
Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	23	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	92	A
Forward voltage (diode)	V_{DSF}	I_{DR} = 23 A, V_{GS} = 0 V	—	—	-1.7	V
Reverse recovery time	t_{rr}	I_{DR} = 23 A, V_{GS} = 0 V, dI_{DR}/dt = 100 A/μs	—	380	—	ns
Reverse recovery charge	Q_{rr}		—	2.4	—	μC

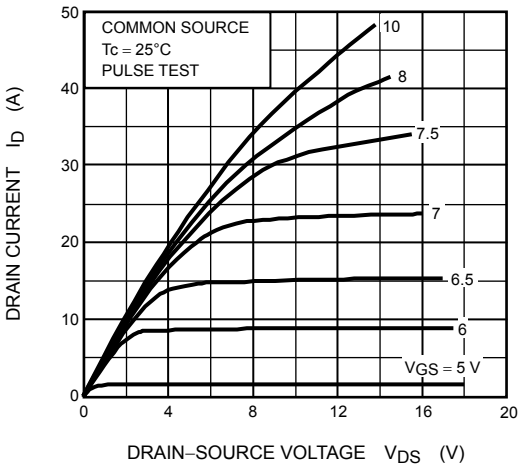
Marking



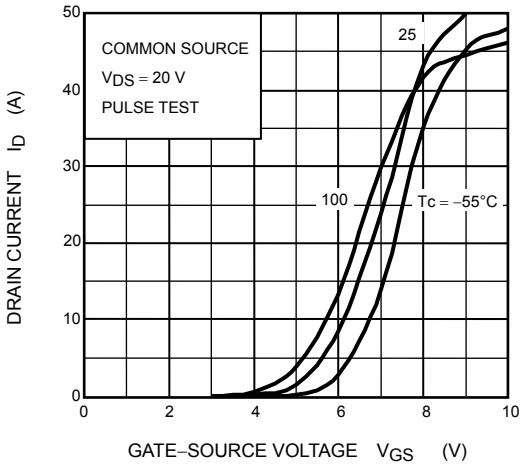
$I_D - V_{DS}$



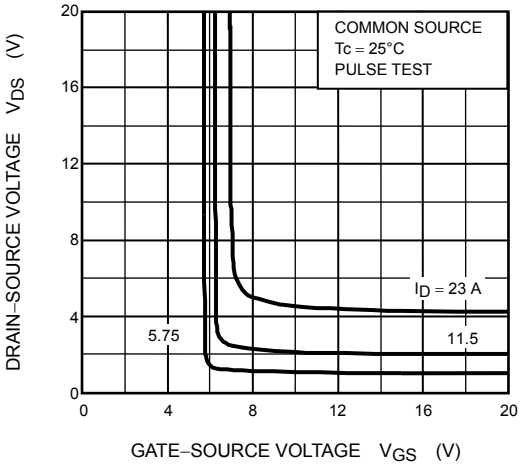
$I_D - V_{DS}$



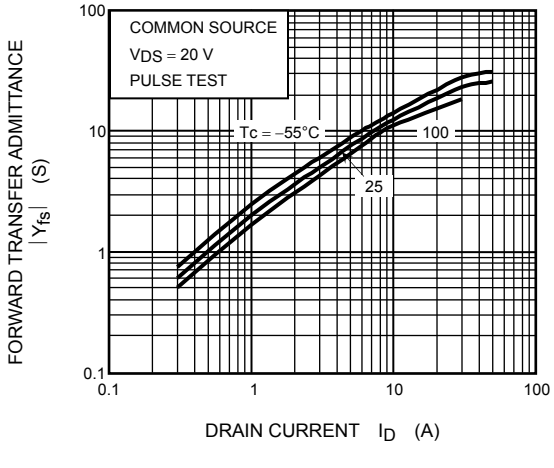
$I_D - V_{GS}$



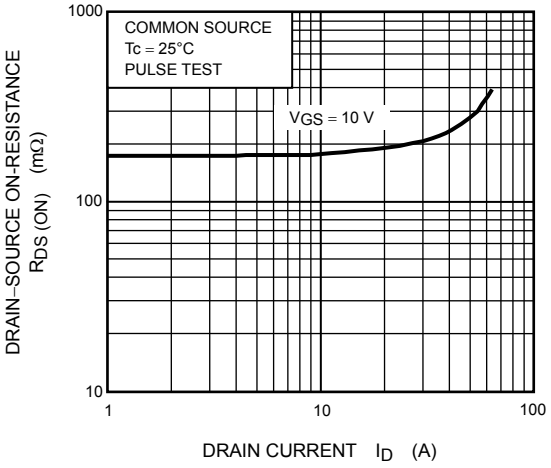
$V_{DS} - V_{GS}$



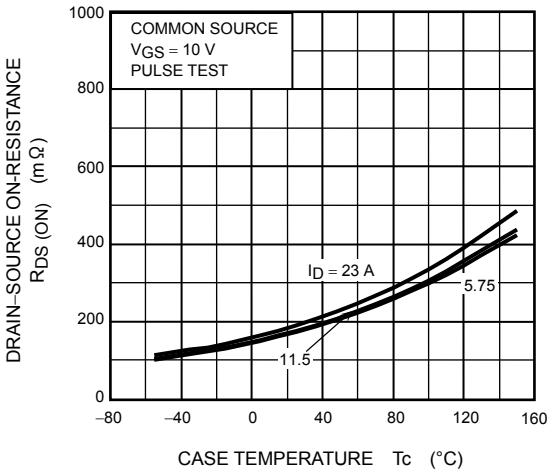
$|Y_{fs}| - I_D$



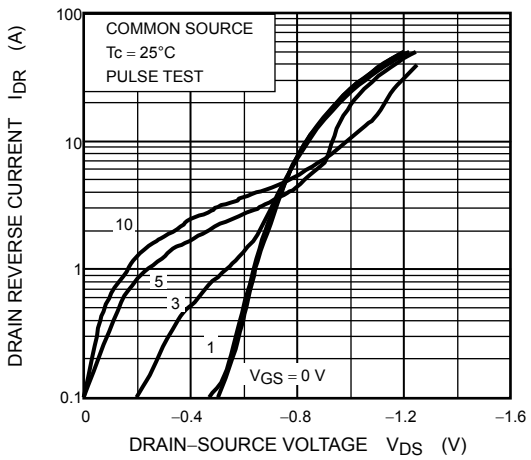
$R_{DS\ (ON)} - I_D$



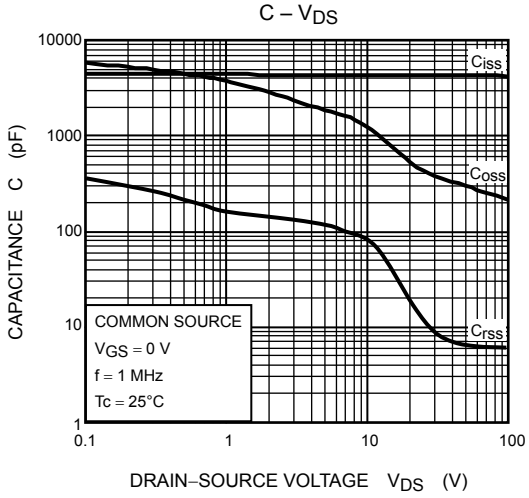
$R_{DS\ (ON)}$ – Tc



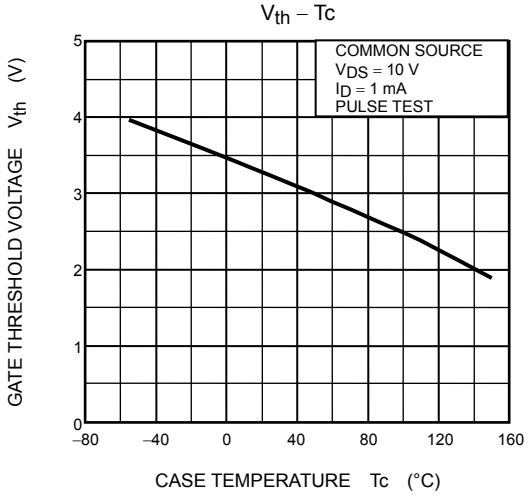
I_{DR} – V_{DS}



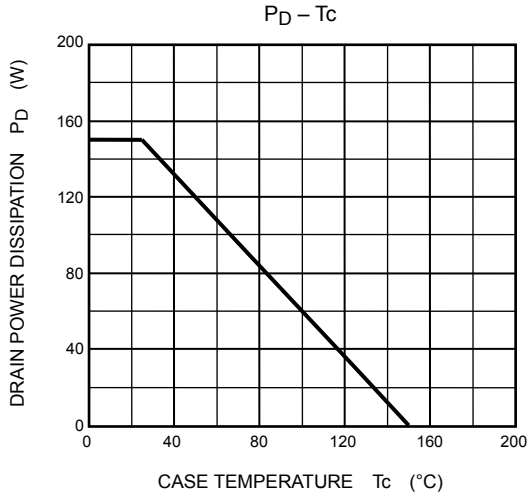
C – V_{DS}



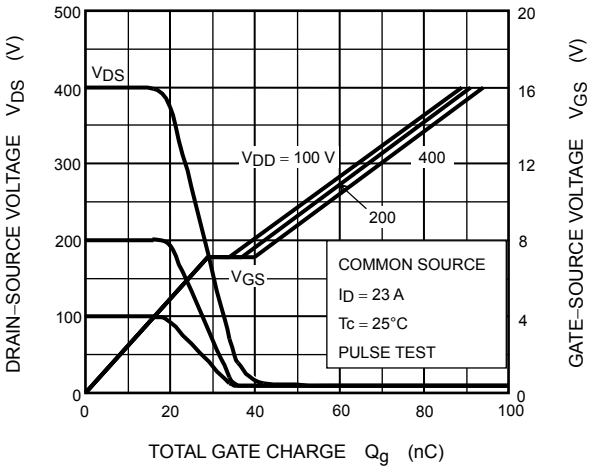
V_{th} – Tc



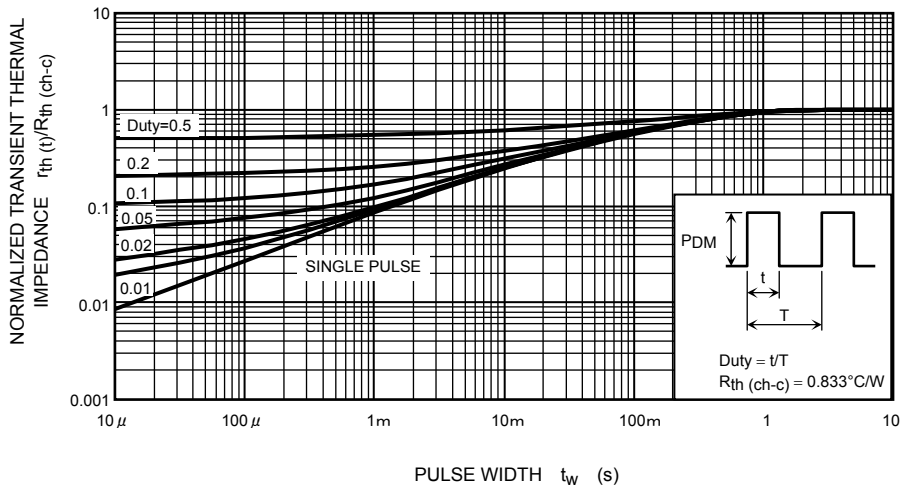
P_D – Tc



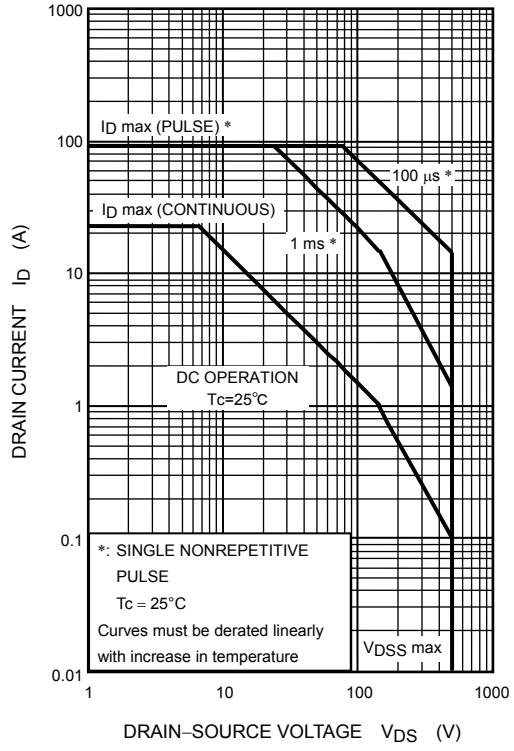
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



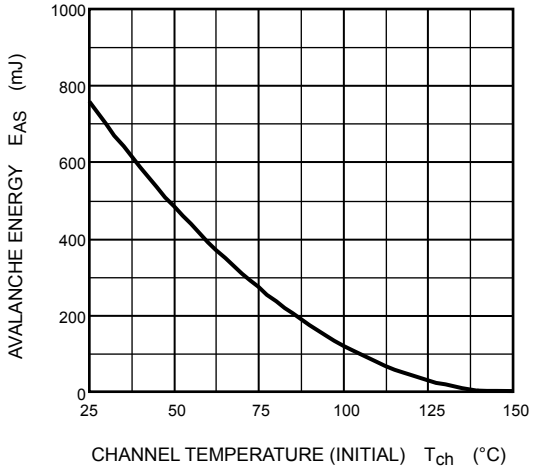
$r_{th} - t_w$

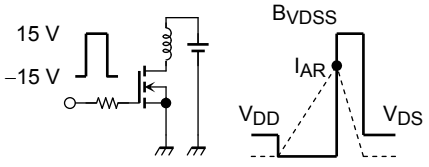


SAFE OPERATING AREA



$E_{AS} - T_{ch}$





TEST CIRCUIT WAVEFORM

$R_G = 25\ \Omega$
$V_{DD} = 90$ V, L = 2.44 mH

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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20070701-EN

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