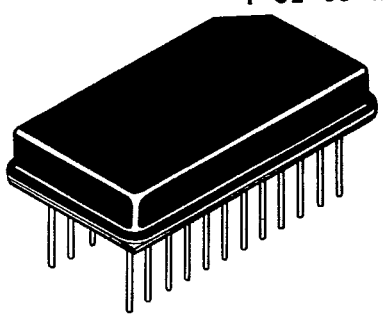
4080 Series

12 Bit/250nsec Voltage Output D/A Converters

T-51-09-12



The 4080 Series of 12 bit voltage-output D/A converters provide the ultimate in high speed, high performance digital to analog conversion. Fully three times faster than their nearest competitors, these D/As settle a 10V step to ±0.02%FSR (±2mV) in 250nsec maximum (they typically settle to ±0.01%FSR in that time). The 4080 Series consists of three similar devices offering different analog output voltage ranges: the 4080 (0 to −10V and 0 to −5V), 4081 (±2.5V and ±5V), and 4082 (0 to +10V and 0 to +5V).

4080 Series devices are housed in industry-standard, hermetically sealed, metal dual-in-line packages. Each device contains its own precision reference, and initial gain, offset, and linearity errors are actively laser trimmed to eliminate the need for external adjusting potentiometers. These adjustments are optional, however, for application requiring greater accuracies. Unlike other presently available high speed D/As 4080 Series devices are TTL (not ECL) compatible and they operate from ±15V supplies with no need for a +5V digital supply. Power consumption, at 900mW maximum, is extremely low for devices of this speed.

Standard units are fully specified for 0°C to +70°C operation. The -83 versions are specified over the -55°C to +125°C temperature range and meet the high reliability requirements of Class "B". These devices may also be ordered screened to Class "S".

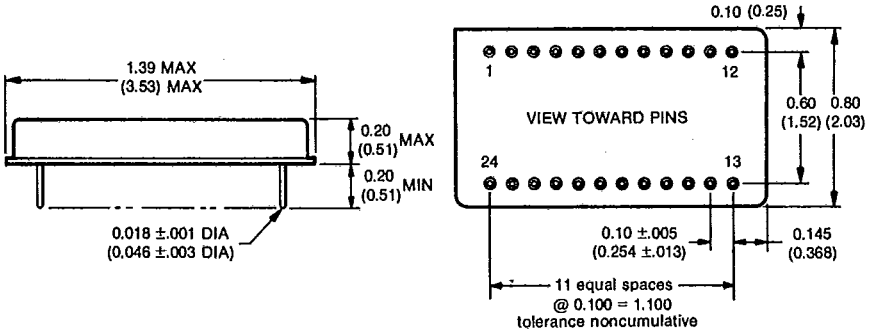
FEATURES

- 250nsec Max. Settling Time
- ±½LSB Max. Linearity Error
- Monotonicity Guaranteed Over Temperature
- TTL Compatible
- 900mW Max. Power Consumption
- −55° C to +125° C Operation

APPLICATIONS

- Digitally Controlled VCOs
- High Speed Displays
- High Speed Servo Systems
- Multiplexed Data Distribution Systems

PACKAGE DIMENSIONS Dimensions are in inches. Those in parentheses are expressed in centimeters.



PIN DESIGNATION	
1. BIT 12 (LSB)	24. −10V REF. OUT.
2. BIT 11	23. −15V SUPPLY
3. BIT 10	22. POWER GROUND
4. BIT 9	21. +15V SUPPLY
5. BIT 8	20. 5V SCALE
6. BIT 7	19. 10V SCALE
7. BIT 6	18. OUTPUT OFFSET
8. BIT 5	17. GAIN ADJUST
9. BIT 4	16. ANALOG GROUND
10. BIT 3	15. V_{OUT}
11. BIT 2	14. SUMMING JUNCTION
12. BIT 1 (MSB)	13. +IN

ABSOLUTE MAXIMUM RATINGS

+15V Supply (+V_{cc}, Pin 21)	+18V
−15V Supply (−V_{cc}, Pin 23)	−18V
Digital Input Voltage (Pins 1-12)	0 to +7V
Output Current (1)	±30mA
Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
408X	0°C to +70°C
408X-83 (2)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

SPECIFICATIONS (+25°C, ±15V supplies unless otherwise indicated.)

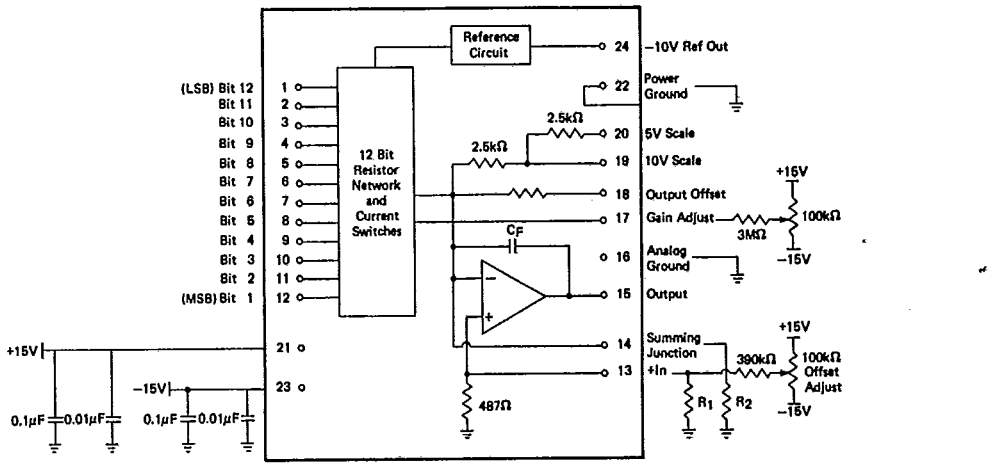
PARAMETER	MIN.	TYP.	MAX.	UNITS
DIGITAL INPUTS				
Logic Levels (3): Logic "1"	+2.0	---	+5.5	V
Logic "0"	+0	---	+0.8	V
Loading (4)	---	---	1	TTL Load
Logic Coding (5): Unipolar Ranges	---	Complementary Straight Binary	---	
Bipolar Ranges	---	Complementary Offset Binary	---	
ANALOG OUTPUTS				
Output Voltage Ranges: 4080	---	0 to −5.0, 0 to −10	---	V
4081	---	±2.5, ±5	---	V
4082	---	0 to +5.0 to +10	---	V
Output Load Current (1)	±5	±10	---	mA
Output Resistance	---	0.05	---	Ohms
TRANSFER CHARACTERISTICS (6)				
Integral Linearity Error	---	±¼	±½	LSB
Differential Linearity Error	---	±¼	---	LSB
Monotonicity	---	Guaranteed Over Temperature	---	
Offset Error (7)(8): 4080	---	±0.01	---	%FSR
4081	---	±0.05	---	%FSR
4082	---	±0.05	---	%FSR
Gain Error (7)(9)	---	±0.1	---	%
Reference Output: Voltage	---	−10.00	---	V
Accuracy	---	±0.05	---	%
External Current	---	---	2	mA
STABILITY				
Integral Linearity Drift	---	±1	---	ppm of FSR/°C
Differential Linearity Drift (10)	---	±1	---	ppm of FSR/°C
Offset Drift: 4080	---	±5	---	ppm of FSR/°C
4080-83	---	±5	±10	ppm of FSR/°C
4081	---	±5	---	ppm of FSR/°C
4081-83	---	±5	±10	ppm of FSR/°C
4082	---	±10	---	ppm of FSR/°C
4082-83	---	±10	±15	ppm of FSR/°C
Gain Drift	---	±10	±20	ppm/°C
Reference Drift	---	±10	---	ppm/°C
DYNAMIC CHARACTERISTICS				
Slew Rate	---	110	---	V/μsec
Settling Time (2kΩ load):				
10V Step to ±0.1%FSR(±10mV)	---	125	170	nsec
10V Step to ±0.02%FSR(±2mV)	---	150	250	nsec
10V Step to ±0.01%FSR(±1mV)	---	250	---	nsec
1LSB Step to ±0.01%FSR (11)	---	75	---	nsec
POWER SUPPLIES				
Power Supply Range	---	±2	---	%
Power Supply Rejection Ratio	---	±0.6	---	LSB/V
Current Drains: +15V Supply	---	+20	+30	mA
−15V Supply	---	−20	−30	mA
Power Consumption	---	600	900	mW
MTBF	---	2.1 x 10^6	---	hrs.

See notes on following page.

NOTES

1. The 4080, 4081, and 4082 are short circuit protected to ground. The reference output (pin 24) can withstand a short to ground for approximately two seconds.
2. Screened to the high reliability requirements of MIL-STD-883C, Class "B". May also be ordered screened to Class "S".
3. TTL compatible. See Optimizing Settling Time for optional use of pull-down resistors.
4. A TTL load is defined as sinking 40μA with a logic "1" applied and sourcing 1.6mA with a logic "0" applied.
5. See Logic Coding table.
6. FSR stands for Full Scale Range and is equivalent to the nominal peak-to-peak voltage of the selected output range, i.e., FSR = 5V for 0 to +5V, 0 to −5V, and ±2.5V output ranges. FSR = 10V for 0 to +10V, 0 to −10V, and ±5V output ranges. For a 12-bit converter, 1LSB = 0.024%FSR.
7. Adjustable to zero with external trim.
8. Offset Error is the difference between the actual and the ideal output voltages with a digital input of 0000 0000 0000.
9. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full output voltage span from the 0000 0000 0000 output to the 1111 1111 1111 output.
10. Monotonicity is guaranteed over each device's entire specified temperature range.
11. 0111 1111 1111 to 1000 0000 0000 digital input.

Functional Block Diagram

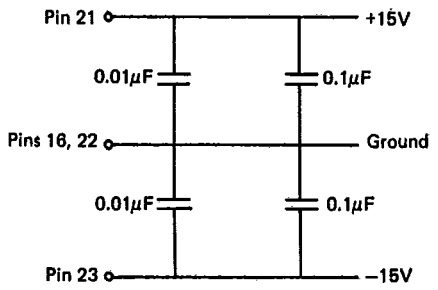


APPLICATIONS INFORMATION

Grounding and Bypassing

Unlike most D/A converters, the 4080 does not have a digital ground pin. It does, however, have separate pins for power supply ground (pin 22) and analog signal ground (pin 16). The device case is connected to the power ground pin. If your system has separate analog power and signal grounds, the 4080 should be connected accordingly. If your system employs a single analog ground, both pin 22 and pin 16 should be connected to it.

Power Supply Bypassing



For optimum performance and noise rejection, power supplies should be bypassed with 0.1μF tantalum capacitors in parallel with 0.01μF ceramic capacitors (as shown), and the capacitors should be located as close to the unit as possible. If your system employs a single ground, the D/A's bypass capacitors and load should both be connected to it as close to each other as possible to minimize lead resistance and inductance. The normally low impedance exhibited by PC board runs can become significant in high frequency applications. For high speed D/As, the result may be an inability to achieve the manufacturer's specified linearity and settling time. To minimize these impedances, PC runs should be as wide as possible. This is particularly important for analog and digital ground runs as they are the reference point for all other circuit voltages. For optimum results, ground plane techniques are essential in reducing ground impedances and stray capacitance between signal lines.

Digital Inputs

The 4080's digital inputs are standard TTL/DTL compatible. If any input bits are not used, they should either be grounded (4080) or tied to +5V (4081, 4082). Because of noise problems, open inputs should not be used as a means of generating a logic "1".

Reference Output

4080 Series devices contain an internal −10V ±0.05% reference that is pinned out at pin 24. This reference can sink up to 2mA in addition to the current requirements of connecting pin 24 to pin 18 (4081, 4082).

Optional Gain and Offset Adjustments

4080 Series devices will operate as specified without additional adjustments. If desired, input/output accuracy error can be reduced to ±0.025%FSR maximum by following the trimming procedures described below. Adjustments should be made following warmup, and to avoid interaction, offset must be adjusted before gain. Multiturn potentiometers with TCRs of 100ppm/°C or less are recommended to minimize drift with temperature. Series resistors can ±20% carbon composition or better. If these adjustments are not used, pin 17 should be left open and pin 13 should be connected as described in the Output Range Selection Table.

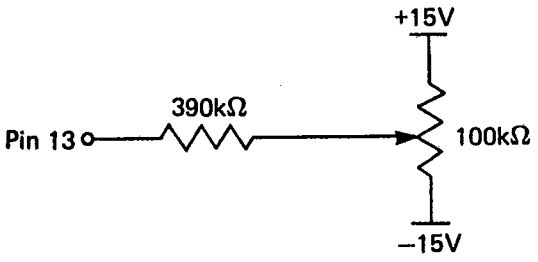


Figure 2. Offset Adjust Circuit

Offset Adjustment — Connect the offset potentiometer as shown above. Apply the code 0000 0000 0000 to the digital input and adjust the output for the ideal value listed in the Input Coding Table.

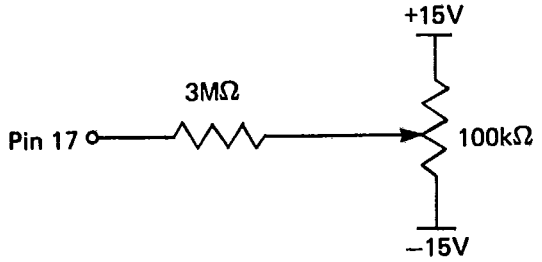


Figure 3. Gain Adjust Circuit

Gain Adjustment — Connect the gain potentiometer as shown above. Apply the code 1111 1111 1111 and adjust the output for the ideal value listed in the Input Coding Table.

External Resistors Optimize Settling Time and Offset Drift

A voltage output D/A converter usually consists of a current output D/A driving an inverting op amp that acts as a current to voltage converter. The output impedance of the current D/A is the source impedance the op amp sees, and in the case of the 4080, this impedance is a 16pF capacitance in parallel with a 604Ω resistance. When the 4080 is operating on its 0 to −10V output range, the device is pin strapped such that the op amp feedback resistor is 2.5kΩ, and the op amp feedback capacitor (internal to the device) has been chosen to optimize phase margin and settling time. The effective DC impedance seen by the op amp's inverting input is 604Ω||2.5kΩ, and a 487Ω resistor (also internal to the device) has been added between the op amp's noninverting input and ground to minimize offset drift. When the 4080 is pin strapped for 0 to −5V operation, the output op amp has a 1.25kΩ feedback resistor. It now becomes necessary to add a 604Ω resistor (R_2) between the inverting input of the output op amp (pin 14) and ground to restore the noise gain of the output op amp to once again optimize phase shift and settling time. R_1 (487Ω in this example) now has to be added between the noninverting input of the output op amp (pin 13) and ground to match the impedances seen by the op amp inputs and again minimize offset drift.

The 4081 and 4082 have similar requirements. Because pin 24 (reference output) is always connected to pin 18 (output offset) for these devices, and because internal circuitry is slightly different from that of the 4080, they have different requirements for R_2. See the Output Range Selection Table.

487Ω, 604Ω, 681Ω, and 787Ω resistors can be purchased as 1% metal film resistors, and the use of external resistors R_1 and R_2 is required for devices to guarantee their published settling time and offset drift specifications. If R_1 and R_2 are within ±10% of their required values, the effect on settling time and offset drift will be negligible. If R_1 and R_2 are not used at all (pins 13 and 14 left open) the consequences could be a 50% increase in settling time and offset drift.

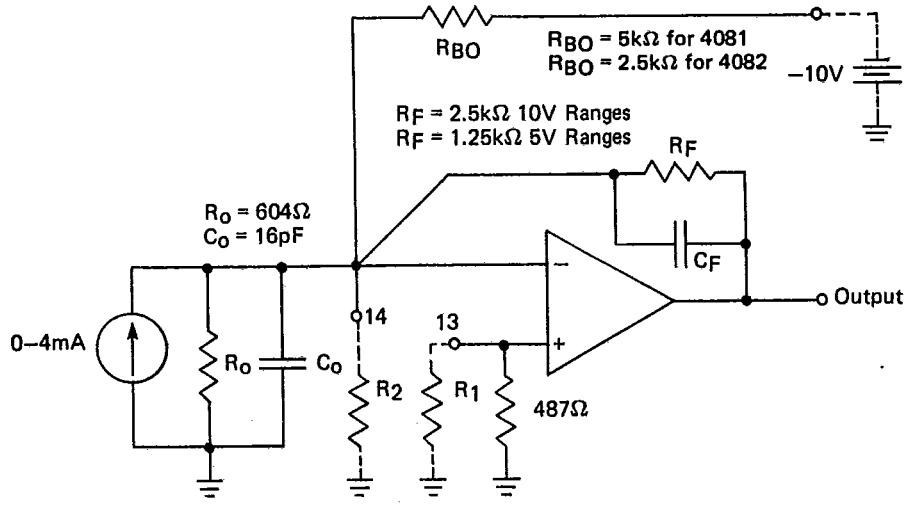


Figure 1. Current Output DAC with Output Op Amp

INPUT CODING

Digital Input			Analog Output (DC Volts)					
			4080		4081		4082	
MSB		LSB	0 to −5V	0 to −10V	±2.5V	±5V	0 to +5V	0 to +10V
0000	0000	0000	0.0000	0.0000	+2.4988	+4.9976	+4.9988	+9.9976
0000	0000	0001	−0.0012	−0.0024	+2.4976	+4.9951	+4.9976	+9.9951
0111	1111	1111	−2.4988	−4.9976	0.0000	0.0000	+2.5000	+5.0000
1000	0000	0000	−2.5000	−5.0000	−0.0012	−0.0024	+2.4988	+4.9976
1111	1111	1110	−4.9976	−9.9951	−2.4988	−4.9976	+0.0012	+0.0024
1111	1111	1111	−4.9988	−9.9976	−2.5000	−5.0000	0.0000	0.0000

OUTPUT RANGE SELECTION

Part Number	Output Voltage Range	Connect Pin	R_1 (Pin 13 to Ground)	R_2 (Pin 14 to Ground)
4080	0 to −10V 0 to −5V	19 to 15 19 to 15, 20 to 14	Open 487Ω	Open 604Ω
4081	−5V to +5V −2.5V to +2.5V	24 to 18, 19 to 15 24 to 18, 19 to 15 20 to 14	Open 487Ω	Open 681Ω
4082	0 to +10V 0 to +5V	24 to 18, 19 to 15 24 to 18, 19 to 15 20 to 14	Open 487Ω	Open 787Ω

Optimizing Settling Time

This section is a general discussion of techniques one can employ in the most critical situations to optimize a DAC's settling time by reducing glitch amplitude and digital feedthrough. It applies to all D/A converters. When properly grounded and bypassed, 4080 Series DACs will meet all their published performance specifications without taking any of the additional precautions described below.

The analog outputs (current or voltage) of all D/A converters display noise spikes, affectionately called glitches, when their digital inputs are changed. Deglitched and specially designed low-glitch DACs can minimize this noise, but no one has figured out how to eliminate it completely. Glitches can result from, among other things, unequal delays or time skew in the digital logic driving the converter and/or from unequal switching times for the current or voltage switches internal to the converter. In either case, the glitch itself may cause problems in a particular application, such as raster scan or vector displays, or the glitch may lengthen a D/A's settling time causing additional problems in other applications, such as closed loop servo systems. The easiest way to reduce a normal (not deglitched or specially designed to be low glitch) DAC's glitches to their lowest level is to follow good grounding and bypassing procedures and to eliminate unequal logic delays with external registers (latches). The most important grounding rule is that a large analog ground plane must be placed under and around the D/A converter, and in most cases, all converter ground pins should be soldered directly to the ground plane. Plastic or ceramic sockets should not be used.

Read manufacturer's data sheets carefully. Even though a given converter may have different pins for analog and digital ground, manufacturers will usually recommend tying both to system analog ground. This is required because as an interface between the analog and digital worlds, the A/D or D/A converter cannot avoid mixing analog and digital ground currents, and the least consequences are suffered by having the digital ground currents returning through the analog system. But the analog ground plane and analog ground runs, in general, must be as low impedance as possible to absorb the ground currents associated with the converter's digital inputs/outputs. Power supplies should be bypassed with at least 0.1μF tantalum capacitors (for low frequencies) paralleled with 0.01μF (for high frequencies). Single 0.1μF or larger ceramic capacitors are even better. Avoid switching power supplies—their output spikes will work their way into the analog ground system. Use accurate, linear-regulated supplies.

For D/A converters, the choice and location of an input latch is critical. Low power Schottky logic is preferred because these devices usually exhibit data delays between rising and falling signals that are more uniform than those of standard or straight Schottky TTL. Physically, the latches should be as close to the converter as possible, and the lead lengths from latch outputs to DAC inputs should all be equal.

The diagram below shows a 4080 that has been double buffered for mating to the data bus of an 8 bit microcomputer. The first 4 bit latch holds the 4 most significant bits of a given 12 bit digital word. As the 8 least significant bits are written to the 8 bit latch, the 4 MSBs are latched into the second 4 bit latch, and the DAC has all twelve of its digital inputs updated at once. By double buffering the MSBs instead of the LSBs, we retain the ability to produce LSB size output changes with a single write cycle, and we greatly reduce digital feedthrough on the MSBs.

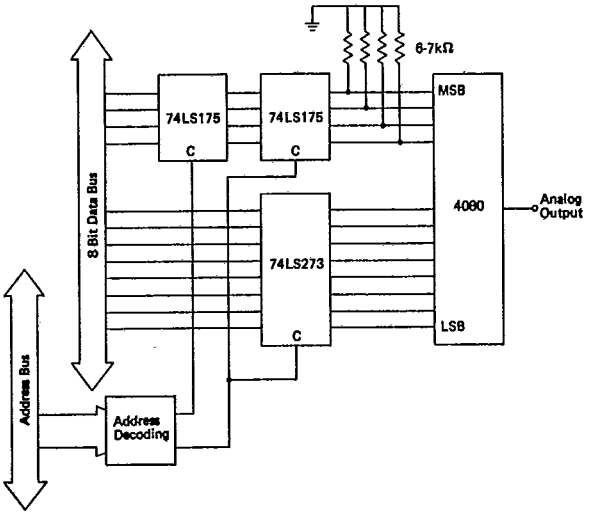


Figure 4. 4080 with Double Buffered Inputs for Mating to a 8 Bit Microcomputer

Digital feedthrough occurs when noise on top of a "1" or "0" at a DAC's input feeds through to its analog output. Digital noise from other sources can also couple its way through to a DAC's output. For the 4080, this coupling is somewhat reduced by grounding the unit's metal package. It can be further reduced by following the layout and grounding guidelines described above. Digital feedthrough, like glitches, can add to a DAC's

settling time by inducing ringing and overshoot in the output. The figure below shows the typical digital feedthrough attenuation (in dB) of the 4080. The "digital noise" source was a 100mVp-p sine wave. It was added to logic "1" (+3.5V) or logic "0" (+0.4V) and applied to all bits simultaneously. Attenuation is less (feedthrough is greater) for inputs high because this is the input state that switches (steers) current to the 4080's output. Inputs low steers current to ground. Because of the binary weighting of a DAC's digital inputs, a given noise signal will produce half as much feedthrough if it is applied to the bit 2 input than if it is applied to the bit 1 (MSB) input. Therefore, when trying to reduce digital feedthrough, concentrate on higher order digital inputs.

The digital feedthrough characteristics of a given DAC, like its glitch characteristics, have to be lived with. The best a user can do is to try to reduce external noise sources. The input registers that helped reduce glitch can also reduce digital feedthrough by reducing digital noise. Again, the latches should physically be located as close to the converter as possible. The short lead lengths that reduced digital time skew also help to avoid additional noise pickup. The latches should be physically oriented so the inputs and outputs for the more significant bits are those of the flip-flops furthest away from the chip's clock (strobe) input. This will reduce clock noise coupling into the DAC. Once again, low power Schottky logic is preferred (74LS174, 74LS175, 74LS273, etc.); in this case, because this logic family creates much less ground current noise than standard or Schottky TTL. Double buffering can even further reduce digital noise. This is another reason why one should double buffer the MSBs and not the LSBs when connecting high resolution DACs to data buses of lower resolution.

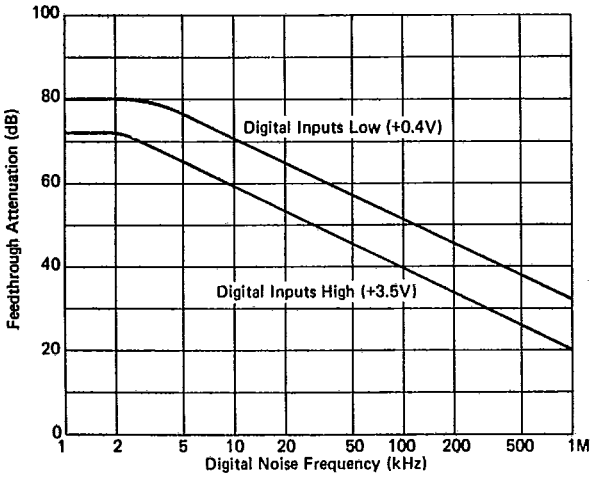


Figure 5. Digital Feedthrough Characteristics

The duty cycle of the latch strobe lines should be such that the latches are driven by as narrow pulses as possible. See the figure below. The first strobe trace shows that for positive pulses, the falling edge of each pulse occurs during the DAC's output settling time. This edge becomes one more source of digital noise that can couple through to the DAC's output. The result may be increased glitch height, but it won't affect the settling time if the pulse is narrow enough. The second strobe trace shows that for negative pulses, the falling edge of each pulse occurs before the DAC's output begins to change. Glitch and settling time are unaffected; though the DAC output may show a small perturbation prior to changing levels.

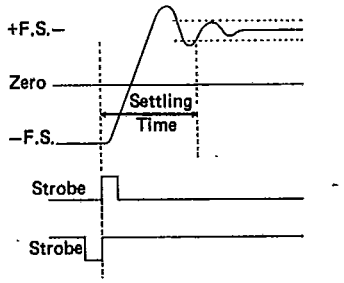


Figure 6. Input Register Strobe Duty Cycle

Another way to optimize settling time by reducing digital feedthrough is to clamp the high outputs of the DAC's digital driver as close to the threshold level as is practicably possible. The minimum voltage for a TTL input is +2.4V, yet the typical "1" output rises to about +3.5 or +4.0V. If a DAC's inputs are switched from "0's" to "1's" and they turn "on" at +2.4V, the continued rise from +2.4 to +3.5 or 4V feeds through to create a greater output glitch and a longer settling time. If the DAC's high input is clamped to +2.4V, the rise above threshold is eliminated. One way to clamp the digital inputs of a TTL DAC is with pulldown resistors from the inputs to ground. These resistors force the digital drive circuit to source more current, lowering its output voltage and source impedance. Both reduce noise and pickup and help to optimize settling. The LS gates shown above are guaranteed to source 400μA for a "1" output and still maintain a +2.4V output voltage. 6-7kΩ pulldown resistors will pull the logic "1" output down to just above +2.4V minimizing the digital feedthrough resulting from digital overdrive. Clamping some digital inputs and not others may introduce unwanted delays resulting in additional glitch. Recall that these effects are reduced with input bit weight. Figure 4 shows a 4080 with the first four digital inputs clamped.