

## 54AC175 • 54ACT175 Quad D Flip-Flop

### General Description

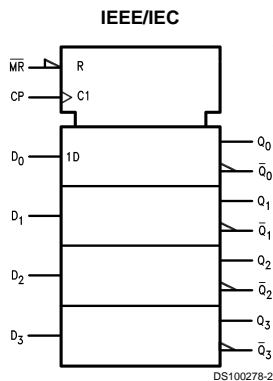
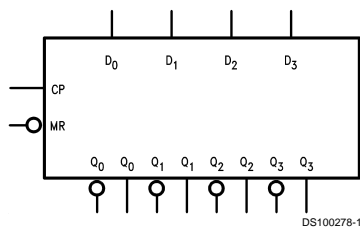
The 'AC/'ACT175 is a high-speed quad D flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

- Buffered positive edge-triggered clock
- Asynchronous common reset
- True and complement output
- Outputs source/sink 24 mA
- 'ACT175 has TTL-compatible inputs
- Standard Microcircuit Drawing (SMD)
  - 'AC175: 5962-89552
  - 'ACT175: 5962-89693

### Features

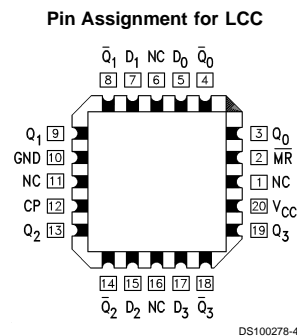
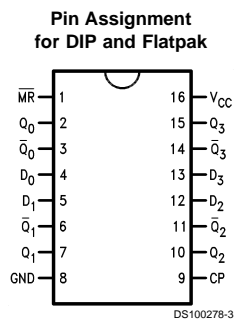
- Edge-triggered D-type inputs

### Logic Symbols



Pin Names	Description
D <sub>0</sub> –D <sub>3</sub>	Data Inputs
CP	Clock Pulse Input
$\overline{MR}$	Master Reset Input
Q <sub>0</sub> –Q <sub>3</sub>	True Outputs
$\overline{Q}_0$ – $\overline{Q}_3$	Complement Outputs

### Connection Diagrams



## Functional Description

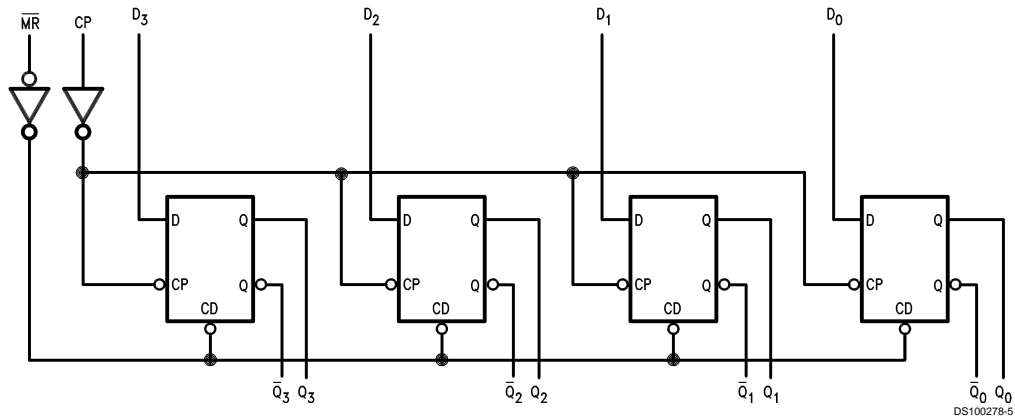
The 'AC/ACT175 consists of four edge-triggered D flip-flops with individual D inputs and Q and  $\bar{Q}$  outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH clock (CP) transition, causing individual Q and  $\bar{Q}$  outputs to follow. A LOW input on the Master Reset ( $\bar{MR}$ ) will force all Q outputs LOW and  $\bar{Q}$  outputs HIGH independent of Clock or Data inputs. The 'AC/ACT175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

## Truth Table

Inputs		Outputs	
@ $t_n$ , $\bar{MR} = H$		@ $t_{n+1}$	
$D_n$		$Q_n$	$\bar{Q}_n$
L		L	H
H		H	L

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 $t_n$  = Bit Time before Clock Pulse  
 $t_{n+1}$  = Bit Time after Clock Pulse

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DS100278-5

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	±50 mA
DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ )	±50 mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Junction Temperature ( $T_J$ )	
CDIP	175°C

## Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	
54AC/ACT	-55°C to +125°C
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
'AC Devices	
$V_{IN}$ from 30% to 70% of $V_{CC}$	
$V_{CC}$ @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
'ACT Devices	
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 4.5V, 5.5V	125 mV/ns

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

## DC Characteristics for 'AC Family Devices

Symbol	Parameter	$V_{CC}$ (V)	54AC		Units	Conditions
			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$			
			Guaranteed Limits			
$V_{IH}$	Minimum High Level Input Voltage	3.0	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	3.15			
		5.5	3.85			
$V_{IL}$	Maximum Low Level Input Voltage	3.0	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	1.35			
		5.5	1.65			
$V_{OH}$	Minimum High Level Output Voltage	3.0	2.9	V	$I_{OUT} = -50 \mu A$	
		4.5	4.4			
		5.5	5.4			
			3.0	2.4	V	(Note 2) $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA}$
			4.5	3.7		
			5.5	4.7		
$V_{OL}$	Maximum Low Level Output Voltage	3.0	0.1	V	$I_{OUT} = 50 \mu A$	
		4.5	0.1			
		5.5	0.1			
			3.0	0.50	V	(Note 2) $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA}$
			4.5	0.50		
			5.5	0.50		
$I_{IN}$	Maximum Input Leakage Current	5.5	±1.0	μA	$V_I = V_{CC}, \text{ GND}$	
$I_{OLD}$	(Note 3) Minimum Dynamic	5.5	50	mA	$V_{OLD} = 1.65V \text{ Max}$	
$I_{OHD}$	Output Current	5.5	-50	mA	$V_{OHD} = 3.85V \text{ Min}$	

### DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	54AC		Units	Conditions
			T <sub>A</sub> = -55°C to +125°C			
			Guaranteed Limits			
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	160.0		μA	V <sub>IN</sub> = V <sub>CC</sub> or GND

**Note 2:** All outputs loaded; thresholds on input associated with output under test.

**Note 3:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 4:** I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.

I<sub>CC</sub> for 54AC @ 25°C is identical to 74AC @ 25°C.

### DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V <sub>CC</sub> (V)	54ACT		Units	Conditions
			T <sub>A</sub> = -55°C to +125°C			
			Guaranteed Limits			
V <sub>IH</sub>	Minimum High Level Input Voltage	4.5	2.0		V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V
		5.5	2.0			
V <sub>IL</sub>	Maximum Low Level Input Voltage	4.5	0.8		V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V
		5.5	0.8			
V <sub>OH</sub>	Minimum High Level Output Voltage	4.5	4.4		V	I <sub>OUT</sub> = -50 μA
		5.5	5.4			
		4.5	3.70		V	(Note 5) V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = -24 mA I <sub>OH</sub> = -24 mA
		5.5	4.70			
V <sub>OL</sub>	Maximum Low Level Output Voltage	4.5	0.1		V	I <sub>OUT</sub> = 50 μA
		5.5	0.1			
		4.5	0.50		V	(Note 5) V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 24 mA I <sub>OL</sub> = 24 mA
		5.5	0.50			
I <sub>IN</sub>	Maximum Input Leakage Current	5.5	±1.0		μA	V <sub>I</sub> = V <sub>CC</sub> , GND
I <sub>CCT</sub>	Maximum I <sub>CC</sub> /Input	5.5	1.6		mA	V <sub>I</sub> = V <sub>CC</sub> - 2.1V
I <sub>OLD</sub>	(Note 6) Minimum Dynamic	5.5	50		mA	V <sub>OLD</sub> = 1.65V Max
I <sub>OHD</sub>	Output Current	5.5	-50		mA	V <sub>OHD</sub> = 3.85V Min
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	160.0		μA	V <sub>IN</sub> = V <sub>CC</sub> or GND

**Note 5:** All outputs loaded; thresholds on input associated with output under test.

**Note 6:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 7:** I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V) (Note 8)	54AC		Units	Fig. No.
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF			
			Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	3.3	95		MHz	
		5.0	95			
t <sub>PLH</sub>	Propagation Delay CP to Q <sub>n</sub> or $\overline{Q}_n$	3.3	1.0	14.5	ns	
		5.0	1.5	10.5		
t <sub>PHL</sub>	Propagation Delay CP to Q <sub>n</sub> or $\overline{Q}_n$	3.3	1.0	15.0	ns	
		5.0	1.5	11.5		
t <sub>PLH</sub>	Propagation Delay $\overline{MR}$ to $\overline{Q}_n$	3.3	1.0	15.0	ns	
		5.0	1.5	11.0		
t <sub>PHL</sub>	Propagation Delay $\overline{MR}$ to Q <sub>n</sub>	3.3	1.0	13.5	ns	
		5.0	1.5	10.5		

**Note 8:** Voltage Range 3.3 is 3.3V ±0.3V  
Voltage Range 5.0 is 5.0V ±0.5V

## AC Operating Requirements

Symbol	Parameter	V <sub>CC</sub> (V) (Note 9)	54AC		Units	Fig. No.
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF			
			Guaranteed Minimum			
t <sub>s</sub>	Setup Time, HIGH or LOW D <sub>n</sub> to CP	3.3	5.0		ns	
		5.0	3.5			
t <sub>h</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP	3.3	2.0		ns	
		5.0	2.5			
t <sub>w</sub>	CP Pulse Width HIGH or LOW	3.3	6.0		ns	
		5.0	5.0			
t <sub>w</sub>	$\overline{MR}$ Pulse Width, LOW	3.3	5.5		ns	
		5.0	5.0			
t <sub>rec</sub>	Recovery Time $\overline{MR}$ to CP	3.3	1.5		ns	
		5.0	1.5			

**Note 9:** Voltage Range 3.3 is 3.3V ±0.3V  
Voltage Range 5.0 is 5.0V ±0.5V

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V) (Note 10)	54ACT		Units	Fig. No.
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF			
			Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	5.0	95		MHz	
t <sub>PLH</sub>	Propagation Delay CP to Q <sub>n</sub> or $\bar{Q}_n$	5.0	1.5	11.5	ns	
t <sub>PHL</sub>	Propagation Delay CP to Q <sub>n</sub> or $\bar{Q}_n$	5.0	1.5	12.5	ns	
t <sub>PLH</sub>	Propagation Delay MR to Q <sub>n</sub>	5.0	1.5	11.5	ns	
t <sub>PHL</sub>	Propagation Delay $\overline{MR}$ to Q <sub>n</sub>	5.0	1.5	11.0	ns	

Note 10: Voltage Range 5.0 is 5.0V ±0.5V

## AC Operating Requirements

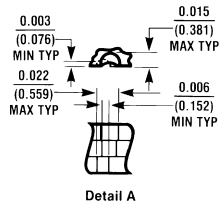
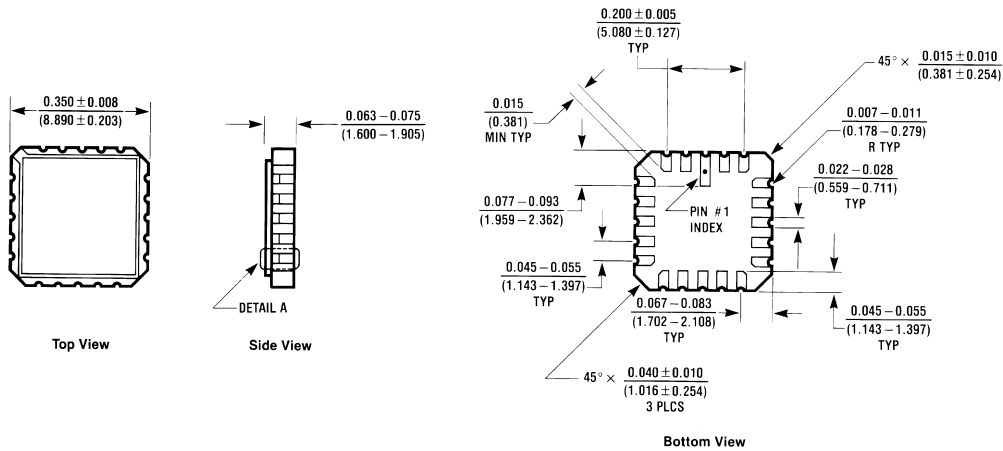
Symbol	Parameter	V <sub>CC</sub> (V) (Note 11)	54ACT		Units	Fig. No.
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF			
			Guaranteed Minimum			
t <sub>s</sub> (H)	Setup Time	5.0	3.5		ns	
t <sub>s</sub> (L)	D <sub>n</sub> to CP	5.0	3.5		ns	
t <sub>h</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP	5.0	1.5		ns	
t <sub>w</sub>	CP Pulse Width HIGH or LOW	5.0	5.0		ns	
t <sub>w</sub>	$\overline{MR}$ Pulse Width, LOW	5.0	5.0		ns	
t <sub>rec</sub>	Recovery Time, MR to CP	5.0	1.5		ns	

Note 11: Voltage Range 5.0 is 5.0V ±0.5V

## Capacitance

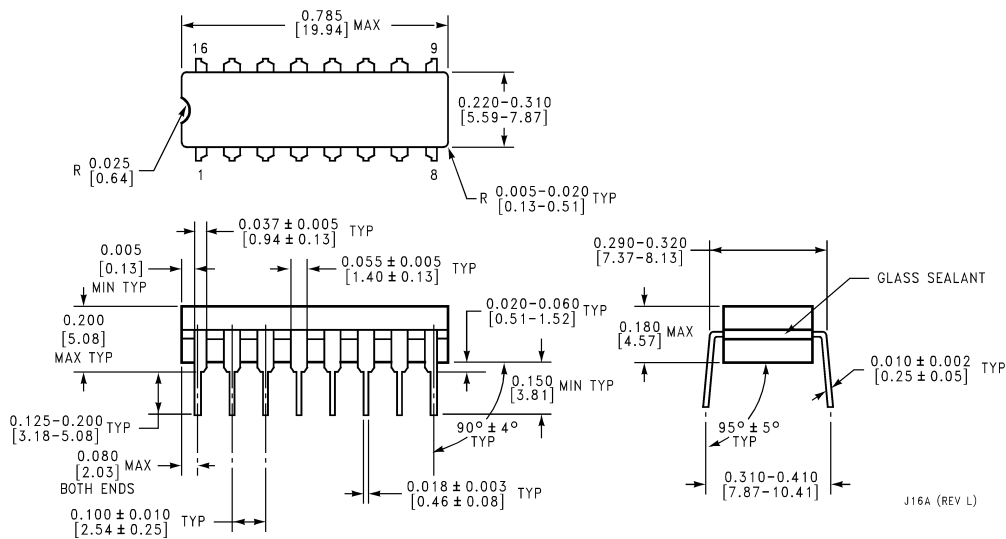
Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = OPEN
C <sub>PD</sub>	Power Dissipation Capacitance	45.0	pF	V <sub>CC</sub> = 5.0V

**Physical Dimensions** inches (millimeters) unless otherwise noted



**20 Terminal Ceramic Leadless Chip Carrier (L)**  
 NS Package Number E20A

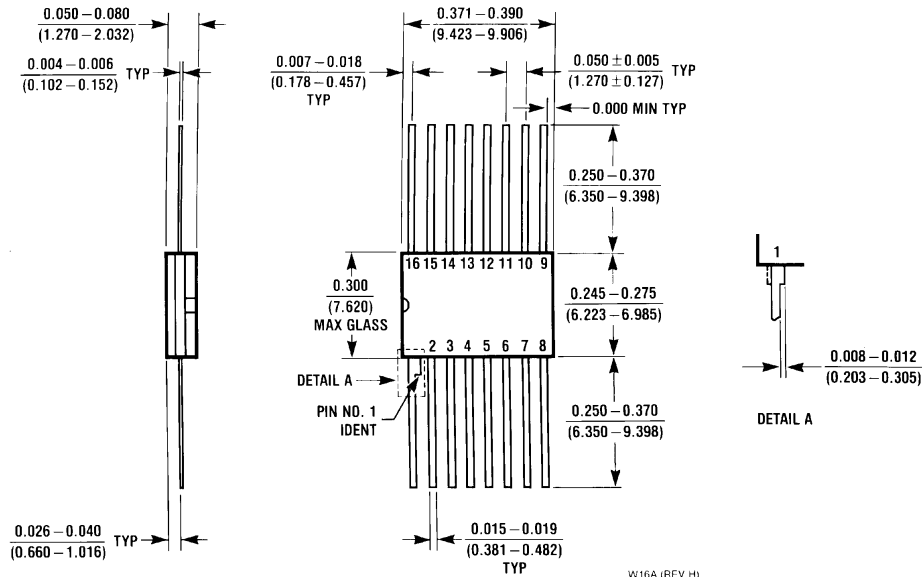
E20A (REV D)



**16-Lead Ceramic Dual-In-Line Package (D)**  
 NS Package Number J16A

J16A (REV L)

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Ceramic Flatpak (F)  
NS Package Number W16A**

**LIFE SUPPORT POLICY**

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



**National Semiconductor Corporation**  
Americas  
Tel: 1-800-272-9959  
Fax: 1-800-737-7018  
Email: support@nsc.com

**National Semiconductor Europe**  
Fax: +49 (0) 1 80-530 85 86  
Email: europe.support@nsc.com  
Deutsch Tel: +49 (0) 1 80-530 85 85  
English Tel: +49 (0) 1 80-532 78 32  
Français Tel: +49 (0) 1 80-532 93 58  
Italiano Tel: +49 (0) 1 80-534 16 80

**National Semiconductor Asia Pacific Customer Response Group**  
Tel: 65-2544466  
Fax: 65-2504466  
Email: sea.support@nsc.com

**National Semiconductor Japan Ltd.**  
Tel: 81-3-5620-6175  
Fax: 81-3-5620-6179

www.national.com