

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Make corrections on sheet 11 Terminal connections for case outline X. Update boilerplate to MIL-PRF-38535 requirements.- LTG	02-08-27	Thomas M. Hess
B	Update boilerplate to current MIL-PRF-38535 requirements. - CFS	07-11-19	Thomas M. Hess

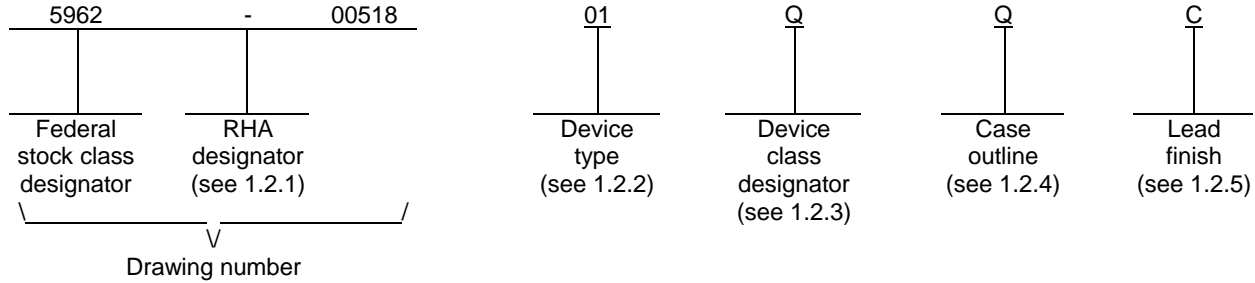
REV																			
SHEET																			
REV	B	B	B	B	B														
SHEET	15	16	17	18	19														
REV STATUS OF SHEETS	REV			B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
	SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14	14	

PMIC N/A	PREPARED BY Larry T. Gauder	<p align="center">DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990 http://www.dsccl.dla.mil</p> <p align="center">MICROCIRCUIT, DIGITAL, CMOS, 8-BIT MICROCONTROLLER, MONOLITHIC SILICON</p>																	
<p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY Thanh V. Nguyen																		
	APPROVED BY Monica L. Poelking																		
	DRAWING APPROVAL DATE 00-10-05																		
	REVISION LEVEL B	SIZE A	CAGE CODE 67268	5962-00518															
	SHEET	1 OF 19																	

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	80C32	CMOS 8-bit microcontroller

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
Q	CDIP2-T40	40	Dual-in-line
X	CQCC2-J44	44	"J" lead chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

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1.3 Absolute maximum ratings. 1/

Supply voltage (V_{DD}).....	-0.3 V to +7.0 V
Input voltage (V_{IN}).....	-0.3 V to $V_{DD} + 0.3$ V
Output current (I_{OUT}).....	80 mA
Power dissipation (P_D).....	0.3 W
Storage temperature range (T_{stg}).....	-65°C to 150°C
Lead temperature (soldering 10 seconds).....	+265°C
Junction temperature (T_J).....	165°C
Thermal resistance, junction to case (θ_{JC}).....	30°C/W

1.4 Recommended operating conditions.

Supply voltage range (V_{DD}).....	4.5 V dc to 5.5 V dc
Case operating temperature range (T_C).....	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Functional diagram. The functional diagram shall be as specified on figure 2.

3.2.4 Timing waveforms. The timing waveforms shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High output voltage	V _{OH1}	I _{OH} = -400 μA V _{DD} = 4.5 V, V _{SS} = 0.0 V	1, 2, 3	All	2.4		V
	V _{OH2}	I _{OH} = -60 μA V _{DD} = 4.5 V, V _{SS} = 0.0 V	1, 2, 3	All	2.4		V
	V _{OH3} 1/	I _{OH} = -150 μA V _{DD} = 4.5 V, V _{SS} = 0.0 V	1, 2, 3	All	3.375		V
	V _{OH4} 1/	I _{OH} = -25 μA V _{DD} = 4.5 V, V _{SS} = 0.0 V	1, 2, 3	All	3.375		V
	V _{OH5} 1/	I _{OH} = -40 μA V _{DD} = 4.5 V, V _{SS} = 0.0 V	1, 2, 3	All	4.05		V
	V _{OH6} 1/	I _{OH} = -10 μA V _{DD} = 4.5 V, V _{SS} = 0.0 V	1, 2, 3	All	4.04		V
Low output voltage	V _{OL1}	I _{OL} = 3.2 mA V _{DD} = 4.5 V, V _{SS} = 0.0 V	1, 2, 3	All		0.45	V
	V _{OL2}	I _{OL} = 1.6 mA V _{DD} = 4.5 V, V _{SS} = 0.0 V	1, 2, 3	All		0.45	V
Quiescent current	I _{DD} 2/	V _{DD} = 5.5 V, V _{SS} = 0.0 V f = 30 MHz	1, 2, 3	All		15	mA
Supply current	I _{DD(S)} 3/	V _{DD} = 5.5 V, V _{SS} = 0.0 V f = 30 MHz	1, 2, 3	All		50	mA
Power down supply current	I _{DD(PD1)} 1/ 4/	V _{DD} = 2.0 V, V _{SS} = 0.0 V	1, 2, 3	All		75	μA
	I _{DD(PD2)} 4/	V _{DD} = 5.5 V, V _{SS} = 0.0 V	1, 2, 3	All		75	μA
Low level input leakage current	I _{IL}	V _{IN} (Under Test) = 0.45 V V _{DD} = 5.5 V, V _{SS} = 0.0 V	1, 2, 3	All	-10	10	μA
High level input leakage current	I _{IH}	V _{IN} (Under Test) = 5.5 V V _{DD} = 5.5 V, V _{SS} = 0.0 V	1, 2, 3	All	-10	10	μA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Low level input current	I _{IL2}	V _{IN} (Under Test) = 0.45 V V _{IN} (Remaining Inputs) = 0.0 V V _{DD} = 5.5 V, V _{SS} = 0.0 V	1, 2, 3	All	-75		μA
High to low transition current	I _{IT}	V _{IN} (Under Test) = 2.0 V V _{IN} (Remaining Inputs) = 0.0 V V _{DD} = 5.5 V, V _{SS} = 0.0 V	1, 2, 3	All	-750		μA
Input clamp voltage (to V _{SS}) <u>1/</u>	V _{IC1}	I _{IN} (Under Test) = 100 μA V _{DD} = Open, V _{SS} = 0.0 V	1, 2, 3	All	0.2		V
Input clamp voltage (to V _{DD}) <u>1/</u>	V _{IC2}	I _{IN} (Under Test) = 100 μA V _{DD} = 0.0 V, V _{SS} = Open	1, 2, 3	All		-0.2	V
Reset resistor	RRST	V _{DD} = 4.5 V	1, 2, 3	All	50	200	kΩ
Functional test 1, Instruction set <u>5/</u>		Verify truth table without load V _{IL} = 0.0 V, V _{IH} = 3.0 V V _{OUT} = 1.5 V V _{DD} = 4.0 V, V _{SS} = 0.0 V f = 1.0 MHz See 4.4.1b	7, 8	All			
Functional test 2, Internal register <u>5/</u>		Verify truth table without load V _{IL} = 0.0 V, V _{IH} = 3.0 V V _{OUT} = 1.5 V, f = 1.0 MHz V _{DD} = 5.5 V, V _{SS} = 0.0 V See 4.4.1b	7, 8	All			
Functional test 3, Interrupts <u>5/</u>		Verify truth table without load V _{IL} = 0.8 V, V _{IH} = 2.2 V V _{OUT} = 1.5 V, f = 1.0 MHz V _{DD} = 4.5 V, V _{SS} = 0.0 V See 4.4.1b	7, 8	All			
Functional test 4, Timer <u>5/</u>		Verify truth table without load V _{IL} = 0.8 V, V _{IH} = 2.2 V V _{OUT} = 1.5 V, f = 1.0 MHz V _{DD} = 5.5 V, V _{SS} = 0.0 V See 4.4.1b	7, 8	All			
Functional test 5, Serial port <u>5/</u>		Verify truth table with load V _{IL} = 0.0 V, V _{IH} = 3.0 V V _{OUT} = 1.5 V, f = 1.0 MHz V _{DD} = 4.5 V, V _{SS} = 0.0 V See 4.4.1b Outputs: 1TTL +50 pF	7, 8	All			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Functional test 6, External data <u>5/</u>		Verify truth table with load V _{IL} = 0.0 V, V _{IH} = 3.0 V V _{OUT} = 1.5 V, , f = 1.0 MHz V _{DD} = 5.5 V, V _{SS} = 0.0 V See 4.4.1b Outputs: 1TTL +50 pF	7, 8	All			
Functional test 7, Program counter <u>5/</u>		Verify truth table with load V _{IL} = 0.0 V, V _{IH} = 3.0 V V _{OUT} = 1.5 V, , f = 12 MHz V _{DD} = 4.5 V, V _{SS} = 0.0 V See 4.4.1b Outputs: 1TTL +50 pF	7, 8	All			
Functional test 8, Ram <u>5/</u>		Verify truth table with load V _{IL} = 0.0 V, V _{IH} = 3.0 V V _{OUT} = 1.5 V, , f = 12 MHz V _{DD} = 5.5 V, V _{SS} = 0.0 V See 4.4.1b Outputs: 1TTL +50 pF	7, 8	All			
Input/output capacitance	C _{IN} /C _{OUT}	V _{IN/OUT} (Not under test) = 0 V V _{DD} = V _{SS} = 0.0 V f = 1.0 MHz, See 4.4.1c	4	All		10	pF
ALE pulse width <u>6/</u>	t _{LHLL}	f = 30 MHz V _{DD} = 4.5 V and 5.5 V, V _{SS} = 0.0 V See figure 4	9, 10, 11	All	60		ns
Address valid to ALE <u>6/</u>	t _{AVLL}		9, 10, 11	All	15		ns
Address hold to ALE <u>6/</u>	t _{LLAX}		9, 10, 11	All	35		ns
ALE to valid Inst. in <u>6/</u>	t _{LLIV}		9, 10, 11	All	100		ns
PSEN to valid Inst. in <u>6/</u>	t _{PLIV}		9, 10, 11	All	65		ns
Address to valid Inst. in <u>6/</u>	t _{AVIV}		9, 10, 11	All	130		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{\text{RD}}$ to valid data in $\underline{\text{6}}$ /	t _{RLDV}	f = 30 MHz V _{DD} = 4.5 V and 5.5 V, V _{SS} = 0.0 V See figure 4	9, 10, 11	All	135		ns
ALE to valid data in $\underline{\text{6}}$ /	t _{LLDV}		9, 10, 11	All	235		ns
ALE to $\overline{\text{WR}}$ $\underline{\text{6}}$ /	t _{LLWL}		9, 10, 11	All	90	115	ns
Address to $\overline{\text{WR}}$ $\underline{\text{6}}$ /	t _{AVWL}		9, 10, 11	All	115		ns
Address to $\overline{\text{RD}}$ $\underline{\text{6}}$ /	t _{AVRL}		9, 10, 11	All	115		ns
ALE to $\overline{\text{PSEN}}$ $\underline{\text{1}}$ /	t _{LLPL}		9, 10, 11	All	25		ns
$\overline{\text{PSEN}}$ pulse width $\underline{\text{1}}$ /	t _{PLPH}		9, 10, 11	All	80		ns
$\overline{\text{PSEN}}$ to in Inst. hold $\underline{\text{1}}$ /	t _{PXIX}		9, 10, 11	All		0.0	ns
$\overline{\text{PSEN}}$ to address valid $\underline{\text{1}}$ /	t _{PXAV}		9, 10, 11	All	30		ns
$\overline{\text{RD}}$ pulse width $\underline{\text{1}}$ /	t _{RLRH}		9, 10, 11	All	180		ns
$\overline{\text{WR}}$ pulse width $\underline{\text{1}}$ /	t _{WLWH}		9, 10, 11	All	180		ns
ALE to data address hold $\underline{\text{1}}$ /	t _{LLAXR}		9, 10, 11	All	55		ns
$\overline{\text{RD}}$ to data hold $\underline{\text{1}}$ /	t _{RHDX}		9, 10, 11	All		0.0	ns
$\overline{\text{RD}}$ to data float $\underline{\text{1}}$ /	t _{RHDZ}		9, 10, 11	All	60		ns
Address to valid data in $\underline{\text{1}}$ /	t _{AVDV}		9, 10, 11	All	260		ns
ALE to $\overline{\text{RD}}$ $\underline{\text{1}}$ /	t _{LLRL}		9, 10, 11	All	90	115	ns
Data valid to $\overline{\text{WR}}$ $\underline{\text{1}}$ /	t _{QVWX}		9, 10, 11	All	20		ns
Data setup to $\overline{\text{WR}}$ high $\underline{\text{1}}$ /	t _{QVWH}		9, 10, 11	All	215		ns
$\overline{\text{WR}}$ to data hold $\underline{\text{1}}$ /	t _{WHQX}		9, 10, 11	All	20		ns
$\overline{\text{RD}}$ low to address float $\underline{\text{1}}$ /	t _{RLAZ}		9, 10, 11	All		0.0	ns
$\overline{\text{WR}}$ high to ALE high $\underline{\text{1}}$ /	t _{WHLH}		9, 10, 11	All	20	40	ns
$\overline{\text{RD}}$ high to ALE high $\underline{\text{1}}$ /	t _{RHLH}		9, 10, 11	All	20	40	ns
Serial port clock cycle time $\underline{\text{1}}$ /	t _{XLXL}		9, 10, 11	All	400		ns
Out data setup to clock $\underline{\text{1}}$ /	t _{QVXH}		9, 10, 11	All	300		ns
Clock to out data hold $\underline{\text{1}}$ /	t _{XHQX}		9, 10, 11	All	50		ns
Clock to in data hold $\underline{\text{1}}$ /	t _{XHDX}		9, 10, 11	All		0.0	ns
Clock high to in data valid $\underline{\text{1}}$ /	t _{XHDV}		9, 10, 11	All	300		ns

See footnotes on next sheet.

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TABLE I. Electrical performance characteristics – Continued.

- 1/ Guaranteed but not tested.
- 2/ I_{DD} is measured with all output pins disconnected; XTAL1 driven with $t_{CLCH} = t_{CHCL} = 5.0$ ns, $V_{IL} = V_{SS} + 0.5$ V, $V_{IH} = V_{DD} - 0.5$ V; XTAL2 = NC; $\overline{EA} = RST = V_{SS}$; PORT0 = V_{DD} .
- 3/ $I_{DD(S)}$ is measured with all output pins disconnected; XTAL1 driven with $t_{CLCH} = t_{CHCL} = 5.0$ ns, $V_{IL} = V_{SS} + 0.5$ V, $V_{IH} = V_{DD} - 0.5$ V; XTAL2 = NC; PORT0 = $\overline{EA} = RST = V_{SS}$.
- 4/ $I_{DD(PD)}$ is measured with all output pins disconnected; $\overline{EA} = PORT0 = V_{DD}$; XTAL2 = NC; XTAL1 = RST = V_{SS} .
- 5/ Functional test includes: Instruction set, Internal registers, Interrupts, Timer, Serial port, External data, Program counter, Ram, Idle mode, Power-down mode.
Other parameters (guaranteed):

$V_{IL} \text{ min} = -0.5 \text{ V}$	$V_{IL} \text{ max} = 0.2V_{DD} - 0.25 \text{ V}$ (0.85 V at 5.5 V) Except pin \overline{EA} : $V_{IL} \text{ max} = 0.2V_{DD} - 0.45 \text{ V}$.
$V_{IH} \text{ max} = V_{DD} + 0.5 \text{ V}$	$V_{IH} \text{ min} = 0.2V_{DD} + 1.1 \text{ V}$ (2.0 V at 4.5 V) Except pins XTAL1, RESET: $V_{IH} \text{ min} = 0.7V_{DD} + 0.2 \text{ V}$.

6/ Measurements shall be performed on a 100 percent basis, Read and Record.

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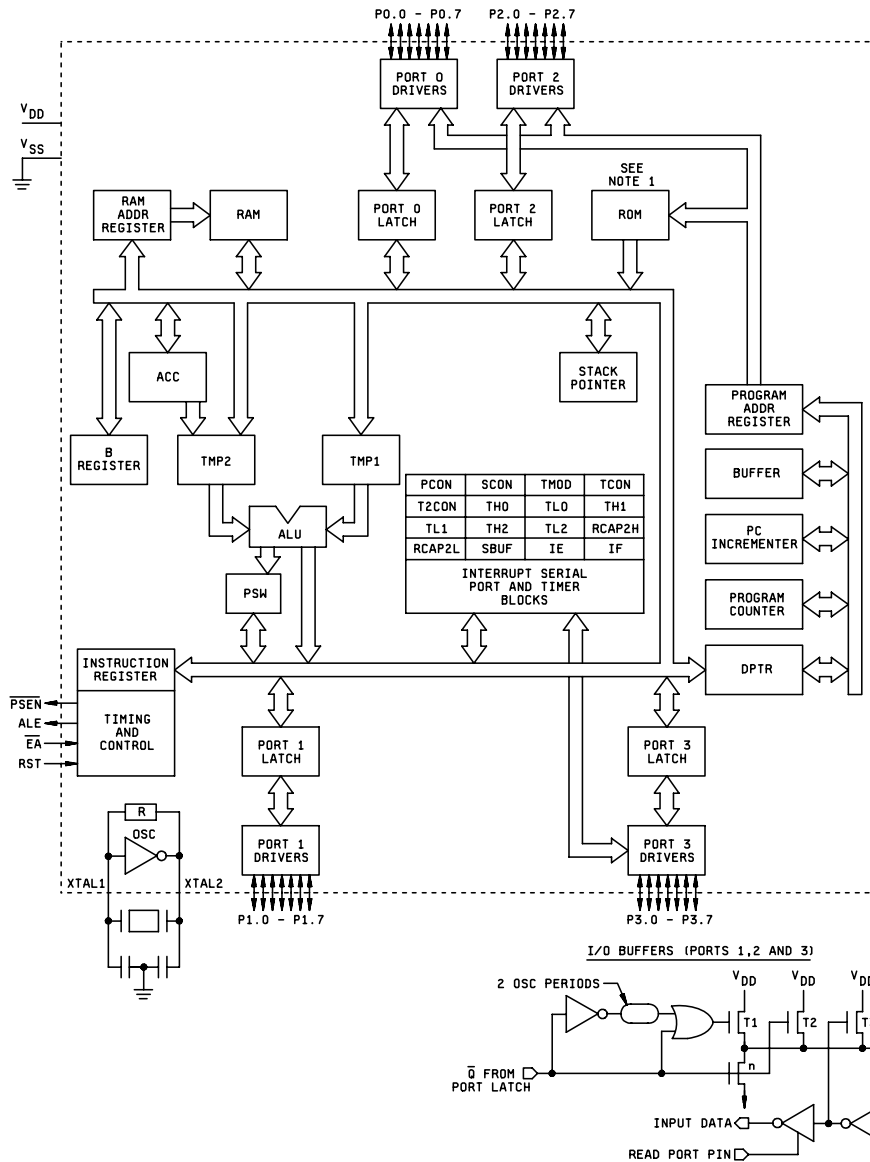
Device type		01	
Case outline		Q	
Pin Number	Pin Symbol	Pin Number	Pin Symbol
1	T2/P1.0	21	P2.0
2	T2EX/P1.1	22	P2.1
3	P1.2	23	P2.2
4	P1.3	24	P2.3
5	P1.4	25	P2.4
6	P1.5	26	P2.5
7	P1.6	27	P2.6
8	P1.7	28	<u>P2.7</u>
9	RST	29	PSEN
10	P3.0/RXD	30	<u>ALE</u>
11	P3.1/TXD	31	EA
12	P3.2/INT0	32	P0.7
13	P3.3/INT1	33	P0.6
14	P3.4/T0	34	P0.5
15	P3.5/T1	35	P0.4
16	P3.6/WR	36	P0.3
17	P3.7/RD	37	P0.2
18	XTAL2	38	P0.1
19	XTAL1	39	P0.0
20	V _{SS}	40	V _{DD}

Device type		01	
Case outline		X	
Pin Number	Pin Symbol	Pin Number	Pin Symbol
1	NC	23	NC
2	T2/P1.0	24	P2.0
3	T2EX/P1.1	25	P2.1
4	P1.2	26	P2.2
5	P1.3	27	P2.3
6	P1.4	28	P2.4
7	P1.5	29	P2.5
8	P1.6	30	P2.6
9	P1.7	31	<u>P2.7</u>
10	RST	32	PSEN
11	P3.0.RXD	33	ALE
12	NC	34	<u>NC</u>
13	P3.1/TXD	35	EA
14	P3.2/INT0	36	P0.7
15	P3.3/INT1	37	P0.6
16	P3.4/T0	38	P0.5
17	P3.5/T1	39	P0.4
18	P3.6/WR	40	P0.3
19	P3.7/RD	41	P0.2
20	XTAL2	42	P0.1
21	XTAL1	43	P0.0
22	V _{SS}	44	V _{DD}

NC = No connection.

FIGURE 1. Terminal connections.

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NOTE: For this device, the ROM is only externally addressable and by using \overline{EA} signal requirements.

FIGURE 2. Functional diagram.

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INTERNAL CLOCK WAVEFORMS

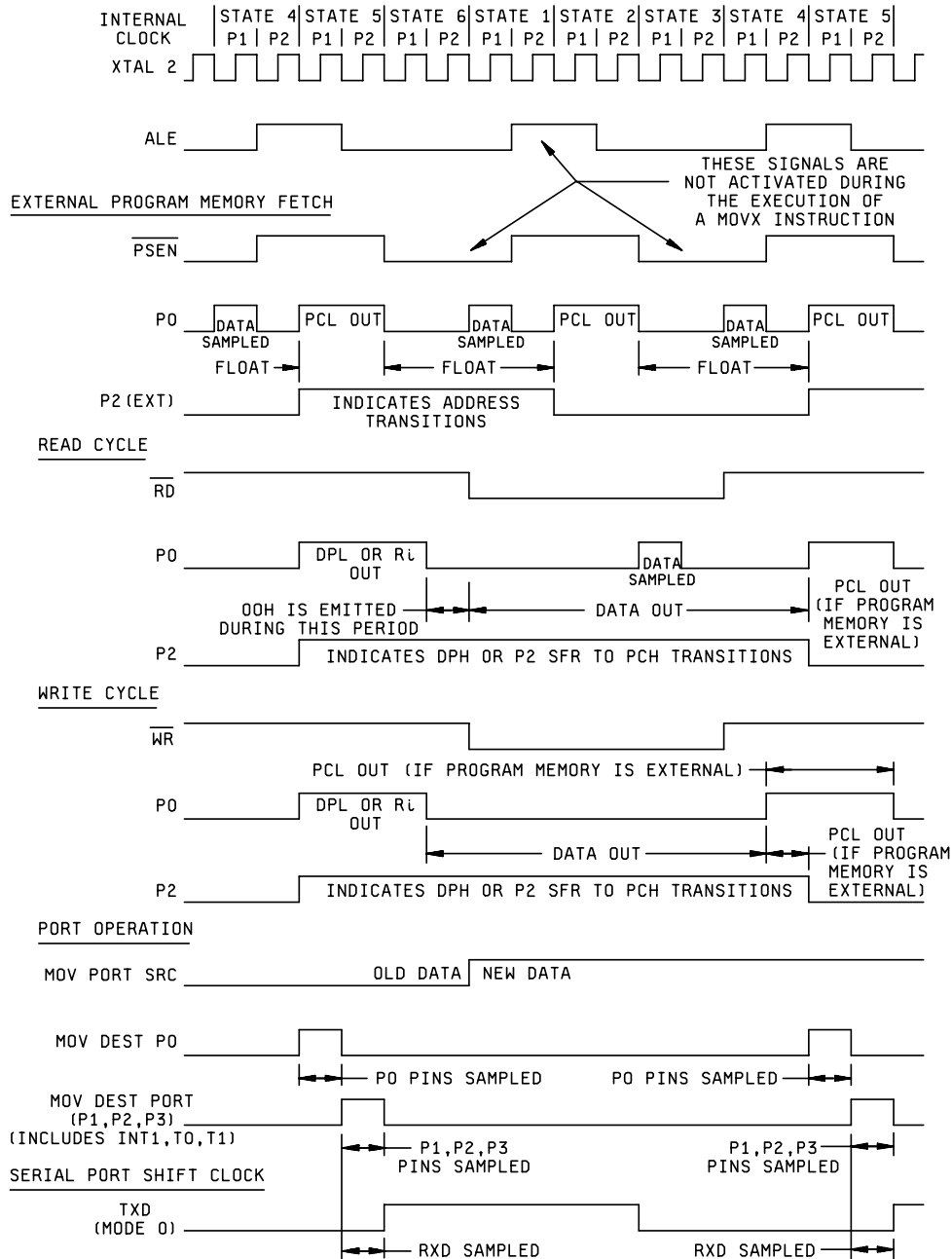


FIGURE 3. Timing waveforms.

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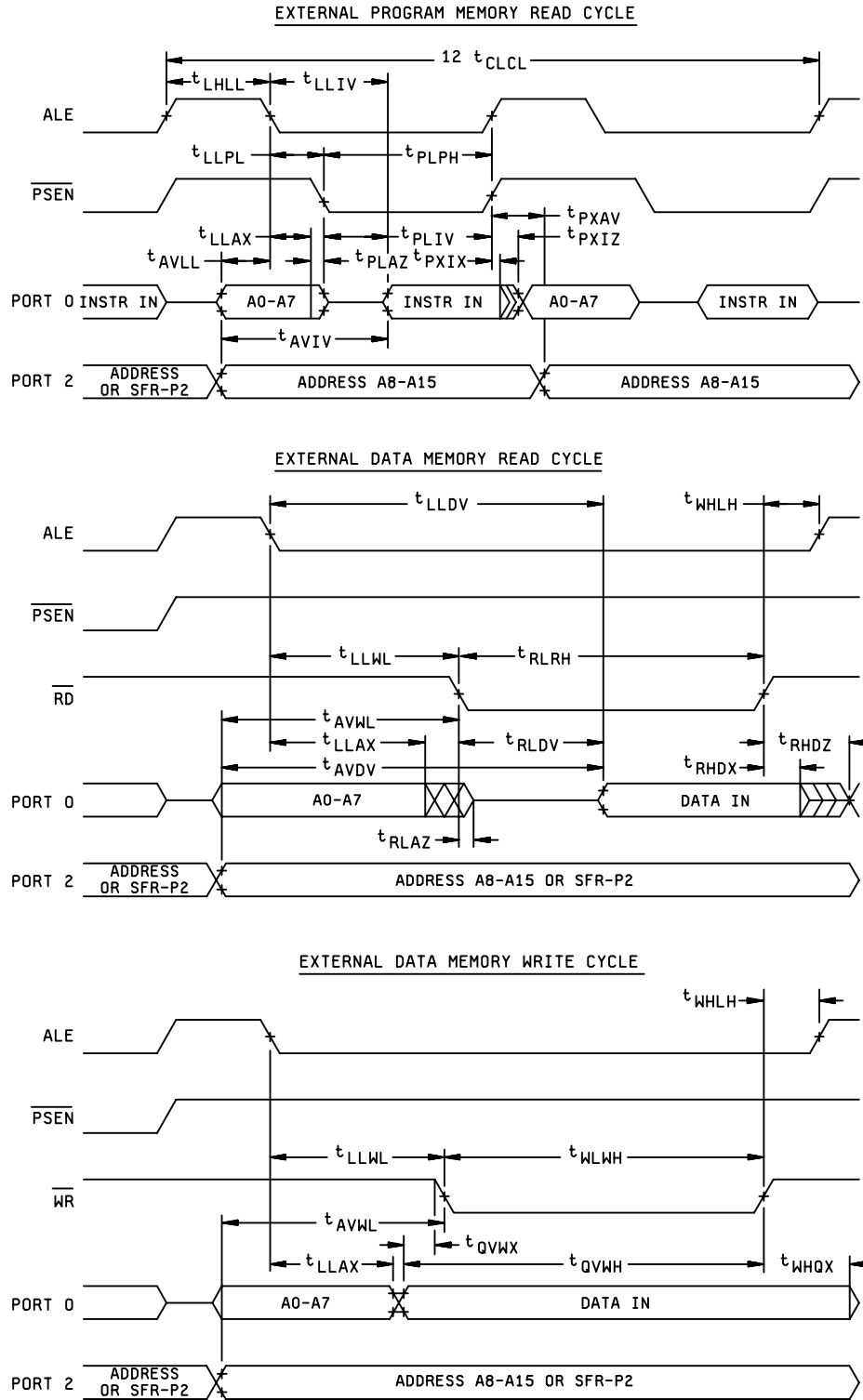
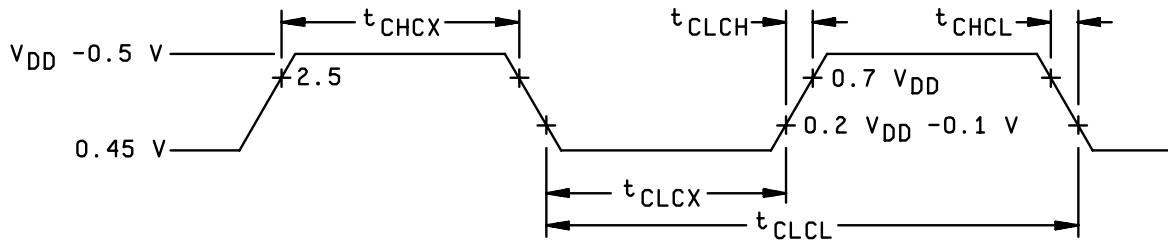


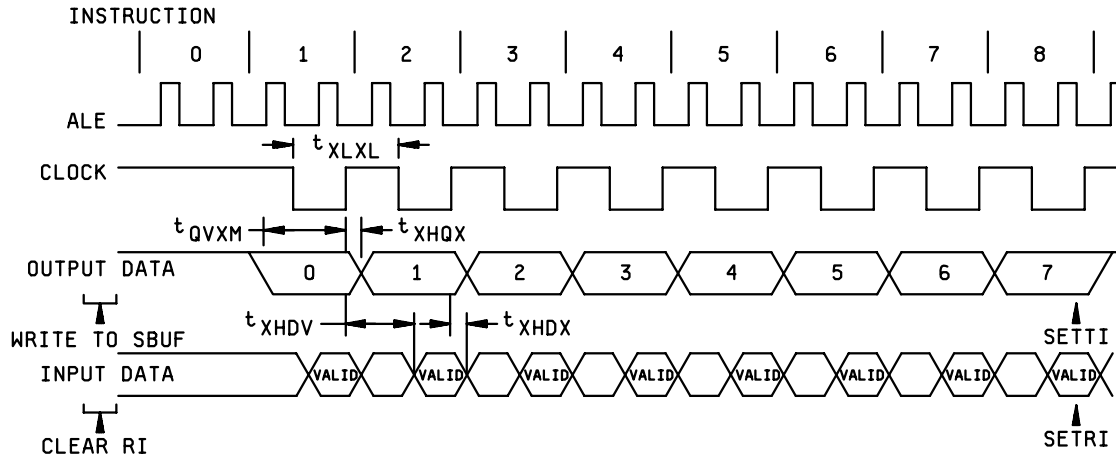
FIGURE 3. Timing waveforms – Continued.

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EXTERNAL CLOCK WAVEFORMS



SHIFT REGISTER TIMING WAVEFORMS



SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{XLXL}	Serial Port Clock Time	$12t_{CLCL}$		μs
t_{QVXH}	Output Data Setup to Clock Rising Edge	$10t_{CLCL}-133$		ns
t_{XHGX}	Output Data Hold After Clock Rising Edge	$2t_{CLCL}-117$		ns
t_{XHDX}	Input Data Hold After Clock Rising Edge	0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid	--	$10t_{LCL}-133$	ns

FIGURE 3. Timing waveforms – Continued.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.
- c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect input or output capacitance. A minimum sample of 3 devices with zero rejects shall be required.

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TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)			
Final electrical parameters (see 4.2)	<u>1/</u> 1, 2, 3, 4, 5, 6, 7, 8A, 8B, 9, 10, 11	<u>1/</u> 1, 2, 3, 4, 5, 6, 7, 8A, 8B, 9, 10, 11	<u>2/</u> 1, 2, 3, 4, 5, 6, 7, 8A, 8B, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8A, 8B, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 4, 7, 9	1, 4, 7, 9	1, 2, 3, 4, 5, 6, 7, 8A, 8B, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 4, 7, 9	1, 4, 7, 9	1, 4, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 4, 7, 9	1, 4, 7, 9	1, 4, 7, 9

1/ PDA applies to subgroup 1.

2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
- b. $T_A = +125^\circ\text{C}$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

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4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and as follows:

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Pin descriptions.

Port 0 - Port 0 is an 8-bit open drain bi-directional I/O port. Port 0 pins that have 1's written to them float and in that state can be used as high impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1's. External pull-ups are required during program verification. Port 0 can sink eight LS TTL inputs.

Port 0 also outputs the code bytes during program verification in the device.

Port 1 - Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. Port 1 pins that have 1's written to them are pulled high by the internal pull-ups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current because of the internal pull-ups.

Port 1 also receives the low order address byte during program verification. It can drive CMOS inputs without external pull-ups. Also in this device Port 1 can sink/source three LS TTL inputs.

Two inputs of Port 1 are also used for Timer/Counter 2:

- P1.0 (T2): External clock inputs.
- P1.1 (T2EX): Trigger input to be reloaded or captured causing Timer/Counter 2 to interrupt.

Port 2 - Port2 is an 8-bit bi-directional I/O port with internal pull-ups. Port 2 pins that have 1's written to them are pulled high by the internal pull-ups and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses. In this application, it uses strong internal pull-ups when emitting 1's. During access to external Data Memory that use 8-bit addresses, Port 2 emits the contents of the P2 Special Function Register.

Port 2 can sink/source three LS TTL inputs. It can drive CMOS inputs with external pull-ups. And in this device Port 2 also receives the high-order address bits and control signals during program verification.

Port 3 - Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. Port 3 pins that have 1's written to them are pulled high by the internal pull-ups and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current because of the pull-ups. It also serves the functions of various special features of the MCS-51 Families listed below.

PORT PIN	ALTERNATE FUNCTION
P3.0	RXD (Serial Input Port)
P3.1	TXD (Serial Output Port)
P3.2	$\overline{\text{INT0}}$ (External Interrupt 0)
P3.3	$\overline{\text{INT1}}$ (External Interrupt 1)
P3.4	T0 (Timer 0 External Input)
P3.5	T1 (Timer 1 External Input)
P3.6	$\overline{\text{WR}}$ (External Data Memory Write Strobe)
P3.7	$\overline{\text{RD}}$ (External Data Memory Read Strobe)

Port 3 can sink/source three LS TTL inputs. It can drive CMOS inputs without external pull-ups.

RST - A high level on this for two machine cycles while the oscillator is running, resets the device. An internal pull-down resistor permits Power-On reset using only a capacitor connected to V_{DD} . As soon as the reset is applied (V_{IN}), Ports 1, 2 and 3 are tied to "1". This operation is achieved asynchronously even if the oscillator does not startup.

ALE - Address Latch Enable output for latching the low byte of the address during accesses to external memory. ALE is activated as though for this purpose at a constant rate of 1/6 of the oscillator frequency except during an external data memory access at which time one ALE pulse is skipped. ALE can sink/source 8 LS TTL inputs. It can drive CMOS inputs without an external pull-up.

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Pin descriptions - Continued.

$\overline{\text{PSEN}}$ - Program Store Enable is the read strobe to external Program Memory. $\overline{\text{PSEN}}$ is activated twice each machine cycle during fetches from external Program Memory (however, when executing out of external Program Memory, two activations of $\overline{\text{PSEN}}$ are skipped during each access to external Data Memory). $\overline{\text{PSEN}}$ is not activated during fetches from internal Program Memory. $\overline{\text{PSEN}}$ can sink/source 8 LSTTL inputs. It can drive CMOS inputs without an external pull-up.

$\overline{\text{EA}}$ - When $\overline{\text{EA}}$ is held high, the CPU executes out of internal Program Memory (unless the Program Counter exceeds 3FFFH).
When $\overline{\text{EA}}$ is held low, the CPU executes only out of external Program Memory. $\overline{\text{EA}}$ must not be floated.

XTAL1 - Input to the inverting amplifier that forms the oscillator. Receives the external oscillator signal when an external oscillator is used.

XTAL2 - Output of the inverting amplifier that forms the oscillator and input of the internal clock generator. This pin should be floated when an external oscillator is used.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 07-11-19

Approved sources of supply for SMD 5962-00518 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at <http://www.dscclia.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-0051801QQC	F7400	MC-80C32E-30MQ
5962-0051801VQC	F7400	SC-80C32E-30SV
5962-0051801QXC	F7400	MJ-80C32E-30MQ
5962-0051801VXC	F7400	SJ-80C32E-30SV

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

F7400

Vendor name
and address

Atmel Nantes
La Chantrerie BP 70602
44306 Nantes Cedex 3, France

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