REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
C	Change maximum Input voltage (VI) in section 1.3 from 3.75 V to 4.1 V max, change Maximum junction temperature (TJ) from 125ºC to 135ºC, and update footnote 10/. Make changes to Table I; clarifications for 5 V tolerance, standby currents, and I/O related changes. Edit notes 2, 3, and 8 on Figure 2; and add note 10. ksr	09-08-17	Charles F. Saffle
D	Updated devices for class V. Updated footnote information for 1.2.4. Updated 2.2. Deleted "and Table IIA note 8/ herein" from Table I footnote 1/. Added footnotes 11/ and 12/. Deleted "Qualification inspection for all devices (01 to 08) complies with class Q level requirements only." from 4.3. Updated 4.4.2.1c. Updated Table IIA and footnotes. Updated Table IIB. Removed vendor website URL from 6.7. Updated boilerplate to current requirements. lhl	12-03-05	Charles F. Saffle
E	Removed all references to Class M to update to current boilerplate requirements. Added devices 09-16, added footnotes 8 - 12 in section 1 and updated footnotes to clarify Class Q with extra screening. Added device types 09 - 16 and updated footnote 4 in Table I. Edited Case U terminals to match datasheet and specified device types 01 - 08 and 09 – 16 labeling in FIGURE 2. Added device types 09 - 16 and Seal Fine Gross Leak Test and Lot specific group B with RGA testing to 4.2.2f. Removed programming software brand name from 4.6. lhl	12-11-09	Charles F. Saffle

REV	E																			
SHEET	55																			
REV	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E
SHEET	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54
REV	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS	REV	E	E	E	E	E	E	E	E	E	E	E	E	E
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Rajesh Pithadia

APPROVED BY
Raymond Monnin

DRAWING APPROVAL DATE
06-04-05

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, FIELD PROGRAMMABLE GATE ARRAY, 2,000,000 GATES, MONOLITHIC SILICON

REVISION LEVEL	SIZE	CAGE CODE	
E	A	67268	5962-04221

SHEET 1 OF 55

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:

5962	-	04221	01	Q	X	C
Federal stock class designator	RHA designator (see 1.2.1)		Device type (see 1.2.2)	Device class designator (see 1.2.3)	Case outline (see 1.2.4)	Lead finish (see 1.2.5)
\		/				
Drawing number						

1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	
01	RTAX2000S	2,000,000 gate field programmable gate array	
02	RTAX2000S-1	2,000,000 gate field programmable gate array	1/
03	RTAX2000S	2,000,000 gate field programmable gate array	2/
04	RTAX2000S-1	2,000,000 gate field programmable gate array	1/ 3/
05	RTAX2000SL	2,000,000 gate field programmable gate array	4/
06	RTAX2000SL-1	2,000,000 gate field programmable gate array	1/ 4/
07	RTAX2000SL	2,000,000 gate field programmable gate array	4/ 5/
08	RTAX2000SL-1	2,000,000 gate field programmable gate array	1/ 4/ 6/
09	RTAX2000D	2,000,000 gate field programmable gate array	7/
10	RTAX2000D-1	2,000,000 gate field programmable gate array	1/ 7/
11	RTAX2000D	2,000,000 gate field programmable gate array	7/, 9/
12	RTAX2000D-1	2,000,000 gate field programmable gate array	1/, 7/, 10/
13	RTAX2000DL	2,000,000 gate field programmable gate array	7/, 8/
14	RTAX2000DL-1	2,000,000 gate field programmable gate array	1/, 7/, 8/
15	RTAX2000DL	2,000,000 gate field programmable gate array	7/, 8/, 11/
16	RTAX2000DL-1	2,000,000 gate field programmable gate array	1/, 7/, 8/, 12/

Note: These devices are specified at junction operating temperature and not at case operating temperature.

1/ Timing performance of the RTAX2000S-1, RTAX2000SL-1, RTAX2000D-1 and RTAX2000DL-1 devices shall be approximately 15% faster than the RTAX2000S, RTAX2000SL. RTAX2000D and RTAX2000DL devices respectively (End users may select the appropriate device speed grade through timing calculations based on timing simulation of specific designs with manufacturer's Libero/Designer software, see 6.7 herein).
2/ Device type 03, only offered as a Class Q device, is a Class Q device type 01 with additional testing (see 4.2.2.f).
3/ Device type 04, only offered as a Class Q device, is a Class Q device type 02 with additional testing (see 4.2.2.f).
4/ Silicon used for devices 01-08 is the same silicon, at 125°C final electrical test, device type 05 to 08 are screened to a lower I_{CCA} limit (see Table I herein).
5/ Device type 07, only offered as a Class Q device, is a Class Q device type 05 with additional testing (see 4.2.2.f).
6/ Device type 08, only offered as a Class Q device, is a Class Q device type 06 with additional testing (see 4.2.2.f).
7/ Silicon used for device types 09 – 16 has identical manufacturing process as device types 01 – 08 but features enhanced DSP functionality with the addition of embedded multiply accumulate blocks.
8/ Silicon used for all devices 09 – 16 is the same silicon, at 125°C final electrical test, device type 13 to 16 are screened to a lower I_{CCA} limit (see Table I herein).
9/ Device type 11, only offered as a Class Q device, is a Class Q device type 09 with additional testing (see 4.2.2.f).
10/ Device type 12, only offered as a Class Q device, is a Class Q device type 10 with additional testing (see 4.2.2.f).
11/ Device type 15, only offered as a Class Q device, is a Class Q device type 13 with additional testing (see 4.2.2.f).
12/ Device type 16, only offered as a Class Q device, is a Class Q device type 14 with additional testing (see 4.2.2.f).

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	352	Ceramic Quad Flat Pack 13/
Y	See figure 1	624	Ceramic Land Grid Array (LGA)
Z	See figure 1	624	Ceramic Column Grid Array (CGA) 14/
U	See figure 1	256	Ceramic Quad Flat Pack
M	See figure 1	1152	Ceramic Land Grid Array (LGA)
T	See figure 1	1152	Ceramic Column Grid Array (CGA) 14/
N	See figure 1	624	Ceramic Column Grid Array (CGA) 14/

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings (for 1.5V/1.8V/2.5V/3.3V operating conditions). 15/

DC core supply voltage (V_{CCA}) ..... -0.3 to +1.7 V
DC I/O supply voltage (V_{CCI}) ..... -0.3 to +3.75 V
DC supply voltage for differential I/Os (V_{CCDA}) ..... -0.3 to +3.75 V
DC I/O reference voltage (V_{REF}) ..... -0.3 to +3.75 V
DC external pump supply voltage (V_{PUMP}) ..... -0.3 to +3.75 V
Input voltage (V_I) ..... -0.5 to +4.1 V 16/
Output voltage (V_O) ..... -0.5 to +3.75 V
Storage temperature range (V_{STG}) ..... -65°C to +150°C
Lead temperature (soldering, 10 seconds) X and U ..... 300°C
Y, Z, T, M, and N ..... 245°C
Maximum junction temperature (T_J) ..... 135°C 17/

13/ For device type 09 – 16 in case outline X the terminal connections are different than device type 1 - 8
14/ Case outlines T and N have a different solder composition than Z (see Figure 1 for details).
15/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
16/ Overshoot/Undershoot limits: For AC signals, the input signal may undershoot during transitions to -1.0 V for no longer than 10% of the period or 11 ns whichever is smaller. Current during the transition must not exceed 95 mA. For AC signals, the input signal may overshoot during transitions to V_{CCI} + 1.0 V for no longer than 10% of the period or 11 ns whichever is smaller. Current during the transition must not exceed 95 mA. Note: This specification does not apply to the PCI standard. The PCI I/Os of this device are compliant to the PCI standard including the PCI overshoot/undershoot specifications.
17/ Maximum junction temperature shall not be exceeded except for allowable short durations during burn-in screening conditions in accordance with method 5004 of MIL-STD-883. T_J=135°C applies with wafer lot numbers starting with D2xxxx. For older wafer lot numbers starting with D1xxxx , the T_J=125°C still applies.

1.3 Absolute maximum ratings (for 1.5V/1.8V/2.5V/3.3V operating conditions) – Continued. 15/

Thermal resistance, junction-to-case (θ_{JC}):
- Case outline X ..... 0.2° C/W 18/ 21/
- Case outlines Y, Z, and N ..... 4.3° C/W 19/ 21/
- Case outline U ..... 0.25°C/W 18/ 21/
- Case outlines M and T ..... 2.0° C/W 19/ 21/

Thermal resistance, junction-to-board (θ_{JB})
- Case outlines Z and N ..... 3.5°C/W 20/ 21/
- Case outline T ..... 2.6°C/W 20/ 21/

AC core supply transient voltage (V_{CCA}) ..... -0.3 to +1.8 V 22/

1.4 Recommended operating conditions.

- 1.5V core supply voltage ..... 1.425 to 1.575 V dc
- 1.5V I/O supply voltage ..... 1.425 to 1.575 V dc
- 1.8V I/O supply voltage ..... 1.71 to 1.89 V dc
- 2.5V I/O supply voltage ..... 2.375 to 2.625 V dc
- 3.3V I/O supply voltage ..... 3.0 to 3.6 V dc
- 2.5V V_{CCDA} I/O supply voltage (no differential I/O used) ..... 2.375 to 2.625 V dc
- 3.3V V_{CCDA} I/O supply voltage (differential or voltage referenced I/O used) ..... 3.0 to 3.6 V dc
- 3.3V V_{PUMP} supply voltage range ..... 3.0 to 3.6 V dc
- Junction operating temperature range (T_J) ..... -55°C to +125°C

1.5 Power-Up/Down Sequence. All device I/Os are tri-stated during power-up until normal device operating conditions are reached, which is when I/Os enter user mode. V_{CCA}, V_{CCI}, and V_{CCDA} can be powered up or powered down in any sequence. All device I/Os are hot-swap compliant with cold-sparing support (except PCI).

1.5.1 R-cells and I/O Registers. On a chip-wide basis at power-up, all R-cells and I/O Registers are either cleared or preset by driving the global clear (GCLR) and global preset (GPSET) inputs (see Figure 3). Default setting is to clear all registers (GCLR = 0 and GPSET =1) at device power-up.

1.6 Device Logic Configuration.

1.6.1 Core array logics include two types of logic modules: the register cell (R-cell) and the combinatorial cell (C-cell). C-cell contains carry logic for efficient arithmetic functions. R-cell appears as a single D-type flip-flop to user, but is implemented in silicon with triple module redundancy (TMR) to improve SEU performance. Each TMR R-cell consist of three master-slave latch pairs, each with asynchronous self-correcting feedback paths. Output of the TMR R-cell is the result of the majority voting of the outputs of the three flip flops in the TMR R-cells. Logic modules are grouped as SuperCluster, each SuperCluster has two Clusters, and each Cluster includes two C-cells, one R-cell, two transmit (TX) and two receive (RX) routing buffers. Each SuperCluster also includes an independent buffer module. On the chip level, SuperClusters are organized into core tiles, which are arrayed to build up the full chip. There are 16 core tiles in this device and each tile has 336 SuperClusters, resulting a total of 10,752 R-cells and 21,504 C-cells in the device.

18/ θ_{JC} for case outlines X and U refers to the thermal resistance between the junction and the bottom of the package.

19/ θ_{JC} for case outlines Y, Z, M, T, and N refers to the thermal resistance between the junction and the top of the package (surface of the metal lid).

20/ θ_{JB} for case outlines Z, T, and N refers to the thermal resistance between the junction and the tips of the solder columns (where the device is attached to the circuit board).

21/ All thermal resistance data are obtained through simulation with computational fluid dynamic software. For case outlines Z, T, and N, the θ_{JB} is simulated with 4L/2P SMT board per JESD 51.

22/ AC transient V_{CCA} limit is for radiation induced transients less than 10µs duration, and not intended for repetitive use. Core voltage spikes from a single event transient will not negatively affect the reliability of the device if, for this non-repetitive event, the transient does not exceed 1.8 V at any time, and the total time that the transient exceeds 1.575 V does not exceed 10 µs in duration.

1.6.2 Clock Resources are available with two types of global clock networks throughout the chip. There are four dedicated hardwired clock input pins (HCLKA/B/C/D) that will directly drive all the sequential modules (R-cells, I/O registers, embedded RAM/FIFO). There are also four global clock input pins (CLKE/F/G/H) for routed clock distribution networks that are buffered prior to clocking the R-cells; the routed clocks can also be programmed to drive S0, S1, PSET, and CLR of a register, or as the inputs of any C-cell. Input levels for all clocks are compatible with all supported I/O standards (there is a P/N pin pair to support differential I/O standards). All clock networks have been hardened to improve SEU performance.

1.6.3 Embedded RAM is available as a global resource. There are four 4,608-bit RAM blocks in each tile, with a total of 294,912 bits in the device. Each 4,608-bit RAM block can be organized as 128x36, 256x18, 512x9, 1,024x4, 2,048x2, or 4,096 x1 (Depth x Word in bits), and are cascadable to create larger memory sizes. Each RAM block has independent read and write ports, which enables simultaneous read and write operations; it also contains its own embedded FIFO controller, allowing the RAM blocks to be configured as either RAM or FIFO. SRAM structures are susceptible to radiation upsets, to achieve high level SEU performance; manufacturer has provided an IP core to enhance the SEU tolerance of the embedded RAM blocks by mitigating upsets with Error Detection and Correction (EDAC) and background memory-refresher (or scrubber). Registers in the FIFO controller are not hardened for radiation, so when high SEU tolerance is required, the FIFO control unit should be implemented with core logic. Note: Simultaneous read and write operations to the same address is not supported.

1.6.4 Multi-Standard I/Os are available on all I/O pins. Below table shows all supported I/O standards.

I/O Standard	Input/Output Supply Voltage (V_{CCI})	Input Reference Voltage (V_{REF})	Board Termination Voltage (V_{TT})
LVTTL	3.3	N/A	N/A
LVCMOS 2.5V	2.5	N/A	N/A
LVCMOS 1.8V	1.8	N/A	N/A
LVCMOS 1.5V	1.5	N/A	N/A
3.3V PCI	3.3	N/A	N/A
GTL+ 3.3V	3.3	1.0	1.2
HSTL Class I	1.5	0.75	0.75
SSTL3 Class I and II	3.3	1.5	1.5
SSTL2 Class I and II	2.5	1.25	1.25
LVDS	2.5	N/A	N/A
LVPECL	3.3	N/A	N/A

Each I/O provides programmable slew rates, drive strength, and weak pull-up and pull-down circuits (in the order of 10kΩ), it also includes three registers (input (InReg), output (OutReg), and enable (EnReg)). I/Os are organized into eight banks (0-7) with two banks per device side. Each I/O bank has a common V_{CCI} and a common reference-voltage bus. For each I/O bank, multiple I/O standards may be selected, however, all I/O standards used in the same I/O bank shall have the same V_{CCI} value and the same V_{REF} value (when required). V_{REF} pin is not pre-defined; any user I/O in the bank can be selected to be a V_{REF}.

1.6.5 Routing Resource provides hierarchical routing structure that ties the logic modules, the embedded memory block, and the I/O modules together. User designs can be implemented with manufacturer's Designer software (see 6.7 herein), which includes a Timer that supports timing-driven place-and-route; plus SmartPower for power estimation; PinEditor and I/O Attribute Editor for I/O assignments and I/O attributes; Netlist Viewer and ChipPlanner for design implementation. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment (see 6.7 herein).

1.6.6 Calculation for Junction Temperature. The temperature variable in the manufacturer's Designer software refers to the junction temperature, not the ambient, case, or board temperature. The operating temperature at case (T_C) can be calculated with $\theta_{JC} = (T_J - T_C) \div P$; and the operating temperature at board interface (T_B) for case outline Z can be calculated with $\theta_{JB} = (T_J - T_B) \div P$. P is the device power consumption, which differs among user designs. Power usage can be determined by logic cell utilization; clock usage and frequency; input cell utilization and frequency; output cell utilization, V_{CCI} level and output frequency; and static power consumption. The manufacturer's software tool will assist users on power estimation.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD 51 - High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages.
JESD 78 - IC Latch-Up Test.

(Copies of this document are available online at www.jedec.org/ or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240-S, Arlington, VA 22201).

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 - Test Access Port and Boundary-Scan Architecture

(Applications for copies should be addressed to the IEEE, 1828 L Street, N.W., Suite 1202, Washington, D.C. 20036-5104.) stds-info@ieee.org

IPC - ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES

IPC/ECA J-STD-002 - Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires

(Applications for copies of IPC publications should be addressed to: IPC – Association Connecting Electronics Industries, 3000 Lakeside Drive, 309 S, Bannockburn, IL 60015; http://www.ipc.org.)

TELECOMMUNICATIONS INDUSTRY ASSOCIATION 2001

TIA/EIA-644 - Electrical Characteristics of Low-Voltage Differential Signaling (LVDS) Interface Circuits

(Applications for copies of TIA publications should be addressed to: Telecommunications Industry Association 2001, Standards and Technology Department, 2500 Wilson Boulevard, Arlington, VA 22201; http://www.tiaonline.org)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.1.1 Case outlines X, Y, Z, U, M, T, and N assembly. Case outlines X, Y, Z, U, M, T, and N are assembled with die attachment (Silver filled Cyanate Ester material), wire bond (25.4μm (1.0 mil) aluminum wire), and hermetic sealed with AuSn lid preformed.

3.2.1.2 Bonding pads. Devices built with all case outlines have two rows of bonding pads on the silicon side with 95 micron bond pad pitch and are bonded on multi-tiered packages. Wire bonds from adjacent bond pads on the silicon may be seen on top view as crossing with each other; however, they are connected to different tiers on the package and have different wire loop heights. In any case, all wires still maintain a minimum clearance of two wire diameters in any direction from the adjacent wires.

3.2.1.3 Solderability test for case outlines Y and M. Solderability test for case outlines Y and M (LGA) is based on IPC/EIA J-STD-002, Test S (Surface Mount Process Simulation Test) with water soluble flux. This is the test method to simulate the solder column attachment process. Test B (dip and look) with steam preconditioning per Method 2003 of MIL-STD-883 does not provide any guidance for LGA devices.

3.2.1.4 Solderability test for case outlines Z, T, and N. Solderability test for case outlines Z, T, and N (CGA) package has been verified during solder column attachment process. Method 2003 of MIL-STD-883 solderability test does not provide any guidance for CGA devices. Devices on this SMD in a CGA package have high lead content (case outline Z has 90% lead content and case outlines T and N has 80% lead content vs. typical eutectic solder's 37% lead content, see Figure 1 for details).

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s).

3.2.3.1 Unprogrammed devices. The truth table or test vectors for unprogrammed devices for contracts involving no altered item drawing is not part of this drawing. When required in screening (see 4.2 herein) or qualification conformance inspection, groups A, B, C, D, or E (see 4.4 herein), the devices shall be programmed by the manufacturer prior to test. A minimum of 95 percent of the total number of logic modules shall be utilized.

3.2.3.2 Programmed devices. Prior to submitting altered item drawing the truth table or test vectors for programmed devices should be agreed upon by acquiring activity and the manufacturer.

3.2.4 Logic blocks diagrams. The logic block diagrams and switching test circuit diagrams are specified in figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full junction operating temperature (T_J) range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations; two processing options are provided for selection in the contract.

3.8.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 4.4.1 and table IIA.

3.8.2 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery. Manufacturer shall verify design checksum after programming.

TABLE I. Electrical performance characteristics. 1/ 2/

Test	Symbol	Conditions 3/ $1.425V \le V_{CCA} \le 1.575V$ $-55°C \le T_J \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
For All I/O Standards							
Standby supply current for core power supply	I_{CCA}	$T_J = 25^oC$	1	01 - 04 09 - 12		50	mA
				05 - 08 13 - 16 4/		30	
		$T_J = 125^oC, -55^oC$	2,3	01 - 04 09 - 12		500	mA
				05 - 08 13 - 16		150	
Standby supply current for I/O power supply	I_{CCI}	$T_J = 25^oC$	1	All		10	mA
		$T_J = 125^oC, -55^oC$	2,3	All		35	mA
Standby supply current for V_{CCDA} power supply	I_{CCDA}	$T_J = 25^oC$	1	All		7	mA
		$T_J = 125^oC, -55^oC$	2,3	All		10	mA
Input leakage current … low	I_{IL}	V_{IN} = GND, $T_J = 25^oC$	1	All		1	µA
		V_{IN} = GND, $T_J = 125^oC, -55^oC$	2,3	All		5	µA
Input leakage current … high	I_{IH}	$V_{IN} = V_{CCI}$, $T_J = 25^oC$	1	All		1	µA
		$V_{IN} = V_{CCI}$, $T_J = 125^oC, -55^oC$	2,3	All		5	µA
Three-state output current leakage	I_{OZ}	$V_{IN} = V_{CCI}$, $T_J = 25^oC$	1	All		1	µA
		$V_{IN} = V_{CCI}$, $T_J = 125^oC, -55^oC$	2,3	All		5	µA
Standby supply current for $V_{CCDIFFA}$ differential pairs	$I_{CCDIFFA}$	$V_{IN} = V_{CCI}$, $T_J = 25^oC$	1	All		3.13	mA
		$V_{IN} = V_{CCI}$, $T_J = 125^oC, -55^oC$	2,3	All		3.7	mA
Functional tests	FT 5/	See 4.4.1e	7,8A,8B	All			
I/O Input Capacitance	C_{IN} & C_{OUT} & C_{INCLK}	See 4.4.1c f = 100 kHz, V_{IN} = 0 V	4	All		15	pF
Binning Circuit Delay 6/	BIN_ FAST		9, 10, 11	All		6.6	µs
	BIN_ SLOW		9, 10, 11	All		8.5	µs

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/ 2/

Test	Symbol	Conditions 3/ $1.425V \le V_{CCA} \le 1.575V$ $-55°C \le T_J \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
3.3V LVTTL							
3.3V I/O supply	V_{CCI}		1,2,3	All	3.0	3.6	V
Low level input voltage	V_{IL}		1,2,3	All	-0.3	0.8	V
High level input voltage	V_{IH}		1,2,3	All	2.0	3.6	V
Low level output voltage	V_{OL}	I_{OL} = 24 mA	1,2,3	All		0.4	V
High level output voltage	V_{OH}	I_{OH} = 24 mA	1,2,3	All	2.4		V
2.5V LVCMOS							
2.5V I/O supply	V_{CCI}		1,2,3	All	2.375	2.625	V
Low level input voltage	V_{IL}		1,2,3	All	-0.3	0.7	V
High level input voltage	V_{IH}		1,2,3	All	1.7	3.6	V
Low level output voltage	V_{OL}	I_{OL} = 12 mA	1,2,3	All		0.4	V
High level output voltage	V_{OH}	I_{OH} = -12 mA	1,2,3	All	2.0		V
1.8V LVCMOS							
1.8V I/O supply	V_{CCI}		1,2,3	All	1.71	1.89	V
Low level input voltage	V_{IL}		1,2,3	All	-0.3	0.2 V_{CCI}	V
High level input voltage	V_{IH}		1,2,3	All	0.7 V_{CCI}	2.1	V
Low level output voltage	V_{OL}	I_{OL} = 8 mA	1,2,3	All		0.2	V
High level output voltage	V_{OH}	I_{OH} = -8 mA	1,2,3	All	V_{CCI} - 0.2		V
1.5V LVCMOS							
1.5V I/O supply	V_{CCI}		1,2,3	All	1.425	1.575	V
Low level input voltage	V_{IL}		1,2,3	All	-0.5	0.35 V_{CCI}	V
High level input voltage	V_{IH}		1,2,3	All	0.65 V_{CCI}	1.95	V
Low level output voltage	V_{OL}	I_{OL} = 8 mA	1,2,3	All		0.4	V
High level output voltage	V_{OH}	I_{OH} = -8 mA	1,2,3	All	V_{CCI} - 0.4		V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/ 2/

Test	Symbol	Conditions 3/ $1.425V \le V_{CCA} \le 1.575V$ $-55°C \le T_J \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
3.3V PCI 7/ 8/							
3.3V I/O supply	V_{CCI}		1,2,3	All	3.0	3.6	V
Low level input voltage	V_{IL}		1,2,3	All	-0.5	0.3 V_{CCI}	V
High level input voltage	V_{IH}		1,2,3	All	0.5 V_{CCI}	V_{CCI} + 0.5	V
Low level output voltage	V_{OL}		1,2,3	All	Per PCI specification 7/		V
High level output voltage	V_{OH}		1,2,3	All	Per PCI specification 7/		V
3.3V GTL+ 9/							
3.3V I/O supply	V_{CCI}		1,2,3	All	3.0	3.6	V
Low level input voltage	V_{IL}		1,2,3	All		V_{REF} - 0.1	V
High level input voltage	V_{IH}		1,2,3	All	V_{REF} + 0.1		V
Low level output voltage	V_{OL}	$T_J = 25°C$	1,2,3	All		0.6	V
		$T_J = 125°C$				0.7	
1.5V HSTL Class I 9/							
1.5V I/O supply	V_{CCI}		1,2,3	All	1.425	1.575	V
Low level input voltage	V_{IL}		1,2,3	All	-0.3	V_{REF} - 0.1	V
High level input voltage	V_{IH}		1,2,3	All	V_{REF} + 0.1	3.6	V
Low level output voltage	V_{OL}	I_{OL} = 8 mA	1,2,3	All		0.4	V
High level output voltage	V_{OH}	I_{OH} = -8 mA	1,2,3	All	V_{CCI} - 0.4		V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/ 2/

Test	Symbol	Conditions 3/ $1.425V \le V_{CCA} \le 1.575V$ $-55°C \le T_J \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
2.5V SSTL2 Class I 9/							
2.5V I/O supply	V_{CCI}		1,2,3	All	2.375	2.625	V
Low level input voltage	V_{IL}		1,2,3	All	-0.3	V_{REF} - 0.2	V
High level input voltage	V_{IH}		1,2,3	All	V_{REF} + 0.2	3.6	V
Low level output voltage	V_{OL}	I_{OL} = 7.6 mA	1,2,3	All		V_{REF} - 0.57	V
High level output voltage	V_{OH}	I_{OH} = -7.6 mA	1,2,3	All	V_{REF} +0.57		V
2.5V SSTL2 Class II 9/							
2.5V I/O supply	V_{CCI}		1,2,3	All	2.375	2.625	V
Low level input voltage	V_{IL}		1,2,3	All	-0.3	V_{REF} - 0.2	V
High level input voltage	V_{IH}		1,2,3	All	V_{REF} + 0.2	3.6	V
Low level output voltage	V_{OL}	I_{OL} = 15.2 mA	1,2,3	All		V_{REF} - 0.8	V
High level output voltage	V_{OH}	I_{OH} = -15.2 mA	1,2,3	All	V_{REF} +0.8		V
3.3V SSTL3 Class I 9/							
3.3V I/O supply	V_{CCI}		1,2,3	All	3.0	3.6	V
Low level input voltage	V_{IL}		1,2,3	All	-0.3	V_{REF} - 0.2	V
High level input voltage	V_{IH}		1,2,3	All	V_{REF} + 0.2	3.6	V
Low level output voltage	V_{OL}	I_{OL} = 8 mA	1,2,3	All		V_{REF} - 0.6	V
High level output voltage	V_{OH}	I_{OH} = -8 mA	1,2,3	All	V_{REF} +0.6		V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/ 2/

Test	Symbol	Conditions 3/ $1.425V \le V_{CCA} \le 1.575V$ $-55°C \le T_J \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
3.3V SSTL3 Class II 9/							
3.3V I/O supply	V_{CCI}		1,2,3	All	3.0	3.6	V
Low level input voltage	V_{IL}		1,2,3	All	-0.3	V_{REF} - 0.2	V
High level input voltage	V_{IH}		1,2,3	All	V_{REF} + 0.2	3.6	V
Low level output voltage	V_{OL}	I_{OL} = 16 mA	1,2,3	All		V_{REF} - 0.8	V
High level output voltage	V_{OH}	I_{OH} = -16 mA	1,2,3	All	V_{REF} +0.8		V
2.5V LVDS 9/ 10/							
2.5V I/O supply	V_{CCI}		1,2,3	All	2.375	2.625	V
Low level output voltage	V_{OL}		1,2,3	All		1.25	V
High level output voltage	V_{OH}		1,2,3	All	1.25		V
Differential output voltage	V_{ODIFF}		1,2,3	All	250	450	mV
Output common mode voltage	V_{OCM}		1,2,3	All	1.125	1.375	V
Input common mode voltage	V_{ICM} 11/		1,2,3	All	0.2	2.2	V
3.3V LVPECL 9/ 12/							
3.3V I/O supply	V_{CCI}		1,2,3	All	3.0	3.6	V
Low level input voltage	V_{IL}		1,2,3	All	0.86	2.125	V
High level input voltage	V_{IH}		1,2,3	All	1.49	2.72	V
Low level output voltage	V_{OL}		1,2,3	All	0.96	1.57	V
High level output voltage	V_{OH}		1,2,3	All	1.8	2.41	V
Differential input voltage			1,2,3	All	0.3		V

1/ AC/Timing parameters (subgroup 9, 10, 11) are not directly tested but fully characterized (see note 2/), which are published on device manufacturer's data sheet and implemented in manufacturer's software (see 6.7).

2/ Characterization data is taken at initial device introduction and repeated after any design or process changes that may affect the related parameters. Devices are first 100 percent functionally tested, then benchmark design/timing patterns are programmed into the devices and then characterized to determine the compliance of the parameters.

3/ All tests shall be performed under the worst-case condition unless otherwise specified.

4/ Devices 05 - 08 and 13 - 16 are selected at final electrical test at 125ºC and are guaranteed to meet the I_{CCA} limit at 25ºC.

5/ Devices are functionally tested using a serial scan test method. Data is shifted into the TDI pin and the TCK pin is used as a clock. The data is used to drive the inputs of the internal logic and I/O modules, allowing a complete functional test to be performed. The outputs of the module can be read by shifting out the output response or by monitoring the TDO pins.

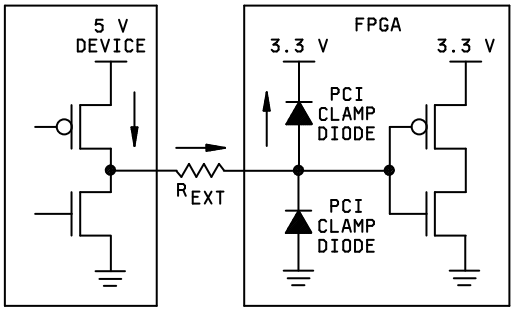
6/ Binning circuit is the only fixed circuit in the device which is capable of measuring AC delays. See Table IIB, note 4/ and 5/ for more detailed description of the binning circuit.

7/ This device is electrically compliant with the PCI Local Bus Specification Rev. 2.1, it supports both 33 MHz and 66 MHz PCI bus applications.

8/ 5V direct input tolerance is allowed only for 3.3 V PCI and for 3.3V LVTTL with clamp diode enabled. Clamp diode is only enabled by default for 3.3V PCI standard; for 3.3V LVTTL, it can be enabled through checking the settings in manufacturer's Designer software. Hot-insertion and cold-sparing are not supported when clamp diode is enabled.

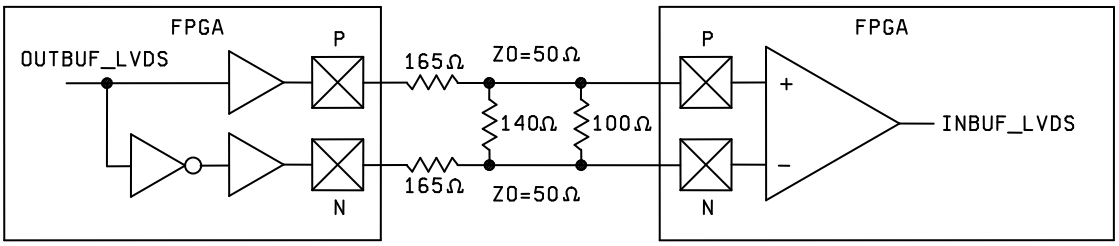
Example: The PCI standard provides an internal clamp diode between the input pad and the V_{CCI} pad (see graph below) so the voltage at the input pin is clamped below the absolute maximum input voltage of 4.1 V (see 1.3 above). An example of the input pad voltage level is shown as: $V_{INPUT} = V_{CCI} + V_{DIODE} = 3.3\ V + 0.7\ V = 4.0\ V$.

The internal clamp diode is only enabled while the device is powered on, so the voltage at the input will not be clamped if the V_{CCI} is powered off. An external series resistor (~100 Ω) is required between the input pin and the 5 V signal source to limit the current to less than 20 mA. The 100 Ω resistor is chosen to meet the maximum I/O input rise and fall time (Tr/Tf) requirement of 50 ns. 5 V tolerance is not allowable for V_{CCI} greater than 3.3 V or for input signals greater than 5.0 V.



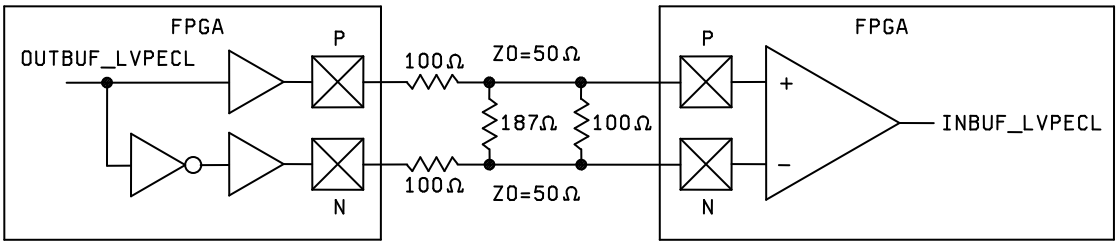
9/ Refer to manufacturer's datasheet for additional requirement for voltage-referenced I/O and differential I/O standards

10/ Low-Voltage Differential Signal (LVDS, TIA/EIA-644) is a high-speed differential I/O standard. An external-resistor network (three resistors) is needed to reduce the voltage swing to about 350mV. It also requires an external resistor termination. Therefore, four external resistors are required, three for the driver and one for the receiver (see the diagram below).

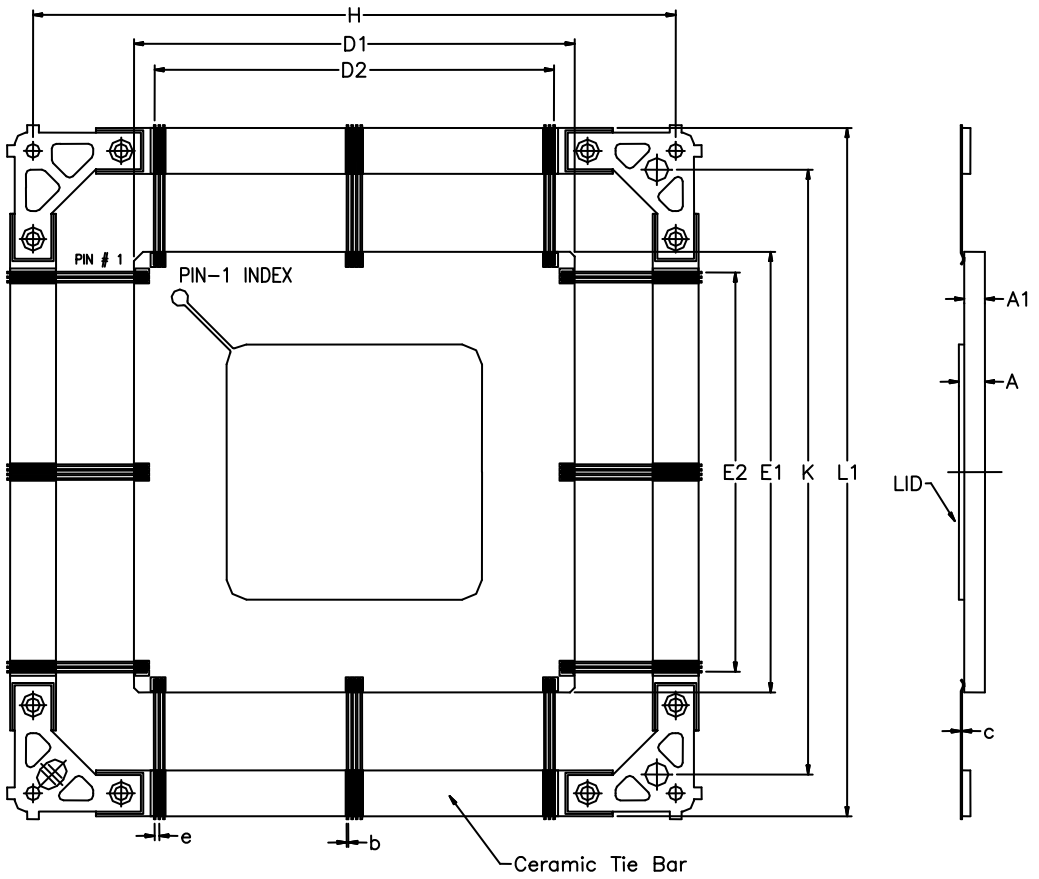


11/ Differential input voltage = ±350mV (LVDS).

12/ Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is a differential I/O standard. It requires four external resistors; three for the driver and one for the receiver (see the diagram below). The voltage swing between these two signal lines is approximately 850 mV. It should be noted that the V_{OH} levels are 200 mV below the standard LVPECL levels.



Case Outline X

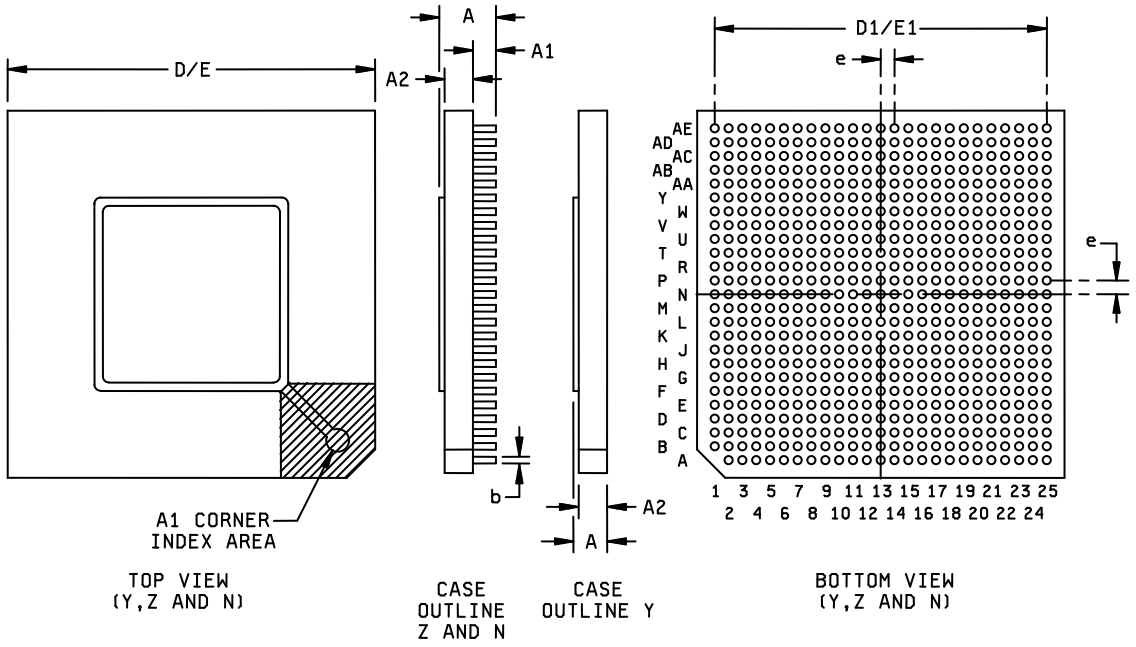


NOTES:

1. All exposed metalized areas and leads are gold plated with 2.5 μm minimum thickness over 2.0~8.9 μm thickness of nickel.
2. Lid and Seal ring area are connected to GND.
3. Die attach pad is connected to GND.
4. Tie-bar dimensions are for reference only.
5. BSC = Basic Spacing between Centers
6. Material used for package lid and leads are Fe-Ni-Co alloy.
7. Case outline X has 24.0 gm weight, which is measured after tie-bar removed.

Case Outline X (CQ352)			
Symbol	Dimension (mm)		
	Min.	Nom.	Max.
A	2.43	---	3.11
A1	2.05	2.29	2.52
b	0.15	0.2	0.25
c	0.1	0.15	0.2
D1/E1	47.75	48	48.25
D2/E2	43.5 BSC		
e	0.5 BSC		
H	70 BSC		
K	65.9 BSC		
L1	74.6	75	75.4

FIGURE 1. Case outline.



Case Outline Y (624 LGA)			
Symbol	Dimension (mm)		
	Min.	Nom.	Max.
A	2.40	---	3.12
A2	2.02	2.3	2.53
D/E	32.17	32.50	32.83
D1/E1	30.48 BSC		
e	1.27 BSC		

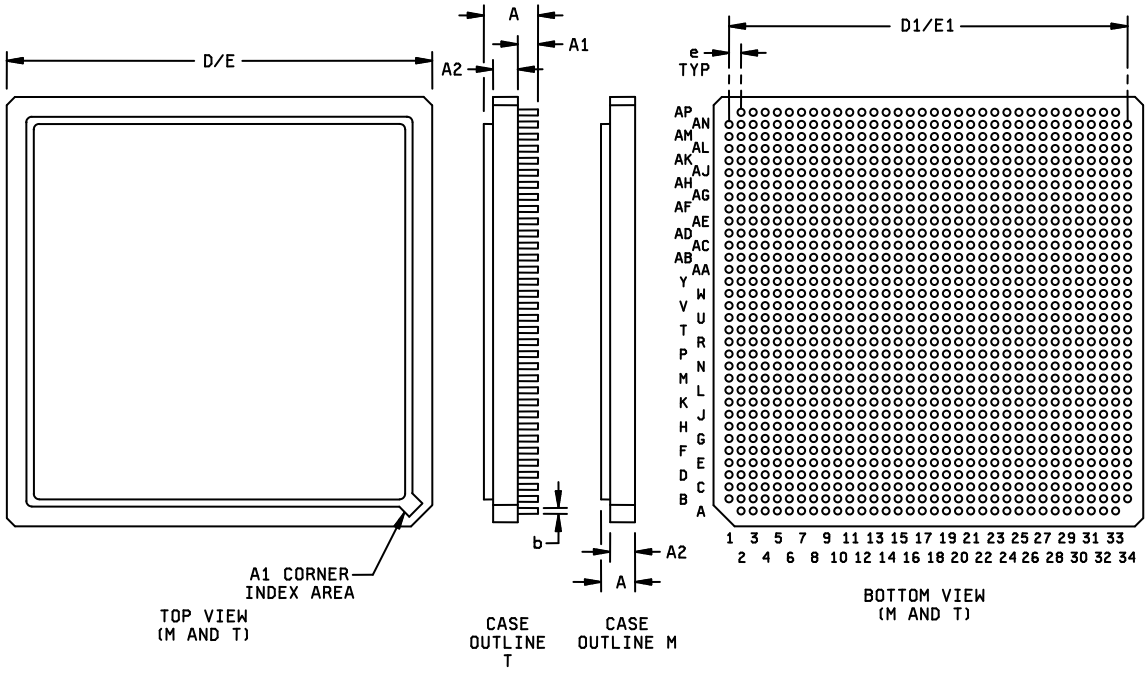
Case Outline Z and N (624 CGA)			
Symbol	Dimension (mm)		
	Min.	Nom.	Max.
A	4.41	---	5.53
A1	2.01	2.21	2.41
A2	2.02	2.3	2.53
b	0.43	0.51	0.58
D/E	32.17	32.50	32.83
D1/E1	30.48 BSC		
e	1.27 BSC		

NOTES:

1. All exposed metalized areas and leads are gold plated with 2.5 μm minimum thickness on top side and 0.03~0.10 μm on bottom side, over 2.0~8.9 μm thickness of nickel.
2. Lid and Seal ring area are connected to GND.
3. Die attach pad is connected to GND.
4. Case outline Y metal pad size is $\phi 0.86 \pm 0.05$ mm
5. Case outline Z solder column material is 10/90 Sn/Pb. Case outline N solder column material is 20/80 Sn/Pb and wrapped with copper spiral coil. A layer of eutectic solder plated over the surface of the Cu spiral.
6. BSC = Basic Spacing between Centers
7. Material used for package lid is Fe-Ni-Co alloy
8. Case outline Y has 11.2 gm of weight, and case outline Z and N have 14.7 gm of weight

FIGURE 1. Case outline – Continued.

Case outlines M and T



NOTES:

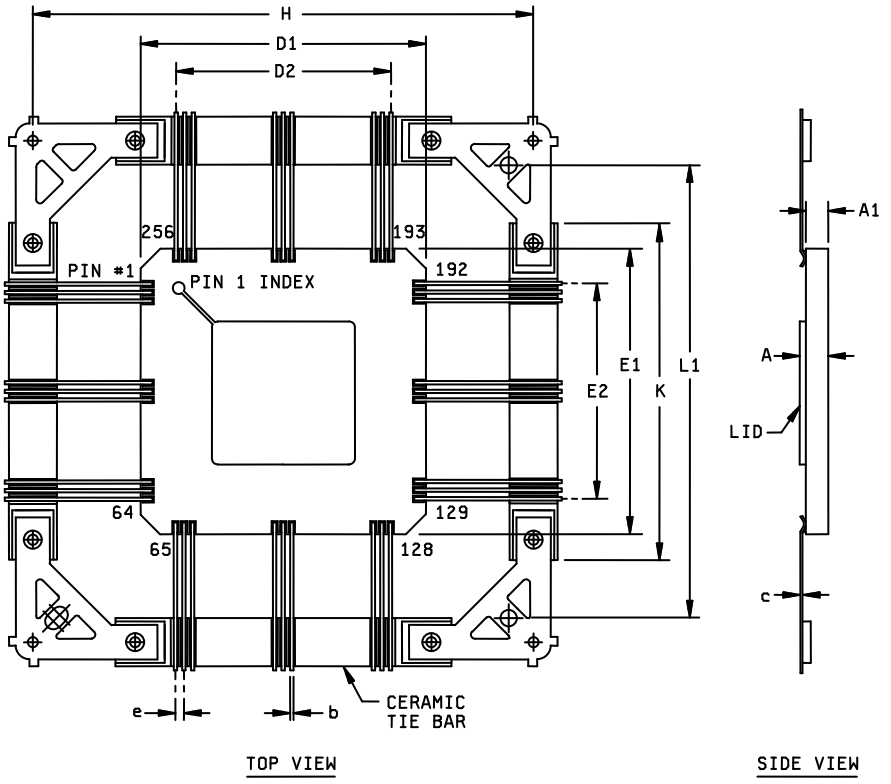
1. All exposed metalized areas and leads are gold plated with 2.5 μm minimum thickness, over 2.0~8.9 μm thickness of nickel. For case outline M, the gold on the bottom side shall be removed prior to solder column attachment.
2. Lid and Seal ring area are connected to GND.
3. Die attach pad is connected to GND.
4. Case outline M metal pad size is $\phi 0.86 \pm 0.05$ mm
5. Case outline T solder column material is 20/80 Sn/Pb and wrapped with copper spiral coil. A layer of eutectic solder plated over the surface of the Cu spiral.
6. BSC = Basic Spacing between Centers
7. Material used for package lid and leads are Fe-Ni-Co alloy.
8. Case outline M has a weight of 16.0 gm, and case outline T has a weight of 20.6 gm.

Case Outline M (1152 LGA)			
Symbol	Dimension (mm)		
	Min.	Nom.	Max.
A	2.87		3.64
A2	2.49	2.77	3.05
D/E	34.65	35	35.35
D1/E1	33.00 BSC		
e	1.00 BSC		

Case Outline T (1152 CGA)			
Symbol	Dimension (mm)		
	Min.	Nom.	Max.
A	4.88		6.05
A1	2.01	2.21	2.41
A2	2.49	2.77	3.05
b	0.43	0.51	0.58
D/E	34.65	35	35.35
D1/E1	33.00 BSC		
e	1.00 BSC		

FIGURE 1. Case outline – Continued.

Case outline U



NOTES:

1. All exposed metalized areas and leads are gold plated with 2.5 μm minimum thickness over 2.0~8.9 μm thickness of nickel.
2. Lid and Seal ring area are connected to GND.
3. Die attach pad is connected to GND.
4. Tie-bar dimensions are for reference only.
5. BSC = Basic Spacing between Centers
6. Material used for package lid and leads are Fe-Ni-Co alloy.
7. Case outline U has 15 gm weight, which is measured after tie-bar removed.

Case Outline U (CQ256)			
Symbol	Dimension (mm)		
	Min.	Nom.	Max.
A	2.43	---	3.11
A1	2.05	2.29	2.52
b	0.15	0.2	0.25
c	0.1	0.15	0.2
D1/E1	35.64	36	36.64
D2/E2	31.5 BSC		
e	0.5 BSC		
H	70 BSC		
K	65.9 BSC		
L1	74.6	75	75.4

FIGURE 1. Case outline – Continued.

Case X (device types 01 – 08).

Device Types	01 - 08	Device Types	01 - 08	Device Types	01 - 08
Case Outline	X	Case Outline	X	Case Outline	X
Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number
Bank 0		IO74PB1F6	272	IO141PB3F13	206
IO01NB0F0	341	**Bank 2**		IO142NB3F13	207
IO01PB0F0	342	IO87NB2F8	261	IO142PB3F13	208
IO02PB0F0	343	IO87PB2F8	262	IO145NB3F13	199
IO04NB0F0	337	IO88NB2F8	255	IO145PB3F13	200
IO04PB0F0	338	IO88PB2F8	256	IO146NB3F13	201
IO05NB0F0	335	IO89NB2F8	259	IO146PB3F13	202
IO05PB0F0	336	IO89PB2F8	260	IO147NB3F13	193
IO08NB0F0	331	IO91NB2F8	253	IO147PB3F13	194
IO08PB0F0	332	IO91PB2F8	254	IO148NB3F13	195
IO37NB0F3	325	IO99NB2F9	249	IO148PB3F13	196
IO37PB0F3	326	IO99PB2F9	250	IO149NB3F13	189
IO38NB0F3	323	IO100NB2F9	247	IO149PB3F13	190
IO38PB0F3	324	IO100PB2F9	248	IO161NB3F15	183
IO41NB0F3/HCLKAN	319	IO107NB2F10	243	IO161PB3F15	184
IO41PB0F3/HCLKAP	320	IO107PB2F10	244	IO163NB3F15	187
IO42NB0F3/HCLKBN	313	IO110NB2F10	241	IO163PB3F15	188
IO42PB0F3/HCLKBP	314	IO110PB2F10	242	IO165NB3F15	181
Bank 1		IO111NB2F10	237	IO165PB3F15	182
IO43NB1F4/HCLKCN	305	IO111PB2F10	238	IO167NB3F15	179
IO43PB1F4/HCLKCP	306	IO112NB2F10	235	IO167PB3F15	180
IO44NB1F4/HCLKDN	299	IO112PB2F10	236	**Bank 4**	
IO44PB1F4/HCLKDP	300	IO113NB2F10	231	IO181NB4F17	172
IO48NB1F4	295	IO113PB2F10	232	IO181PB4F17	173
IO48PB1F4	296	IO114NB2F10	229	IO182NB4F17	170
IO65NB1F6	283	IO114PB2F10	230	IO182PB4F17	171
IO65PB1F6	284	IO115NB2F10	225	IO183NB4F17	166
IO66NB1F6	289	IO115PB2F10	226	IO183PB4F17	167
IO66PB1F6	290	IO117NB2F10	223	IO184NB4F17	164
IO68NB1F6	287	IO117PB2F10	224	IO184PB4F17	165
IO68PB1F6	288	**Bank 3**		IO185NB4F17	160
IO69NB1F6	275	IO129NB3F12	219	IO185PB4F17	161
IO69PB1F6	276	IO129PB3F12	220	IO190NB4F17	158
IO70NB1F6	281	IO132NB3F12	217	IO190PB4F17	159
IO70PB1F6	282	IO132PB3F12	218	IO191NB4F17	154
IO71NB1F6	277	IO137NB3F12	213	IO191PB4F17	155
IO71PB1F6	278	IO137PB3F12	214	IO192NB4F17	152
IO73NB1F6	269	IO139NB3F13	211	IO192PB4F17	153
IO73PB1F6	270	IO139PB3F13	212	IO207NB4F19	146
IO74NB1F6	271	IO141NB3F13	205	IO207PB4F19	147

FIGURE 2. Terminal connections. 1/ 2/ 3/ 4/ 5/ 6/ 7/ 8/ 9/ 10/

Device Types	01 - 08	Device Types	01 - 08	Device Types	01 - 08
Case Outline	X	Case Outline	X	Case Outline	X
Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number
IO212NB4F19/CLKEN	142	IO280PB6F26	71	IO335NB7F31	12
IO212PB4F19/CLKEP	143	IO281NB6F26	66	IO335PB7F31	13
IO213NB4F19/CLKFN	136	IO281PB6F26	67	IO338NB7F31	6
IO213PB4F19/CLKFP	137	IO282NB6F26	64	IO338PB7F31	7
Bank 5		IO282PB6F26	65	IO341NB7F31	4
IO214NB5F20/CLKGN	128	IO284NB6F26	60	IO341PB7F31	5
IO214PB5F20/CLKGP	129	IO284PB6F26	61	**Dedicated I/O**	
IO215NB5F20/CLKHN	122	IO285NB6F26	58	GND	1
IO215PB5F20/CLKHP	123	IO285PB6F26	59	GND	9
IO217NB5F20	118	IO286NB6F26	54	GND	15
IO217PB5F20	119	IO286PB6F26	55	GND	21
IO236NB5F22	110	IO287NB6F26	52	GND	27
IO236PB5F22	111	IO287PB6F26	53	GND	33
IO237NB5F22	112	IO294NB6F27	48	GND	39
IO237PB5F22	113	IO294PB6F27	49	GND	45
IO238NB5F22	104	IO296NB6F27	46	GND	51
IO238PB5F22	105	IO296PB6F27	47	GND	57
IO239NB5F22	106	**Bank 7**		GND	63
IO239PB5F22	107	IO300NB7F28	42	GND	69
IO240NB5F22	100	IO300PB7F28	43	GND	75
IO240PB5F22	101	IO303NB7F28	40	GND	81
IO242NB5F22	94	IO303PB7F28	41	GND	88
IO242PB5F22	95	IO310NB7F29	34	GND	89
IO243NB5F22	98	IO310PB7F29	35	GND	97
IO243PB5F22	99	IO311NB7F29	36	GND	103
IO244NB5F22	92	IO311PB7F29	37	GND	109
IO244PB5F22	93	IO312NB7F29	28	GND	115
Bank 6		IO312PB7F29	29	GND	121
IO257PB6F24	86	IO315NB7F29	30	GND	133
IO258NB6F24	84	IO315PB7F29	31	GND	145
IO258PB6F24	85	IO316NB7F29	22	GND	151
IO261NB6F24	82	IO316PB7F29	23	GND	157
IO261PB6F24	83	IO317NB7F29	24	GND	163
IO262NB6F24	78	IO317PB7F29	25	GND	169
IO262PB6F24	79	IO318NB7F29	18	GND	176
IO265NB6F24	76	IO318PB7F29	19	GND	177
IO265PB6F24	77	IO320NB7F29	16	GND	186
IO279NB6F26	72	IO320PB7F29	17	GND	192
IO279PB6F26	73	IO334NB7F31	10	GND	198
IO280NB6F26	70	IO334PB7F31	11	GND	204

FIGURE 2. Terminal connections – Continued. 1/ 2/ 3/ 4/ 5/ 6/ 7/ 8/ 9/ 10/

Device Types	01 - 08	Device Types	01 - 08	Device Types	01 - 08
Case Outline	X	Case Outline	X	Case Outline	X
Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number
GND	210	PRB	311	VCCDA	178
GND	216	PRC	135	VCCDA	221
GND	222	PRD	134	VCCDA	266
GND	228	TCK	349	VCCDA	268
GND	234	TDI	348	VCCDA	293
GND	240	TDO	347	VCCDA	294
GND	246	TMS	350	VCCDA	307
GND	252	TRST	351	VCCDA	308
GND	258	VCCA	3	VCCDA	309
GND	264	VCCA	14	VCCDA	327
GND	265	VCCA	32	VCCDA	328
GND	274	VCCA	56	VCCDA	346
GND	280	VCCA	74	VCCIB0	321
GND	286	VCCA	87	VCCIB0	333
GND	292	VCCA	102	VCCIB0	344
GND	298	VCCA	114	VCCIB1	273
GND	310	VCCA	150	VCCIB1	285
GND	322	VCCA	162	VCCIB1	297
GND	330	VCCA	175	VCCIB2	227
GND	334	VCCA	191	VCCIB2	239
GND	340	VCCA	209	VCCIB2	245
GND	345	VCCA	233	VCCIB2	257
GND	352	VCCA	251	VCCIB3	185
NC	124	VCCA	263	VCCIB3	197
NC	125	VCCA	279	VCCIB3	203
NC	126	VCCA	291	VCCIB3	215
NC	127	VCCA	329	VCCIB4	144
NC	138	VCCA	339	VCCIB4	156
NC	139	VCCDA	2	VCCIB4	168
NC	140	VCCDA	44	VCCIB5	96
NC	141	VCCDA	90	VCCIB5	108
NC	301	VCCDA	91	VCCIB5	120
NC	302	VCCDA	116	VCCIB6	50
NC	303	VCCDA	117	VCCIB6	62
NC	304	VCCDA	130	VCCIB6	68
NC	315	VCCDA	131	VCCIB6	80
NC	316	VCCDA	132	VCCIB7	8
NC	317	VCCDA	148	VCCIB7	20
NC	318	VCCDA	149	VCCIB7	26
PRA	312	VCCDA	174	VCCIB7	38
				VPUMP	267

FIGURE 2. Terminal connections – Continued. 1/ 2/ 3/ 4/ 5/ 6/ 7/ 8/ 9/ 10/

Case X (device types 09 – 16).

Device Types	09 - 16	Device Types	09 - 16	Device Types	09 - 16
Case Outline	X	Case Outline	X	Case Outline	X
Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number
Bank 0		**Bank 2**		IO159NB3F14	189
IO01PB0F0	343	IO91NB2F8	257	IO159PB3F14	190
IO05NB0F0	341	IO91PB2F8	258	IO163NB3F15	187
IO05PB0F0	342	IO95NB2F8	253	IO163PB3F15	188
IO13NB0F1	337	IO95PB2F8	254	IO167NB3F15	183
IO13PB0F1	338	IO99NB2F9	251	IO167PB3F15	184
IO17NB0F1	335	IO99PB2F9	252	IO170NB3F15	181
IO17PB0F1	336	IO103NB2F9	245	IO170PB3F15	182
IO25NB0F2	331	IO103PB2F9	246	**Bank 4**	
IO25PB0F2	332	IO107NB2F10	241	IO172NB4F16	173
IO29NB0F2	329	IO107PB2F10	242	IO176NB4F16	171
IO29PB0F2	330	IO111NB2F10	239	IO176PB4F16	172
IO41NB0F3/HCLKAN	317	IO111PB2F10	240	IO184NB4F17	167
IO41PB0F3/HCLKAP	318	IO115NB2F10	235	IO184PB4F17	168
IO42NB0F3/HCLKBN	313	IO115PB2F10	236	IO188NB4F17	165
IO42PB0F3/HCLKBP	314	IO119NB2F11	233	IO188PB4F17	166
IO01PB0F0	343	IO119PB2F11	234	IO192NB4F17	161
IO05NB0F0	341	IO121NB2F11	229	IO192PB4F17	162
Bank 1		IO121NB2F11	230	IO196NB4F18	159
IO43NB1F4/HCLKCN	303	IO123NB2F11	227	IO196PB4F18	160
IO43PB1F4/HCLKCP	304	IO123PB2F11	228	IO200NB4F18	155
IO44NB1F4/HCLKDN	299	IO127NB2F11	223	IO200PB4F18	156
IO44PB1F4/HCLKDP	300	IO127PB2F11	224	IO208NB4F19	153
IO53NB1F4	287	**Bank 3**		IO208PB4F19	154
IO53PB1F4	288	IO131NB3F12	217	IO212NB4F19/CLKEN	141
IO57NB1F5	285	IO131PB3F12	218	IO212PB4F19/CLKEP	142
IO57PB1F5	286	IO135NB3F12	213	IO213NB4F19/CLKFN	137
IO61NB1F5	281	IO135PB3F12	214	IO213PB4F19/CLKFP	138
IO61PB1F5	282	IO137NB3F12	211	**Bank 5**	
IO65NB1F6	279	IO137PB3F12	212	IO214NB5F20/CLKGN	127
IO65PB1F6	280	IO139NB3F13	207	IO214PB5F20/CLKGP	128
IO69NB1F6	275	IO139PB3F13	208	IO215NB5F20/CLKHN	123
IO69PB1F6	276	IO143NB3F13	205	IO215PB5F20/CLKHP	124
IO77NB1F7	273	IO143PB3F13	206	IO218NB5F20	111
IO77PB1F7	274	IO147NB3F13	201	IO218PB5F20	112
IO81NB1F7	269	IO147PB3F13	202	IO228NB5F21	109
IO81PB1F7	270	IO151NB3F14	199	IO228PB5F21	110
Bank 2		IO151NB3F14	200	IO232NB5F21	105
IO87NB2F8	259	IO155NB3F14	195	IO232PB5F21	106
IO87PB2F8	260	IO155PB3F14	196	IO236NB5F22	103

FIGURE 2. Terminal connections – Continued. 1/ 2/ 3/ 4/ 5/ 6/ 7/ 8/ 9/ 10/

Case X (device types 09 – 16) – Continued.

Device Types	09 - 16	Device Types	09 - 16	Device Types	09 - 16
Case Outline	X	Case Outline	X	Case Outline	X
Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number
IO236PB5F22	104	IO322PB7F30	25	GND	198
IO240NB5F22	99	IO326NB7F30	20	GND	204
IO240PB5F22	100	IO326PB7F30	21	GND	210
IO246NB5F23	97	IO330NB7F30	14	GND	216
IO246PB5F23	98	IO330PB7F30	15	GND	222
IO248NB5F23	92	IO334NB7F31	12	GND	226
IO252NB5F23	93	IO334PB7F31	13	GND	232
IO252PB5F23	94	IO338NB7F31	8	GND	238
Bank 6		IO338PB7F31	9	GND	244
IO257PB6F24	84	IO341NB7F31	6	GND	248
IO258NB6F24	82	**Dedicated I/O**		GND	256
IO258PB6F24	83	GND	1	GND	262
IO262NB6F24	78	GND	5	GND	264
IO262PB6F24	79	GND	11	GND	265
IO266NB6F24	76	GND	19	GND	272
IO266PB6F24	77	GND	23	GND	278
IO270NB6F25	70	GND	29	GND	284
IO270PB6F25	71	GND	35	GND	293
IO274NB6F25	66	GND	41	GND	302
IO274PB6F25	67	GND	47	GND	308
IO278NB6F26	64	GND	51	GND	310
IO278PB6F26	65	GND	57	GND	316
IO282NB6F26	60	GND	63	GND	325
IO282PB6F26	61	GND	69	GND	334
IO286NB6F26	58	GND	73	GND	340
IO286PB6F26	59	GND	81	GND	345
IO290NB6F27	54	GND	86	GND	352
IO290PB6F27	55	GND	88	NC	16
IO294NB6F27	52	GND	89	NC	17
IO294PB6F27	53	GND	96	NC	44
IO298NB6F27	48	GND	102	NC	45
IO298PB6F27	49	GND	108	NC	74
Bank 7		GND	117	NC	75
O302NB7F28	42	GND	126	NC	113
IO302PB7F28	43	GND	132	NC	118
IO306NB7F28	38	GND	134	NC	119
IO306PB7F28	39	GND	140	NC	120
IO308NB7F28	32	GND	149	NC	122
IO308PB7F28	33	GND	158	NC	129
IO310NB7F29	36	GND	164	NC	143
IO310PB7F29	37	GND	170	NC	144
IO314NB7F29	30	GND	176	NC	146
IO314PB7F29	31	GND	177	NC	147
IO318NB7F29	26	GND	180	NC	151
IO318PB7F29	27	GND	186	NC	152
IO322NB7F30	24	GND	194	NC	191

FIGURE 2. Terminal connections – Continued. 1/ 2/ 3/ 4/ 5/ 6/ 7/ 8/ 9/ 10/

Case X (device types 09 – 16) – Continued.

Device Types	09 - 16	Device Types	09 - 16
Case Outline	X	Case Outline	X
Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number
NC	192	VCCA	261
NC	219	VCCA	277
NC	220	VCCA	292
NC	249	VCCA	307
NC	250	VCCA	324
NC	289	VCCA	339
NC	294	VCCDA	2
NC	295	VCCDA	130
NC	296	VCCDA	133
NC	298	VCCDA	145
NC	305	VCCDA	150
NC	319	VCCDA	174
NC	320	VCCDA	178
NC	322	VCCDA	221
NC	323	VCCDA	266
NC	327	VCCDA	268
NC	328	VCCDA	290
PRA	312	VCCDA	291
PRB	311	VCCDA	297
PRC	136	VCCDA	306
PRD	135	VCCDA	309
TCK	349	VCCDA	321
TDI	348	VCCDA	326
TDO	347	VCCDA	346
TMS	350	VCCIB0	315
TRST	351	VCCIB0	333
VCCA	3	VCCIB0	344
VCCA	87	VCCIB1	271
VCCA	175	VCCIB1	283
VCCA	263	VCCIB1	301
VCCA	4	VCCIB2	225
VCCA	18	VCCIB2	237
VCCA	34	VCCIB2	243
VCCA	56	VCCIB5	107
VCCA	72	VCCIB5	125
VCCA	85	VCCIB6	50
VCCA	101	VCCIB6	62
VCCA	116	VCCIB6	68
VCCA	131	VCCIB6	80
VCCA	148	VCCIB7	10
VCCA	163	VCCIB7	22
VCCA	179	VCCIB7	28
VCCA	193	VCCIB7	40
VCCA	209	VPUMP	267
VCCA	231		
VCCA	247		

FIGURE 2. Terminal connections – Continued. 1/ 2/ 3/ 4/ 5/ 6/ 7/ 8/ 9/ 10/

Case Y, Z, and N (device types 01 – 08).

Device Types	01 - 08	Device Types	01 - 08	Device Types	01 - 08
Case Outline	Y, Z, N	Case Outline	Y, Z, N	Case Outline	Y, Z, N
Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number
Bank 0		IO33NB0F2	D12	IO63NB1F5	H18
IO00NB0F0	D7	IO33PB0F2	D11	IO65NB1F6	C17
IO00PB0F0	E7	IO34NB0F3	A11	IO66PB1F6	B18
IO01NB0F0	G7	IO34PB0F3	A10	IO67NB1F6	J18
IO01PB0F0	G6	IO37NB0F3	J13	IO67PB1F6	J19
IO02NB0F0	B5	IO37PB0F3	K13	IO68NB1F6	B20
IO02PB0F0	B4	IO38NB0F3	H11	IO68PB1F6	B19
IO04PB0F0	C7	IO38PB0F3	G11	IO69NB1F6	E17
IO05NB0F0	F8	IO40PB0F3	B12	IO69PB1F6	F17
IO05PB0F0	F7	IO41NB0F3/HCLKAN	G13	IO70NB1F6	B22
IO06NB0F0	H8	IO41PB0F3/HCLKAP	G12	IO70PB1F6	B21
IO06PB0F0	H7	IO42NB0F3/HCLKBN	C13	IO71PB1F6	G18
IO11NB0F0	J8	IO42PB0F3/HCLKBP	C12	IO73NB1F6	G19
IO11PB0F0	J7	**Bank 1**		IO74NB1F6	C19
IO12PB0F1	B6	IO43NB1F4/HCLKCN	G15	IO74PB1F6	C18
IO13NB0F1	E9	IO43PB1F4/HCLKCP	G14	IO75NB1F6	D18
IO13PB0F1	D8	IO44NB1F4/HCLKDN	B14	IO75PB1F6	D17
IO15NB0F1	C9	IO44PB1F4/HCLKDP	B13	IO76NB1F7	C21
IO15PB0F1	C8	IO45NB1F4	H13	IO76PB1F7	C20
IO16NB0F1	A5	IO47NB1F4	D14	IO79NB1F7	H20
IO16PB0F1	A4	IO47PB1F4	C14	IO79PB1F7	H19
IO17NB0F1	D10	IO48NB1F4	A16	IO80NB1F7	E18
IO17PB0F1	D9	IO48PB1F4	A15	IO80PB1F7	F18
IO18NB0F1	A7	IO49PB1F4	H15	IO81NB1F7	G21
IO18PB0F1	A6	IO51NB1F4	E15	IO81PB1F7	G20
IO19NB0F1	G9	IO51PB1F4	F15	IO82NB1F7	F20
IO19PB0F1	G8	IO52NB1F4	A17	IO82PB1F7	F19
IO20PB0F1	B7	IO55NB1F5	G16	IO85NB1F7	D20
IO23NB0F2	F10	IO55PB1F5	H16	IO85PB1F7	D19
IO23PB0F2	F9	IO56NB1F5	A20	**Bank 2**	
IO26NB0F2	C11	IO56PB1F5	A19	IO86NB2F8	F23
IO26PB0F2	B8	IO57NB1F5	D16	IO86PB2F8	E23
IO27NB0F2	H10	IO57PB1F5	D15	IO87NB2F8	H23
IO27PB0F2	H9	IO58NB1F5	A22	IO87PB2F8	G23
IO28NB0F2	A9	IO58PB1F5	A21	IO88NB2F8	E24
IO28PB0F2	B9	IO59NB1F5	F16	IO88PB2F8	D24
IO30NB0F2	B11	IO61NB1F5	G17	IO89NB2F8	M17
IO30PB0F2	B10	IO61PB1F5	H17	IO89PB2F8	G22
IO31NB0F2	E11	IO62NB1F5	B17	IO91NB2F8	J22
IO31PB0F2	F11	IO62PB1F5	B16	IO91PB2F8	H22

FIGURE 2. Terminal connections – Continued. 1/ 2/ 3/ 4/ 5/ 6/ 7/ 8/ 9/ 10/

Case Y, Z, and N (device types 01 – 08) – Continued.

Device Types	01 - 08	Device Types	01 - 08	Device Types	01 - 08
Case Outline	Y, Z, N	Case Outline	Y, Z, N	Case Outline	Y, Z, N
Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number
IO92NB2F8	L18	IO127NB2F11	P18	IO163NB3F15	V22
IO92PB2F8	K18	IO127PB2F11	P17	IO163PB3F15	U22
IO96NB2F9	G24	IO128NB2F11	N25	IO164NB3F15	V23
IO96PB2F9	F24	IO128PB2F11	M25	IO164PB3F15	V24
IO97NB2F9	J21	**Bank 3**		IO166NB3F15	AB24
IO97PB2F9	J20	IO129NB3F12	N20	IO167NB3F15	V21
IO98PB2F9	J23	IO130PB3F12	P24	IO167PB3F15	U21
IO99NB2F9	L19	IO131NB3F12	P21	IO168NB3F15	Y23
IO99PB2F9	K19	IO133NB3F12	P20	IO168PB3F15	AA23
IO100NB2F9	E25	IO133PB3F12	P19	IO169NB3F15	W22
IO100PB2F9	D25	IO138NB3F12	R23	IO169PB3F15	W23
IO103PB2F9	K20	IO138PB3F12	P23	IO170NB3F15	Y22
IO105NB2F9	M19	IO139NB3F13	R22	IO170PB3F15	Y21
IO105PB2F9	M18	IO139PB3F13	P22	**Bank 4**	
IO106NB2F9	J24	IO141NB3F13	R19	IO171NB4F16	AC20
IO106PB2F9	H24	IO142NB3F13	R25	IO171PB4F16	AC21
IO107NB2F10	L23	IO142PB3F13	P25	IO172NB4F16	W20
IO107PB2F10	N16	IO143PB3F13	R21	IO172PB4F16	Y20
IO109NB2F10	L22	IO145NB3F13	T18	IO173NB4F16	AD21
IO109PB2F10	K22	IO145PB3F13	R18	IO173PB4F16	AD22
IO110NB2F10	G25	IO146NB3F13	T24	IO174NB4F16	AA19
IO110PB2F10	F25	IO146PB3F13	R24	IO176NB4F16	Y18
IO111NB2F10	L21	IO147NB3F13	T20	IO176PB4F16	Y19
IO111PB2F10	L20	IO147PB3F13	R20	IO177NB4F16	AB19
IO112NB2F10	L24	IO148NB3F13	U25	IO177PB4F16	AB18
IO112PB2F10	K24	IO148PB3F13	T25	IO182NB4F17	V19
IO113NB2F10	N17	IO149NB3F13	T22	IO182PB4F17	W19
IO115NB2F10	M20	IO153NB3F14	U19	IO183PB4F17	AC19
IO115PB2F10	M21	IO153PB3F14	T19	IO184NB4F17	AB17
IO117NB2F10	N19	IO154NB3F14	Y25	IO184PB4F17	AC17
IO117PB2F10	N18	IO154PB3F14	W25	IO185NB4F17	AD19
IO118NB2F11	J25	IO157NB3F14	V20	IO185PB4F17	AD20
IO121NB2F11	N24	IO157PB3F14	U20	IO187PB4F17	AC18
IO121PB2F11	M24	IO158NB3F14	AB25	IO188NB4F17	Y17
IO122NB2F11	L25	IO158PB3F14	AA25	IO188PB4F17	AA17
IO122PB2F11	K25	IO160PB3F14	W24	IO189PB4F17	AE22
IO123NB2F11	N22	IO161NB3F15	U24	IO191NB4F17	W18
IO123PB2F11	M22	IO161PB3F15	U23	IO191PB4F17	V18
IO124NB2F11	N23	IO162NB3F15	AA24	IO192PB4F17	U18
IO124PB2F11	M23	IO162PB3F15	Y24	IO195PB4F18	AE21

FIGURE 2. Terminal connections – Continued. 1/ 2/ 3/ 4/ 5/ 6/ 7/ 8/ 9/ 10/

Case Y, Z, and N (device types 01 - 08) – Continued.

Device Types	01 - 08	Device Types	01 - 08	Device Types	01 - 08
Case Outline	Y, Z, N	Case Outline	Y, Z, N	Case Outline	Y, Z, N
Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number
IO196NB4F18	AB16	IO225NB5F21	AE6	IO256PB5F23	AA6
IO197NB4F18	AD17	IO225PB5F21	AE7	**Bank 6**	
IO197PB4F18	AD18	IO226NB5F21	Y10	IO257NB6F24	Y3
IO198NB4F18	V17	IO226PB5F21	W10	IO257PB6F24	AA3
IO198PB4F18	W17	IO227PB5F21	T13	IO258NB6F24	V3
IO199NB4F18	AE19	IO228NB5F21	AB10	IO258PB6F24	W3
IO199PB4F18	AE20	IO228PB5F21	AB11	IO259NB6F24	AA2
IO200NB4F18	AC15	IO229NB5F21	AD9	IO259PB6F24	AB2
IO201NB4F18	AD15	IO229PB5F21	AD10	IO260NB6F24	V6
IO201PB4F18	AD16	IO230NB5F21	V11	IO260PB6F24	W4
IO202NB4F18	Y15	IO233NB5F21	AD7	IO262NB6F24	U4
IO202PB4F18	Y16	IO233PB5F21	AD8	IO262PB6F24	V4
IO206NB4F19	AB14	IO234NB5F21	V9	IO263NB6F24	Y5
IO206PB4F19	AB15	IO234PB5F21	V10	IO263PB6F24	W5
IO207NB4F19	AE15	IO236NB5F22	AC9	IO268NB6F25	U6
IO207PB4F19	AE16	IO238NB5F22	W8	IO268PB6F25	U5
IO208PB4F19	W16	IO238PB5F22	W9	IO269PB6F25	U3
IO209NB4F19	AE14	IO239NB5F22	AE4	IO272NB6F25	T2
IO210NB4F19	V15	IO239PB5F22	AE5	IO272PB6F25	U2
IO210PB4F19	V16	IO240NB5F22	AB9	IO273NB6F25	W2
IO211NB4F19	AD14	IO242NB5F22	AA9	IO273PB6F25	Y2
IO211PB4F19	AC14	IO242PB5F22	Y9	IO274NB6F25	R6
IO212NB4F19/CLKEN	W14	IO243NB5F22	AD5	IO274PB6F25	T6
IO212PB4F19/CLKEP	W15	IO243PB5F22	AD6	IO275NB6F25	T7
IO213NB4F19/CLKFN	AC13	IO244NB5F22	U8	IO275PB6F25	U7
IO213PB4F19/CLKFP	AD13	IO246NB5F23	AB8	IO277NB6F25	V2
Bank 5		IO246PB5F23	AC8	IO278NB6F26	R4
IO214NB5F20/CLKGN	W13	IO247NB5F23	AB7	IO278PB6F26	T4
IO214PB5F20/CLKGP	Y13	IO247PB5F23	AC7	IO279PB6F26	R3
IO215NB5F20/CLKHN	AC12	IO250NB5F23	AA8	IO280NB6F26	R5
IO215PB5F20/CLKHP	AD12	IO250PB5F23	Y8	IO281NB6F26	AA1
IO216NB5F20	U13	IO251NB5F23	V8	IO281PB6F26	AB1
IO216PB5F20	V13	IO251PB5F23	V7	IO284NB6F26	R8
IO217NB5F20	AE10	IO252NB5F23	Y7	IO284PB6F26	T8
IO217PB5F20	AE11	IO252PB5F23	W7	IO285NB6F26	W1
IO218NB5F20	W11	IO253NB5F23	AC5	IO285PB6F26	Y1
IO218PB5F20	W12	IO253PB5F23	AC6	IO286NB6F26	P2
IO222NB5F20	AA11	IO254NB5F23	Y6	IO286PB6F26	R2
IO222PB5F20	Y11	IO254PB5F23	W6	IO287NB6F26	T1
IO223PB5F21	AE9	IO256NB5F23	AB6	IO287PB6F26	U1

FIGURE 2. Terminal connections – Continued. 1/ 2/ 3/ 4/ 5/ 6/ 7/ 8/ 9/ 10/

Case Y, Z, and N (device types 01 - 08) – Continued.

Device Types	01 - 08	Device Types	01 - 08	Device Types	01 - 08
Case Outline	Y, Z, N	Case Outline	Y, Z, N	Case Outline	Y, Z, N
Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number
IO288NB6F26	P5	IO324NB7F30	M9	GND	AC10
IO290NB6F27	P6	IO324PB7F30	M8	GND	AC16
IO291NB6F27	P1	IO327NB7F30	F1	GND	AC23
IO291PB6F27	R1	IO327PB7F30	G1	GND	AC3
IO292NB6F27	P7	IO328NB7F30	K7	GND	AD1
IO292PB6F27	R7	IO328PB7F30	K6	GND	AD2
IO293NB6F27	M1	IO329NB7F30	D1	GND	AD24
IO293PB6F27	N1	IO329PB7F30	E1	GND	AD25
IO294NB6F27	P8	IO331PB7F30	G2	GND	AE1
IO296NB6F27	N3	IO332NB7F31	H3	GND	AE18
IO296PB6F27	P3	IO332PB7F31	H2	GND	AE2
IO298NB6F27	N4	IO333NB7F31	E2	GND	AE24
IO298PB6F27	P4	IO333PB7F31	F2	GND	AE25
IO299NB6F27	M2	IO334NB7F31	H4	GND	AE8
IO299PB6F27	N2	IO334PB7F31	J4	GND	B1
Bank 7		IO335NB7F31	H5	GND	B2
IO300NB7F28	P9	IO335PB7F31	H6	GND	B24
IO300PB7F28	N6	IO337NB7F31	D2	GND	B25
IO302NB7F28	M6	IO338NB7F31	J6	GND	C10
IO304NB7F28	N8	IO338PB7F31	J5	GND	C16
IO304PB7F28	N7	IO339NB7F31	F3	GND	C23
IO308NB7F28	M4	IO339PB7F31	E3	GND	C3
IO309NB7F28	L3	IO340NB7F31	G4	GND	D22
IO309PB7F28	M3	IO340PB7F31	G3	GND	D4
IO310NB7F29	N10	IO341NB7F31	K8	GND	E10
IO310PB7F29	N9	IO341PB7F31	L8	GND	E16
IO311NB7F29	K1	**Dedicated I/O**		GND	E21
IO311PB7F29	L1	GND	K5	GND	E5
IO313NB7F29	M5	GND	A18	GND	E8
IO316NB7F29	L6	GND	A2	GND	H1
IO316PB7F29	L5	GND	A24	GND	H21
IO317NB7F29	K2	GND	A25	GND	H25
IO317PB7F29	L2	GND	A8	GND	K21
IO318NB7F29	K4	GND	AA10	GND	K23
IO318PB7F29	L4	GND	AA16	GND	K3
IO320NB7F29	J3	GND	AA18	GND	L11
IO321NB7F30	J2	GND	AA21	GND	L12
IO321PB7F30	J1	GND	AA5	GND	L13
IO323NB7F30	L7	GND	AB22	GND	L14
IO323PB7F30	M7	GND	AB4	GND	L15

FIGURE 2. Terminal connections – Continued. 1/ 2/ 3/ 4/ 5/ 6/ 7/ 8/ 9/ 10/

Case Y, Z, and N (device types 01 - 08) – Continued.

Device Types	01 - 08	Device Types	01 - 08	Device Types	01 - 08
Case Outline	Y, Z, N	Case Outline	Y, Z, N	Case Outline	Y, Z, N
Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number
GND	M11	NC	V14	VCCDA	AD11
GND	M12	NC	Y12	VCCDA	AD4
GND	M13	NC	Y14	VCCDA	AE12
GND	M14	PRA	F13	VCCDA	AE17
GND	M15	PRB	A13	VCCDA	B15
GND	N11	PRC	AB12	VCCDA	C15
GND	N12	PRD	AE13	VCCDA	C6
GND	N13	TCK	F5	VCCDA	D13
GND	N14	TDI	C5	VCCDA	E13
GND	N15	TDO	F6	VCCDA	E19
GND	P11	TMS	D6	VCCDA	F21
GND	P12	TRST	E6	VCCDA	G10
GND	P13	VCCA	AB20	VCCDA	G5
GND	P14	VCCA	F22	VCCDA	N21
GND	P15	VCCA	F4	VCCDA	N5
GND	R11	VCCA	J17	VCCDA	W21
GND	R12	VCCA	J9	VCCIB0	A3
GND	R13	VCCA	K10	VCCIB0	B3
GND	R14	VCCA	K11	VCCIB0	C4
GND	R15	VCCA	K15	VCCIB0	D5
GND	T21	VCCA	K16	VCCIB0	J10
GND	T23	VCCA	L10	VCCIB0	J11
GND	T3	VCCA	L16	VCCIB0	K12
GND	T5	VCCA	R10	VCCIB1	A23
GND	V1	VCCA	R16	VCCIB1	B23
GND	V25	VCCA	T10	VCCIB1	C22
GND	V5	VCCA	T11	VCCIB1	D21
NC	AA12	VCCA	T15	VCCIB1	J15
NC	AA14	VCCA	T16	VCCIB1	J16
NC	E12	VCCA	U17	VCCIB1	K14
NC	E14	VCCA	U9	VCCIB2	C24
NC	F12	VCCA	Y4	VCCIB2	C25
NC	F14	VCCDA	A12	VCCIB2	D23
NC	H12	VCCDA	A14	VCCIB2	E22
NC	H14	VCCDA	AA13	VCCIB2	K17
NC	J12	VCCDA	AA15	VCCIB2	L17
NC	J14	VCCDA	AA20	VCCIB2	M16
NC	U12	VCCDA	AA7	VCCIB3	AA22
NC	U14	VCCDA	AB13	VCCIB3	AB23
NC	V12	VCCDA	AC11	VCCIB3	AC24

FIGURE 2. Terminal connections – Continued. 1/ 2/ 3/ 4/ 5/ 6/ 7/ 8/ 9/ 10/

Case Y, Z, and N (device types 01 - 08) – Continued.

Device Types	01 - 08	Device Types	01 - 08	Device Types	01 - 08
Case Outline	Y, Z, N	Case Outline	Y, Z, N	Case Outline	Y, Z, N
Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number
VCCIB3	AC25	VCCIB5	AB5	VCCIB6	P10
VCCIB3	P16	VCCIB5	AC4	VCCIB6	R9
VCCIB3	R17	VCCIB5	AD3	VCCIB6	T9
VCCIB3	T17	VCCIB5	AE3	VCCIB7	C1
VCCIB4	AB21	VCCIB5	T12	VCCIB7	C2
VCCIB4	AC22	VCCIB5	U10	VCCIB7	D3
VCCIB4	AD23	VCCIB5	U11	VCCIB7	E4
VCCIB4	AE23	VCCIB6	AA4	VCCIB7	K9
VCCIB4	T14	VCCIB6	AB3	VCCIB7	L9
VCCIB4	U15	VCCIB6	AC1	VCCIB7	M10
VCCIB4	U16	VCCIB6	AC2	VPUMP	E20

FIGURE 2. Terminal connections – Continued. 1/ 2/ 3/ 4/ 5/ 6/ 7/ 8/ 9/ 10/

Case U (device types 01 – 08).

Device Types	01- 08	Device Types	01- 08	Device Types	01- 08
Case Outline	U	Case Outline	U	Case Outline	U
Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number
Bank 0		O112NB2F10	174	IO192NB4F17	110
IO01NB0F0	248	IO112PB2F10	175	IO192PB4F17	111
IO01PB0F0	249	IO113NB2F10	172	IO212NB4F19/CLKEN	104
IO04NB0F0	246	IO113PB2F10	173	IO212PB4F19/CLKEP	105
IO04PB0F0	247	IO114NB2F10	168	IO213NB4F19/CLKFN	100
IO05NB0F0	242	IO114PB2F10	169	IO213PB4F19/CLKFP	101
IO05PB0F0	243	IO115NB2F10	166	**Bank 5**	
IO08NB0F0	240	IO115PB2F10	167	IO214NB5F20/CLKGN	92
IO08PB0F0	241	IO117NB2F10	162	IO214PB5F20/CLKGP	93
IO37NB0F3	234	IO117PB2F10	163	IO215NB5F20/CLKHN	88
IO37PB0F3	235	**Bank 3**		IO215PB5F20/CLKHP	89
IO41NB0F3/HCLKAN	232	IO139NB3F13	158	IO236NB5F22	82
IO41PB0F3/HCLKAP	233	IO139PB3F13	159	IO236PB5F22	83
IO42NB0F3/HCLKBN	228	IO141NB3F13	154	IO238NB5F22	80
IO42PB0F3/HCLKBP	229	IO141PB3F13	155	IO238PB5F22	81
Bank 1		IO142NB3F13	152	IO240NB5F22	76
IO43NB1F4/HCLKCN	220	IO142PB3F13	153	IO240PB5F22	77
IO43PB1F4/HCLKCP	221	IO145NB3F13	148	IO242NB5F22	74
IO44NB1F4/HCLKDN	216	IO145PB3F13	149	IO242PB5F22	75
IO44PB1F4/HCLKDP	217	IO146NB3F13	146	IO243NB5F22	70
IO65NB1F6	210	IO146PB3F13	147	IO243PB5F22	71
IO65PB1F6	211	IO147NB3F13	140	IO244NB5F22	68
IO69NB1F6	208	IO147PB3F13	141	IO244PB5F22	69
IO69PB1F6	209	IO148NB3F13	142	**Bank 6**	
IO70NB1F6	199	IO148PB3F13	143	IO257PB6F24	60
IO71NB1F6	204	IO149NB3F13	136	IO258NB6F24	58
IO71PB1F6	205	IO149PB3F13	137	IO258PB6F24	59
IO73NB1F6	202	IO165NB3F15	135	IO279NB6F26	56
IO73PB1F6	203	IO167NB3F15	133	IO279PB6F26	57
IO74NB1F6	197	IO167PB3F15	134	IO280NB6F26	52
IO74PB1F6	198	**Bank 4**		IO280PB6F26	53
Bank 2		IO181NB4F17	124	IO281NB6F26	50
IO87NB2F8	187	IO181PB4F17	125	IO281PB6F26	51
IO87PB2F8	188	IO182NB4F17	122	IO282NB6F26	46
IO89PB2F8	186	IO182PB4F17	123	IO282PB6F26	47
IO107NB2F10	184	IO183NB4F17	118	IO284NB6F26	44
IO107PB2F10	185	IO183PB4F17	119	IO284PB6F26	45
IO110NB2F10	180	IO184NB4F17	116	IO285NB6F26	40
IO110PB2F10	181	IO184PB4F17	117	IO285PB6F26	41
IO111NB2F10	178	IO190NB4F17	112	IO286NB6F26	38
IO111PB2F10	179	IO190PB4F17	113	IO286PB6F26	39

FIGURE 2. Terminal connections – Continued. 1/ 2/ 3/ 4/ 5/ 6/ 7/ 8/ 9/ 10/

Device Types	01- 08	Device Types	01- 08	Device Types	01- 08
Case Outline	U	Case Outline	U	Case Outline	U
Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number
Bank 7		GND	109	VCCA	61
IO310NB7F29	30	GND	115	VCCA	63
IO310PB7F29	31	GND	121	VCCA	84
IO311NB7F29	26	GND	128	VCCA	108
IO311PB7F29	27	GND	129	VCCA	127
IO312NB7F29	24	GND	132	VCCA	131
IO312PB7F29	25	GND	139	VCCA	150
IO315NB7F29	20	GND	145	VCCA	170
IO315PB7F29	21	GND	151	VCCA	189
IO316NB7F29	18	GND	157	VCCA	191
IO316PB7F29	19	GND	161	VCCA	212
IO317NB7F29	14	GND	165	VCCA	238
IO317PB7F29	15	GND	171	VCCDA	2
IO318NB7F29	12	GND	177	VCCDA	32
IO318PB7F29	13	GND	183	VCCDA	66
IO320NB7F29	8	GND	190	VCCDA	67
IO320PB7F29	9	GND	192	VCCDA	86
IO341NB7F31	6	GND	193	VCCDA	87
IO341PB7F31	7	GND	201	VCCDA	94
Dedicated I/O		GND	207	VCCDA	95
GND	1	GND	213	VCCDA	96
GND	5	GND	219	VCCDA	106
GND	11	GND	225	VCCDA	107
GND	17	GND	231	VCCDA	126
GND	23	GND	239	VCCDA	130
GND	29	GND	245	VCCDA	160
GND	33	GND	256	VCCDA	194
GND	37	PRA	227	VCCDA	196
GND	43	PRB	226	VCCDA	214
GND	49	PRC	99	VCCDA	215
GND	55	PRD	98	VCCDA	222
GND	62	TCK	253	VCCDA	223
GND	64	TDI	252	VCCDA	224
GND	65	TDO	250	VCCDA	236
GND	73	TMS	254	VCCDA	237
GND	79	TRST	255	VCCDA	251
GND	85	VCCA	3	VCCIB0	230
GND	91	VCCA	4	VCCIB0	244
GND	97	VCCA	22	VCCIB1	200
GND	103	VCCA	42	VCCIB1	206

FIGURE 2. Terminal connections – Continued. 1/ 2/ 3/ 4/ 5/ 6/ 7/ 8/ 9/ 10/

Case U (device types 01 - 08) - Continued

Device Types	01- 08
Case Outline	U
Terminal Symbol	Terminal Number
VCCIB1	206
VCCIB1	218
VCCIB2	164
VCCIB2	176
VCCIB2	182
VCCIB3	138
VCCIB3	144
VCCIB3	156
VCCIB4	102
VCCIB4	114
VCCIB4	120
VCCIB5	72
VCCIB5	78
VCCIB5	90
VCCIB6	36
VCCIB6	48
VCCIB6	54
VCCIB7	10
VCCIB7	16
VCCIB7	28
VPUMP	195

FIGURE 2. Terminal connections – Continued. 1/ 2/ 3/ 4/ 5/ 6/ 7/ 8/ 9/ 10/

Case M and T (device types 01 – 08).

Device Types	01 - 08	Device Types	01 - 08	Device Types	01 - 08
Case Outline	M & T	Case Outline	M & T	Case Outline	M & T
Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number
Bank 0		IO19PB0F1	G13	IO39PB0F3	L16
IO00NB0F0	D6	IO20NB0F1	A10	IO40NB0F3	D17
IO00PB0F0	C6	IO20PB0F1	A9	IO40PB0F3	C17
IO01NB0F0	H10	IO21NB0F1	K14	IO41NB0F3/HCLKAN	E16
IO01PB0F0	H9	IO21PB0F1	K13	IO41PB0F3/HCLKAP	F16
IO02NB0F0	F8	IO22NB0F2	B11	IO42NB0F3/HCLKBN	G17
IO02PB0F0	G8	IO22PB0F2	B10	IO42PB0F3/HCLKBP	F17
IO03NB0F0	A6	IO23NB0F2	C12	**Bank 1**	
IO03PB0F0	B6	IO23PB0F2	C11	IO43NB1F4/HCLKCN	G19
IO04NB0F0	C7	IO24NB0F2	A12	IO43PB1F4/HCLKCP	G18
IO04PB0F0	D7	IO24PB0F2	A11	IO44NB1F4/HCLKDN	E19
IO05NB0F0	K10	IO25NB0F2	H14	IO44PB1F4/HCLKDP	F19
IO05PB0F0	J10	IO25PB0F2	J14	IO45NB1F4	C18
IO06NB0F0	F9	IO26NB0F2	D13	IO45PB1F4	D18
IO06PB0F0	G9	IO26PB0F2	D12	IO46NB1F4	A18
IO07NB0F0	F10	IO27NB0F2	F14	IO46PB1F4	B18
IO07PB0F0	G10	IO27PB0F2	G14	IO47NB1F4	K19
IO08NB0F0	E9	IO28NB0F2	E14	IO47PB1F4	L19
IO08PB0F0	E8	IO28PB0F2	E13	IO48NB1F4	C19
IO09NB0F0	J11	IO29NB0F2	B13	IO48PB1F4	D19
IO09PB0F0	K11	IO29PB0F2	B12	IO49NB1F4	K20
IO10NB0F0	C8	IO30NB0F2	C14	IO49PB1F4	L20
IO10PB0F0	D8	IO30PB0F2	C13	IO50NB1F4	A19
IO11NB0F0	K12	IO31NB0F2	H15	IO50PB1F4	B19
IO11PB0F0	J12	IO31PB0F2	J15	IO51NB1F4	H20
IO12NB0F1	G11	IO32NB0F2	A14	IO51PB1F4	J20
IO12PB0F1	H11	IO32PB0F2	B14	IO52NB1F4	B20
IO13NB0F1	G12	IO33NB0F2	K15	IO52PB1F4	A20
IO13PB0F1	H12	IO33PB0F2	L15	IO53NB1F4	F20
IO14NB0F1	A7	IO34NB0F3	D15	IO53PB1F4	E20
IO14PB0F1	B7	IO34PB0F3	D14	IO54NB1F5	B21
IO15NB0F1	H13	IO35NB0F3	A15	IO54PB1F5	A21
IO15PB0F1	J13	IO35PB0F3	B15	IO55NB1F5	K21
IO16NB0F1	C9	IO36NB0F3	B16	IO55PB1F5	J21
IO16PB0F1	D9	IO36PB0F3	A16	IO56NB1F5	D21
IO17NB0F1	F12	IO37NB0F3	G16	IO56PB1F5	C21
IO17PB0F1	F11	IO37PB0F3	G15	IO57NB1F5	G22
IO18NB0F1	E11	IO38NB0F3	D16	IO57PB1F5	G21
IO18PB0F1	E10	IO38PB0F3	C16	IO58NB1F5	E22
IO19NB0F1	F13	IO39NB0F3	K16	IO58PB1F5	E21

FIGURE 2. Terminal connections – Continued. 1/ 2/ 3/ 4/ 5/ 6/ 7/ 8/ 9/ 10/

Case M and T (device types 01 - 08) – Continued.

Device Types	01 - 08	Device Types	01 - 08	Device Types	01 - 08
Case Outline	M & T	Case Outline	M & T	Case Outline	M & T
Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number
IO59NB1F5	D22	IO79NB1F7	H25	IO98PB2F9	K30
IO59PB1F5	C22	IO79PB1F7	G25	IO99NB2F9	N25
IO60NB1F5	B23	IO80NB1F7	F27	IO99PB2F9	N26
IO60PB1F5	A23	IO80PB1F7	E27	IO100NB2F9	M29
IO61NB1F5	H22	IO81NB1F7	J25	IO100PB2F9	L29
IO61PB1F5	H21	IO81PB1F7	J24	IO101NB2F9	L33
IO62NB1F5	C24	IO82NB1F7	D29	IO101PB2F9	L32
IO62PB1F5	C23	IO82PB1F7	C29	IO102NB2F9	K34
IO63NB1F5	F23	IO83NB1F7	H26	IO102PB2F9	K33
IO63PB1F5	F22	IO83PB1F7	G26	IO103NB2F9	N28
IO64NB1F6	B24	IO84NB1F7	F28	IO103PB2F9	M28
IO64PB1F6	A24	IO84PB1F7	E28	IO104NB2F9	M34
IO65NB1F6	J22	IO85NB1F7	H27	IO104PB2F9	L34
IO65PB1F6	K22	IO85PB1F7	G27	IO105NB2F9	P27
IO66NB1F6	B25	**Bank 2**		IO105PB2F9	N27
IO66PB1F6	A25	IO86NB2F8	J28	IO106NB2F9	M32
IO67NB1F6	K23	IO86PB2F8	J27	IO106PB2F9	M31
IO67PB1F6	J23	IO87NB2F8	M25	IO107NB2F10	P25
IO68NB1F6	F24	IO87PB2F8	L25	IO107PB2F10	P26
IO68PB1F6	E24	IO88NB2F8	L26	IO108NB2F10	N33
IO69NB1F6	C27	IO88PB2F8	K26	IO108PB2F10	M33
IO69PB1F6	C26	IO89NB2F8	G31	IO109NB2F10	P29
IO70NB1F6	H24	IO89PB2F8	F31	IO109PB2F10	N29
IO70PB1F6	G24	IO90NB2F8	H29	IO110NB2F10	P30
IO71NB1F6	H23	IO90PB2F8	G29	IO110PB2F10	N30
IO71PB1F6	G23	IO91NB2F8	K28	IO111NB2F10	R24
IO72NB1F6	B28	IO91PB2F8	K27	IO111PB2F10	R25
IO72PB1F6	A28	IO92NB2F8	J30	IO112NB2F10	P31
IO73NB1F6	E26	IO92PB2F8	H30	IO112PB2F10	N31
IO73PB1F6	E25	IO93NB2F8	L28	IO113NB2F10	R28
IO74NB1F6	F26	IO93PB2F8	L27	IO113PB2F10	P28
IO74PB1F6	F25	IO94NB2F8	K29	IO114NB2F10	P32
IO75NB1F6	K25	IO94PB2F8	J29	IO114PB2F10	N32
IO75PB1F6	K24	IO95NB2F8	K31	IO115NB2F10	R30
IO76NB1F7	D27	IO95PB2F8	J31	IO115PB2F10	R29
IO76PB1F7	D26	IO96NB2F9	J32	IO116NB2F10	P34
IO77NB1F7	B29	IO96PB2F9	H32	IO116PB2F10	P33
IO77PB1F7	A29	IO97NB2F9	M27	IO117NB2F10	R27
IO78NB1F7	D28	IO97PB2F9	M26	IO117PB2F10	R26
IO78PB1F7	C28	IO98NB2F9	L30	IO118NB2F11	R34

FIGURE 2. Terminal connections – Continued. 1/ 2/ 3/ 4/ 5/ 6/ 7/ 8/ 9/ 10/

Case M and T (device types 01 - 08) – Continued.

Device Types	01 - 08	Device Types	01 - 08	Device Types	01 - 08
Case Outline	M & T	Case Outline	M & T	Case Outline	M & T
Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number
IO118PB2F11	R33	IO138NB3F12	Y29	IO158NB3F14	AH33
IO119NB2F11	T24	IO138PB3F12	W29	IO158PB3F14	AG33
IO119PB2F11	T25	IO139NB3F13	Y27	IO159NB3F14	AD27
IO120NB2F11	T33	IO139PB3F13	W27	IO159PB3F14	AC27
IO120PB2F11	T34	IO140NB3F13	AA33	IO160NB3F14	AG32
IO121NB2F11	T27	IO140PB3F13	Y33	IO160PB3F14	AF32
IO121PB2F11	T26	IO141NB3F13	Y25	IO161NB3F15	AG31
IO122NB2F11	T30	IO141PB3F13	Y24	IO161PB3F15	AF31
IO122PB2F11	T29	IO142NB3F13	AA31	IO162NB3F15	AF29
IO123NB2F11	U28	IO142PB3F13	Y31	IO162PB3F15	AE29
IO123PB2F11	T28	IO143NB3F13	AA28	IO163NB3F15	AE28
IO124NB2F11	T31	IO143PB3F13	Y28	IO163PB3F15	AD28
IO124PB2F11	T32	IO144NB3F13	AA34	IO164NB3F15	AG30
IO125NB2F11	U24	IO144PB3F13	Y34	IO164PB3F15	AF30
IO125PB2F11	U25	IO145NB3F13	AA26	IO165NB3F15	AE26
IO126NB2F11	U33	IO145PB3F13	Y26	IO165PB3F15	AD26
IO126PB2F11	U34	IO146NB3F13	AA29	IO166NB3F15	AJ30
IO127NB2F11	U26	IO146PB3F13	AA30	IO166PB3F15	AH30
IO127PB2F11	U27	IO147NB3F13	AB30	IO167NB3F15	AG28
IO128NB2F11	U31	IO147PB3F13	AB29	IO167PB3F15	AF28
IO128PB2F11	U32	IO148NB3F13	AB32	IO168NB3F15	AF27
Bank 3		IO148PB3F13	AA32	IO168PB3F15	AE27
IO129NB3F12	V29	IO149NB3F13	AB27	IO169NB3F15	AH29
IO129PB3F12	U29	IO149PB3F13	AA27	IO169PB3F15	AG29
IO130NB3F12	V31	IO150NB3F14	AC31	IO170NB3F15	AD25
IO130PB3F12	V32	IO150PB3F14	AB31	IO170PB3F15	AC25
IO131NB3F12	V24	IO151NB3F14	AD33	**Bank 4**	
IO131PB3F12	V25	IO151PB3F14	AC33	IO171NB4F16	AP29
IO132NB3F12	W28	IO152NB3F14	AC28	IO171PB4F16	AN29
IO132PB3F12	V28	IO152PB3F14	AB28	IO172NB4F16	AH26
IO133NB3F12	W26	IO153NB3F14	AB25	IO172PB4F16	AH27
IO133PB3F12	V26	IO153PB3F14	AA25	IO173NB4F16	AJ27
IO134NB3F12	W33	IO154NB3F14	AD32	IO173PB4F16	AJ28
IO134PB3F12	V33	IO154PB3F14	AC32	IO174NB4F16	AL27
IO135NB3F12	W25	IO155NB3F14	AD29	IO174PB4F16	AL28
IO135PB3F12	W24	IO155PB3F14	AC29	IO175NB4F16	AM28
IO136NB3F12	W31	IO156NB3F14	AE30	IO175PB4F16	AM29
IO136PB3F12	W32	IO156PB3F14	AD30	IO176NB4F16	AG25
IO137NB3F12	Y30	IO157NB3F14	AC26	IO176PB4F16	AG26
IO137PB3F12	W30	IO157PB3F14	AB26	IO177NB4F16	AK26

FIGURE 2. Terminal connections – Continued. 1/ 2/ 3/ 4/ 5/ 6/ 7/ 8/ 9/ 10/

Case M and T (device types 01 - 08) – Continued.

Device Types	01 - 08	Device Types	01 - 08	Device Types	01 - 08
Case Outline	M & T	Case Outline	M & T	Case Outline	M & T
Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number
IO177PB4F16	AK27	IO197PB4F18	AM22	IO217NB5F20	AM17
IO178NB4F16	AF25	IO198NB4F18	AE21	IO217PB5F20	AL17
IO178PB4F16	AE25	IO198PB4F18	AE22	IO218NB5F20	AG16
IO179NB4F16	AP28	IO199NB4F18	AJ21	IO218PB5F20	AF16
IO179PB4F16	AN28	IO199PB4F18	AJ22	IO219NB5F20	AM16
IO180NB4F16	AJ25	IO200NB4F18	AK21	IO219PB5F20	AL16
IO180PB4F16	AJ26	IO200PB4F18	AK22	IO220NB5F20	AP16
IO181NB4F17	AM26	IO201NB4F18	AM21	IO220PB5F20	AN16
IO181PB4F17	AM27	IO201PB4F18	AL21	IO221NB5F20	AN15
IO182NB4F17	AF24	IO202NB4F18	AE20	IO221PB5F20	AP15
IO182PB4F17	AE24	IO202PB4F18	AD20	IO222NB5F20	AD15
IO183NB4F17	AH24	IO203NB4F19	AN21	IO222PB5F20	AE16
IO183PB4F17	AH25	IO203PB4F19	AP21	IO223NB5F21	AL14
IO184NB4F17	AG23	IO204NB4F19	AP20	IO223PB5F21	AL15
IO184PB4F17	AG24	IO204PB4F19	AN20	IO224NB5F21	AN14
IO185NB4F17	AL25	IO205NB4F19	AN19	IO224PB5F21	AP14
IO185PB4F17	AL26	IO205PB4F19	AP19	IO225NB5F21	AK13
IO186NB4F17	AP25	IO206NB4F19	AG20	IO225PB5F21	AK14
IO186PB4F17	AP26	IO206PB4F19	AF20	IO226NB5F21	AE15
IO187NB4F17	AK24	IO207NB4F19	AL19	IO226PB5F21	AF15
IO187PB4F17	AK25	IO207PB4F19	AL20	IO227NB5F21	AG14
IO188NB4F17	AF23	IO208NB4F19	AG19	IO227PB5F21	AG15
IO188PB4F17	AE23	IO208PB4F19	AF19	IO228NB5F21	AJ13
IO189NB4F17	AN24	IO209NB4F19	AN18	IO228PB5F21	AJ14
IO189PB4F17	AM24	IO209PB4F19	AP18	IO229NB5F21	AM13
IO190NB4F17	AH22	IO210NB4F19	AE19	IO229PB5F21	AM14
IO190PB4F17	AH23	IO210PB4F19	AD19	IO230NB5F21	AE14
IO191NB4F17	AJ23	IO211NB4F19	AL18	IO230PB5F21	AF14
IO191PB4F17	AJ24	IO211PB4F19	AM18	IO231NB5F21	AN12
IO192NB4F17	AG21	IO212NB4F19/CLKEN	AJ20	IO231PB5F21	AP12
IO192PB4F17	AG22	IO212PB4F19/CLKEP	AK20	IO232NB5F21	AG13
IO193NB4F18	AP23	IO213NB4F19/CLKFN	AJ18	IO232PB5F21	AH13
IO193PB4F18	AP24	IO213PB4F19/CLKFP	AJ19	IO233NB5F21	AL12
IO194NB4F18	AN22	**Bank 5**		IO233PB5F21	AL13
IO194PB4F18	AN23	IO214NB5F20/CLKGN	AJ16	IO234NB5F21	AE13
IO195NB4F18	AM23	IO214PB5F20/CLKGP	AJ17	IO234PB5F21	AF13
IO195PB4F18	AL23	IO215NB5F20/CLKHN	AJ15	IO235NB5F22	AN11
IO196NB4F18	AF21	IO215PB5F20/CLKHP	AK15	IO235PB5F22	AP11
IO196PB4F18	AF22	IO216NB5F20	AD16	IO236NB5F22	AM11
IO197NB4F18	AL22	IO216PB5F20	AE17	IO236PB5F22	AM12

FIGURE 2. Terminal connections – Continued. 1/ 2/ 3/ 4/ 5/ 6/ 7/ 8/ 9/ 10/

Device Types	01 - 08	Device Types	01 - 08	Device Types	01 - 08
Case Outline	M & T	Case Outline	M & T	Case Outline	M & T
Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number
IO237NB5F22	AJ11	**Bank 6**		IO276PB6F25	AD2
IO237PB5F22	AJ12	IO257NB6F24	AG6	IO277NB6F25	AC4
IO238NB5F22	AH11	IO257PB6F24	AH6	IO277PB6F25	AC3
IO238PB5F22	AH12	IO258NB6F24	AD9	IO278NB6F26	AA8
IO239NB5F22	AK10	IO258PB6F24	AE9	IO278PB6F26	AA9
IO239PB5F22	AK11	IO259NB6F24	AF7	IO279NB6F26	AB5
IO240NB5F22	AE12	IO259PB6F24	AG7	IO279PB6F26	AB6
IO240PB5F22	AF12	IO260NB6F24	AH3	IO280NB6F26	Y10
IO241NB5F22	AN10	IO260PB6F24	AH4	IO280PB6F26	Y11
IO241PB5F22	AP10	IO261NB6F24	AH5	IO281NB6F26	AB3
IO242NB5F22	AG11	IO261PB6F24	AJ5	IO281PB6F26	AB4
IO242PB5F22	AG12	IO262NB6F24	AE6	IO282NB6F26	Y7
IO243NB5F22	AL9	IO262PB6F24	AF6	IO282PB6F26	AA7
IO243PB5F22	AL10	IO263NB6F24	AF5	IO283NB6F26	AC2
IO244NB5F22	AM8	IO263PB6F24	AG5	IO283PB6F26	AC1
IO244PB5F22	AM9	IO264NB6F24	AD8	IO284NB6F26	Y9
IO245NB5F23	AH10	IO264PB6F24	AE8	IO284PB6F26	Y8
IO245PB5F23	AJ10	IO265NB6F24	AF3	IO285NB6F26	AA5
IO246NB5F23	AF10	IO265PB6F24	AG3	IO285PB6F26	AA6
IO246PB5F23	AF11	IO266NB6F24	AC10	IO286NB6F26	W10
IO247NB5F23	AJ9	IO266PB6F24	AD10	IO286PB6F26	W11
IO247PB5F23	AK9	IO267NB6F25	AD7	IO287NB6F26	AA3
IO248NB5F23	AN7	IO267PB6F25	AE7	IO287PB6F26	AA4
IO248PB5F23	AP7	IO268NB6F25	AD5	IO288NB6F26	W9
IO249NB5F23	AL7	IO268PB6F25	AE5	IO288PB6F26	W8
IO249PB5F23	AL8	IO269NB6F25	AE4	IO289NB6F27	AA1
IO250NB5F23	AE10	IO269PB6F25	AF4	IO289PB6F27	AA2
IO250PB5F23	AE11	IO270NB6F25	AB9	IO290NB6F27	W6
IO251NB5F23	AK8	IO270PB6F25	AC9	IO290PB6F27	Y6
IO251PB5F23	AJ8	IO271NB6F25	AC6	IO291NB6F27	W5
IO252NB5F23	AH8	IO271PB6F25	AD6	IO291PB6F27	Y5
IO252PB5F23	AH9	IO272NB6F25	AB8	IO292NB6F27	V7
IO253NB5F23	AN6	IO272PB6F25	AC8	IO292PB6F27	W7
IO253PB5F23	AP6	IO273NB6F25	AE1	IO293NB6F27	W4
IO254NB5F23	AG9	IO273PB6F25	AE2	IO293PB6F27	Y4
IO254PB5F23	AG10	IO274NB6F25	AA10	IO294NB6F27	V10
IO255NB5F23	AJ7	IO274PB6F25	AB10	IO294PB6F27	V11
IO255PB5F23	AK7	IO275NB6F25	AB7	IO295NB6F27	Y1
IO256NB5F23	AL6	IO275PB6F25	AC7	IO295PB6F27	Y2
IO256PB5F23	AM6	IO276NB6F25	AD1	IO296NB6F27	W1

FIGURE 2. Terminal connections – Continued. 1/ 2/ 3/ 4/ 5/ 6/ 7/ 8/ 9/ 10/

Device Types	01 - 08	Device Types	01 - 08	Device Types	01 - 08
Case Outline	M & T	Case Outline	M & T	Case Outline	M & T
Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number
IO296PB6F27	W2	IO316NB7F29	R9	IO336NB7F31	K7
IO297NB6F27	V1	IO316PB7F29	R8	IO336PB7F31	L7
IO297PB6F27	V2	IO317NB7F29	N5	IO337NB7F31	G4
IO298NB6F27	V9	IO317PB7F29	P5	IO337PB7F31	G3
IO298PB6F27	V8	IO318NB7F29	R10	IO338NB7F31	K9
IO299NB6F27	U4	IO318PB7F29	R11	IO338PB7F31	L9
IO299PB6F27	V4	IO319NB7F29	L2	IO339NB7F31	H6
Bank 7		IO319PB7F29	L1	IO339PB7F31	H5
IO300NB7F28	U10	IO320NB7F29	N8	IO340NB7F31	H7
IO300PB7F28	U11	IO320PB7F29	P8	IO340PB7F31	J7
IO301NB7F28	U2	IO321NB7F30	M6	IO341NB7F31	J8
IO301PB7F28	U1	IO321PB7F30	N6	IO341PB7F31	K8
IO302NB7F28	U6	IO322NB7F30	P10	**Dedicated I/O**	
IO302PB7F28	U7	IO322PB7F30	P9	GND	A13
IO303NB7F28	T3	IO323NB7F30	L3	GND	A2
IO303PB7F28	U3	IO323PB7F30	M3	GND	A22
IO304NB7F28	U9	IO324NB7F30	M7	GND	A27
IO304PB7F28	U8	IO324PB7F30	N7	GND	A3
IO305NB7F28	R2	IO325NB7F30	K2	GND	A31
IO305PB7F28	R1	IO325PB7F30	K1	GND	A32
IO306NB7F28	R4	IO326NB7F30	G2	GND	A33
IO306PB7F28	T4	IO326PB7F30	H2	GND	A4
IO307NB7F28	R5	IO327NB7F30	L6	GND	A8
IO307PB7F28	T5	IO327PB7F30	L5	GND	AA14
IO308NB7F28	T11	IO328NB7F30	N10	GND	AA15
IO308PB7F28	T10	IO328PB7F30	N9	GND	AA16
IO309NB7F28	T6	IO329NB7F30	J4	GND	AA17
IO309PB7F28	T7	IO329PB7F30	K4	GND	AA18
IO310NB7F29	T9	IO330NB7F30	J5	GND	AA19
IO310PB7F29	T8	IO330PB7F30	K5	GND	AA20
IO311NB7F29	N3	IO331NB7F30	M10	GND	AA21
IO311PB7F29	P3	IO331PB7F30	M9	GND	AB1
IO312NB7F29	P7	IO332NB7F31	L8	GND	AB13
IO312PB7F29	R7	IO332PB7F31	M8	GND	AB22
IO313NB7F29	P6	IO333NB7F31	F2	GND	AB34
IO313PB7F29	R6	IO333PB7F31	F1	GND	AC12
IO314NB7F29	M2	IO334NB7F31	J6	GND	AC23
IO314PB7F29	N2	IO334PB7F31	K6	GND	AC30
IO315NB7F29	N4	IO335NB7F31	H4	GND	AC5
IO315PB7F29	P4	IO335PB7F31	H3	GND	AD11

FIGURE 2. Terminal connections – Continued. 1/ 2/ 3/ 4/ 5/ 6/ 7/ 8/ 9/ 10/

Device Types	01 - 08	Device Types	01 - 08	Device Types	01 - 08	Device Types	01 - 08
Case Outline	M & T	Case Outline	M & T	Case Outline	M & T	Case Outline	M & T
Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number
GND	AD24	GND	AM33	GND	C31	GND	M5
GND	AD31	GND	AM34	GND	C32	GND	N1
GND	AD4	GND	AM4	GND	C33	GND	N13
GND	AE3	GND	AN1	GND	C34	GND	N22
GND	AE32	GND	AN2	GND	C4	GND	N34
GND	AF2	GND	AN26	GND	D1	GND	P14
GND	AF33	GND	AN3	GND	D11	GND	P15
GND	AG1	GND	AN31	GND	D2	GND	P16
GND	AG27	GND	AN32	GND	D24	GND	P17
GND	AG34	GND	AN33	GND	D3	GND	P18
GND	AG8	GND	AN34	GND	D31	GND	P19
GND	AH28	GND	AN4	GND	D32	GND	P20
GND	AH7	GND	AN9	GND	D33	GND	P21
GND	AJ29	GND	AP13	GND	D34	GND	R14
GND	AJ6	GND	AP2	GND	D4	GND	R15
GND	AK12	GND	AP22	GND	E12	GND	R16
GND	AK17	GND	AP27	GND	E17	GND	R17
GND	AK18	GND	AP3	GND	E18	GND	R18
GND	AK23	GND	AP31	GND	E23	GND	R19
GND	AK30	GND	AP32	GND	E30	GND	R20
GND	AK5	GND	AP33	GND	E5	GND	R21
GND	AL1	GND	AP4	GND	F29	GND	R3
GND	AL11	GND	AP8	GND	F30	GND	R32
GND	AL2	GND	B1	GND	F6	GND	T14
GND	AL24	GND	B2	GND	G28	GND	T15
GND	AL3	GND	B26	GND	G6	GND	T16
GND	AL31	GND	B3	GND	G7	GND	T17
GND	AL32	GND	B31	GND	H1	GND	T18
GND	AL33	GND	B32	GND	H34	GND	T19
GND	AL34	GND	B33	GND	J2	GND	T20
GND	AL4	GND	B34	GND	J33	GND	T21
GND	AM1	GND	B4	GND	K3	GND	U14
GND	AM10	GND	B9	GND	K32	GND	U15
GND	AM15	GND	C1	GND	L11	GND	U16
GND	AM2	GND	C10	GND	L24	GND	U17
GND	AM20	GND	C15	GND	L31	GND	U18
GND	AM25	GND	C2	GND	L4	GND	U19
GND	AM3	GND	C20	GND	M12	GND	U20
GND	AM31	GND	C25	GND	M23	GND	U21
GND	AM32	GND	C3	GND	M30	GND	U30

FIGURE 2. Terminal connections – Continued. 1/ 2/ 3/ 4/ 5/ 6/ 7/ 8/ 9/ 10/

Device Types	01 - 08	Device Types	01 - 08	Device Types	01 - 08	Device Types	01 - 08
Case Outline	M & T	Case Outline	M & T	Case Outline	M & T	Case Outline	M & T
Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number
GND	U5	NC	AE34	NC	D23	TDI	F7
GND	V14	NC	AF1	NC	D25	TDO	L10
GND	V15	NC	AF17	NC	F3	TMS	H8
GND	V16	NC	AF18	NC	F32	TRST	E6
GND	V17	NC	AF34	NC	F33	VCCA	AA13
GND	V18	NC	AG2	NC	F34	VCCA	AA22
GND	V19	NC	AG4	NC	F4	VCCA	AB14
GND	V20	NC	AH1	NC	G1	VCCA	AB15
GND	V21	NC	AH16	NC	G32	VCCA	AB16
GND	V30	NC	AH19	NC	G33	VCCA	AB17
GND	V5	NC	AH2	NC	G34	VCCA	AB18
GND	W14	NC	AH31	NC	H16	VCCA	AB19
GND	W15	NC	AH32	NC	H19	VCCA	AB20
GND	W16	NC	AH34	NC	H31	VCCA	AB21
GND	W17	NC	AJ1	NC	H33	VCCA	AF8
GND	W18	NC	AJ2	NC	J1	VCCA	AK28
GND	W19	NC	AJ3	NC	J16	VCCA	G30
GND	W20	NC	AJ31	NC	J19	VCCA	G5
GND	W21	NC	AJ32	NC	J3	VCCA	N14
GND	Y14	NC	AJ33	NC	J34	VCCA	N15
GND	Y15	NC	AJ34	NC	K17	VCCA	N16
GND	Y16	NC	AJ4	NC	K18	VCCA	N17
GND	Y17	NC	AK16	NC	L17	VCCA	N18
GND	Y18	NC	AK19	NC	L18	VCCA	N19
GND	Y19	NC	AL29	NC	M1	VCCA	N20
GND	Y20	NC	AM19	NC	M4	VCCA	N21
GND	Y21	NC	AM7	NC	P1	VCCA	P13
GND	Y3	NC	AN13	NC	P2	VCCA	P22
GND	Y32	NC	AN17	NC	R31	VCCA	R13
NC	A17	NC	AN25	NC	T1	VCCA	R22
NC	A26	NC	AN27	NC	T2	VCCA	T13
NC	AB2	NC	AN8	NC	V3	VCCA	T22
NC	AB33	NC	AP17	NC	V34	VCCA	U13
NC	AC34	NC	AP9	NC	W3	VCCA	U22
NC	AD17	NC	B17	NC	W34	VCCA	V13
NC	AD3	NC	B22	PRA	J17	VCCA	V22
NC	AD34	NC	B27	PRB	F18	VCCA	W13
NC	AE18	NC	B8	PRC	AD18	VCCA	W22
NC	AE31	NC	D10	PRD	AH18	VCCA	Y13
NC	AE33	NC	D20	TCK	J9	VCCA	Y22

FIGURE 2. Terminal connections – Continued. 1/ 2/ 3/ 4/ 5/ 6/ 7/ 8/ 9/ 10/

Device Types	01 - 08	Device Types	01 - 08	Device Types	01 - 08	Device Types	01 - 08
Case Outline	M & T	Case Outline	M & T	Case Outline	M & T	Case Outline	M & T
Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number
VCCDA	AF26	VCCIB1	L21	VCCIB4	AL30	VPUMP	J26
VCCDA	AF9	VCCIB1	L22	VCCIB4	AM30		
VCCDA	AG17	VCCIB1	L23	VCCIB4	AN30		
VCCDA	AG18	VCCIB1	M18	VCCIB4	AP30		
VCCDA	AH14	VCCIB1	M19	VCCIB5	AC13		
VCCDA	AH15	VCCIB1	M20	VCCIB5	AC14		
VCCDA	AH17	VCCIB1	M21	VCCIB5	AC15		
VCCDA	AH20	VCCIB1	M22	VCCIB5	AC16		
VCCDA	AH21	VCCIB2	E31	VCCIB5	AC17		
VCCDA	AK29	VCCIB2	E32	VCCIB5	AD12		
VCCDA	AK6	VCCIB2	E33	VCCIB5	AD13		
VCCDA	E15	VCCIB2	E34	VCCIB5	AD14		
VCCDA	E29	VCCIB2	M24	VCCIB5	AL5		
VCCDA	E7	VCCIB2	N23	VCCIB5	AM5		
VCCDA	F15	VCCIB2	N24	VCCIB5	AN5		
VCCDA	F21	VCCIB2	P23	VCCIB5	AP5		
VCCDA	F5	VCCIB2	P24	VCCIB6	AA11		
VCCDA	G20	VCCIB2	R23	VCCIB6	AA12		
VCCDA	H17	VCCIB2	T23	VCCIB6	AB11		
VCCDA	H18	VCCIB2	U23	VCCIB6	AB12		
VCCDA	H28	VCCIB3	AA23	VCCIB6	AC11		
VCCDA	J18	VCCIB3	AA24	VCCIB6	AK1		
VCCDA	V27	VCCIB3	AB23	VCCIB6	AK2		
VCCDA	V6	VCCIB3	AB24	VCCIB6	AK3		
VCCIB0	A5	VCCIB3	AC24	VCCIB6	AK4		
VCCIB0	B5	VCCIB3	AK31	VCCIB6	V12		
VCCIB0	C5	VCCIB3	AK32	VCCIB6	W12		
VCCIB0	D5	VCCIB3	AK33	VCCIB6	Y12		
VCCIB0	L12	VCCIB3	AK34	VCCIB7	E1		
VCCIB0	L13	VCCIB3	V23	VCCIB7	E2		
VCCIB0	L14	VCCIB3	W23	VCCIB7	E3		
VCCIB0	M13	VCCIB3	Y23	VCCIB7	E4		
VCCIB0	M14	VCCIB4	AC18	VCCIB7	M11		
VCCIB0	M15	VCCIB4	AC19	VCCIB7	N11		
VCCIB0	M16	VCCIB4	AC20	VCCIB7	N12		
VCCIB0	M17	VCCIB4	AC21	VCCIB7	P11		
VCCIB1	A30	VCCIB4	AC22	VCCIB7	P12		
VCCIB1	B30	VCCIB4	AD21	VCCIB7	R12		
VCCIB1	C30	VCCIB4	AD22	VCCIB7	T12		
VCCIB1	D30	VCCIB4	AD23	VCCIB7	U12		

FIGURE 2. Terminal connections – Continued. 1/ 2/ 3/ 4/ 5/ 6/ 7/ 8/ 9/ 10/

1/ IO pin naming scheme shows which bank an I/O belongs, and the pairing and pin polarity for differential I/Os:

"IO**XX**YBℤ*FG*": **XX(X)*** is the I/O pair number, starting with "**00**"; Y is "P" = Positive Pin or "N" = Negative pin;

ℤ is the I/O bank ID (0 – 7); *FG* can be ignored (not used)

Note: * the third **X** denotes I/O numbers greater than 99.
a slash / provides a division of the IO naming scheme as indicated below

"IO**XX**YBℤ*FG*" / Special_Function_Name": This pin can be configured as an I/O pin or a special function pin.

2/ HCLKA/B/C/D are the clock inputs for sequential modules, they are directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. HCLKE/F/G/H are the clock inputs for clock distribution networks, they are buffered prior to clocking the R-cells. All clock pins (HCLKA/B/C/D, CLKE/F/G/H) are compatible with all supported I/O standards, when they are used with single-ended I/O standard, they must be tied to the P-pads of the clock package pins, and the N-pads can be used as user I/Os. When any of the HCLKA/B/C/D pins are not used either as clock or I/O pins, they shall be tied to Ground. When any of the CLKE/F/G/H pins are not used either as clock or I/O pins, they shall be tied to a known state.

3/ V_{CCIBX} is the supply voltage for I/O, BX is the I/O bank ID (0-7).
Unused I/O banks may be tied to GND or can be tied to other used I/O banks within the same device.

4/ V_{CCDA} is the supply voltage for the I/O differential amplifier, JTAG and Probe interfaces. V_{CCDA} is either 3.3V or 2.5V, and must be 3.3V when voltage-referenced and/or differential IO are used. Additionally, V_{CCDA} must be greater than or equal to any V_{CCI} voltages (i.e. $V_{CCDA} \geq V_{CCIBX}$)

5/ JTAG interface (include TMS, TDI, TCK, TRST, and TDO pins) is compliant with the IEEE 1149.1 standard, except for the device ID length, which is 33 bits.

6/ Probe pins (PRA, PRB, PRC, PRD) are used to bring out up to four individual signals inside the device without disturbing normal device operation to allow real time diagnostics. The probe circuitry is accessed and controlled via manufacturer's Silicon Explorer II tool and communicates with the device via the JTAG port.

7/ JTAG and Probe pins should be configured for flight as below:

Pin Name	Configurations
TCK	Can be hardwired to V_{CCDA} or Ground, or can be driven to V_{CCDA} or Ground, and TCK pin must not be left un-terminated
TDO	Must be left un-connected
TDI, TMS	Can be hardwired or driven to V_{CCDA}, or can be left unconnected (equipped with 10kΩ internal pull-up resistor)
TRST	Must be hardwired to ground (Optional 10kΩ internal pull-up resistor can be set by user at programming. Care should be exercised when using this option in combination with an external tie-off to ground)
PRA, PRB PRC, PRD	Must be left unconnected

8/ V_{PUMP} is used to access an external charge pump by bypassing internal charge pump to reduce power consumption. When V_{PUMP} voltage level is set to 3.3V, the device will use V_{PUMP} voltage as the charge pump voltage and the internal charge pump will be turned off. Adequate voltage regulation (i.e., high drive, low output impedance, and good decoupling) shall be used for V_{PUMP} shall be directly tied or through a 1kΩ resistor to the Ground.

FIGURE 2. Terminal connections – Continued.

9/ N/C is No-Connect pin, it is not connected to circuitry within the device, and can be driven to any voltage or be left floating with no effect on the operation of the device.

10/ I/O Customizations: By utilizing manufacturer's Designer software (see 6.7 herein), the following I/O features can be customized:

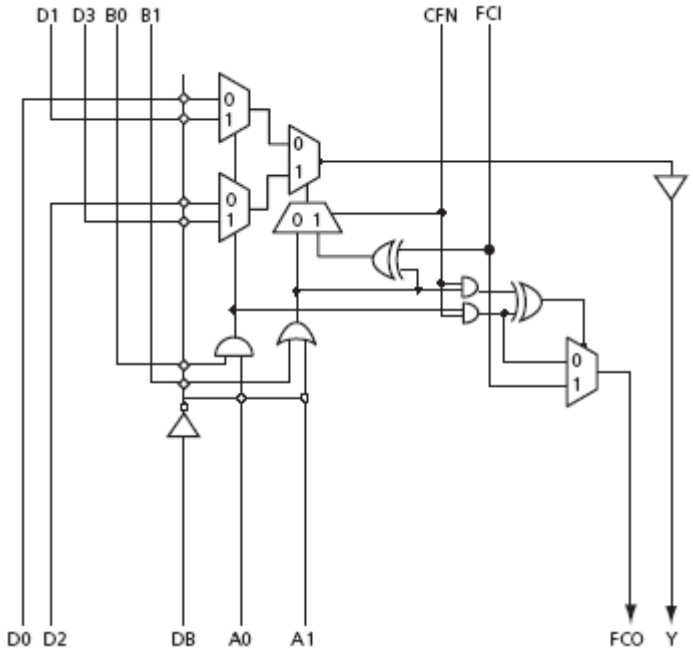
Bank-Wide Programmable Input Delays: A five-bit programmable input delay element is associated with each I/O. The value of this delay is set on a bank-wide basis. It is optional for each input buffer within the bank (i.e. the user can enable or disable the delay element for the I/O). The default setting for this property can be set in Manufacturer's Designer software. When the input buffer drives a register within the I/O, the delay element is activated by default to ensure a zero hold-time. When the input buffer does not drive a register, the delay element is deactivated to provide higher performance.

Slew-Rate and Drive Strength for LVTTL Output Buffer: By using Manufacturer's Designer software, the slew-rate value for the LVTTL output buffer can be programmed and can be set to either slow or fast. The drive strength value for LVTTL output buffer can also be programmed to four different drive strength values (8mA, 12mA, 16mA, or 24mA).

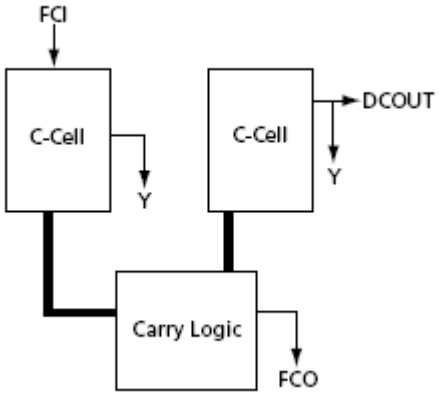
Other I/O types and features: Differential I/O standards, voltage-referenced I/O standards, Double Data Rate (DDR), access to I/O registers, using weak pull-up and pull-down resistors can be instantiated through using I/O macros in manufacturer's Designer software.

FIGURE 2. Terminal connections – Continued.

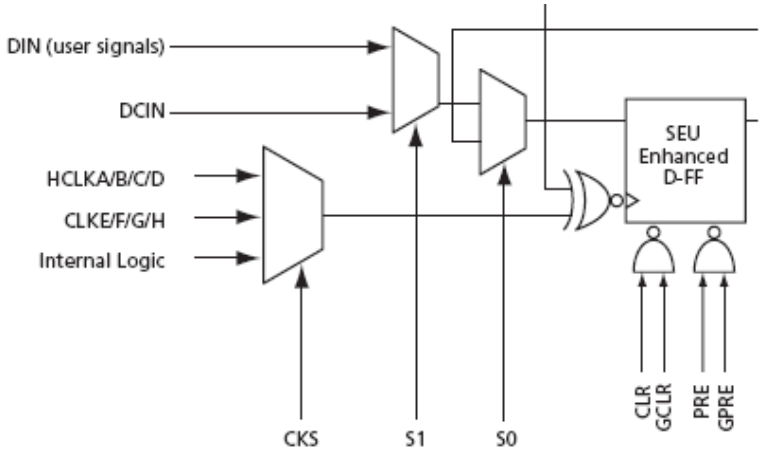
Logic Block Diagram for C-Cell



C-Cells with 2-bit Carry Logic



Logic Block Diagram for R-Cell



R-Cell Implementation of D Flip-Flop

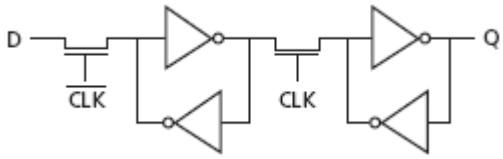
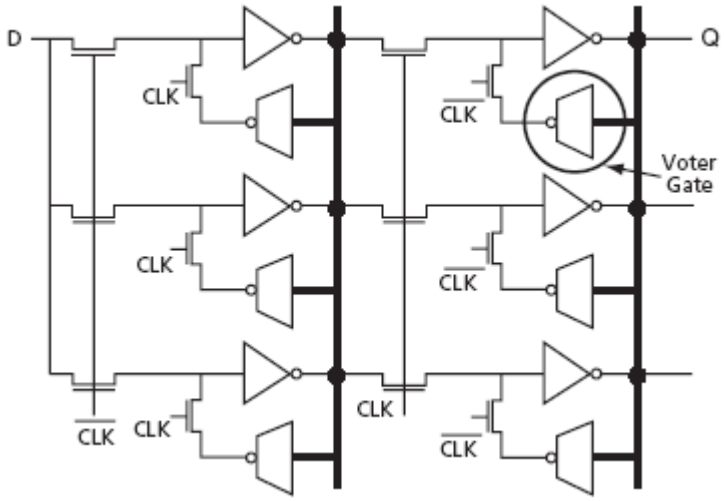
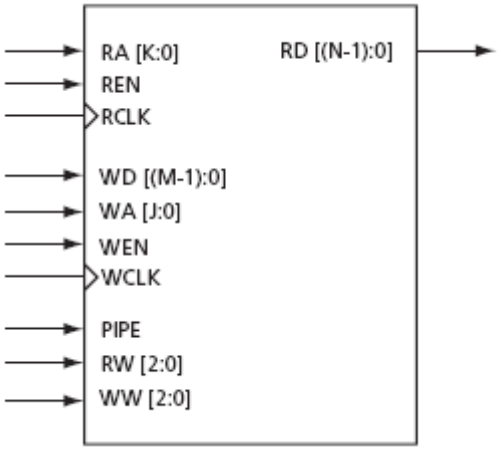


FIGURE 3. Logic Block Diagrams.

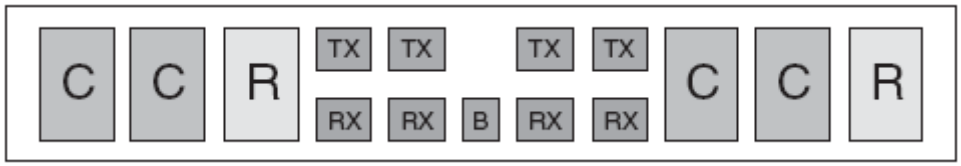
TMR R-cell Implementation of D Flip-Flop Using Voter



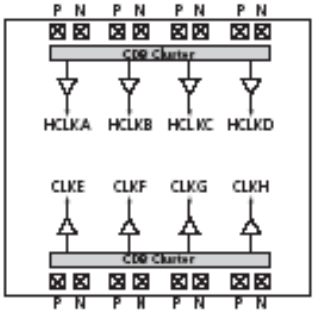
RAM Block



Super Cluster



Global Clocks



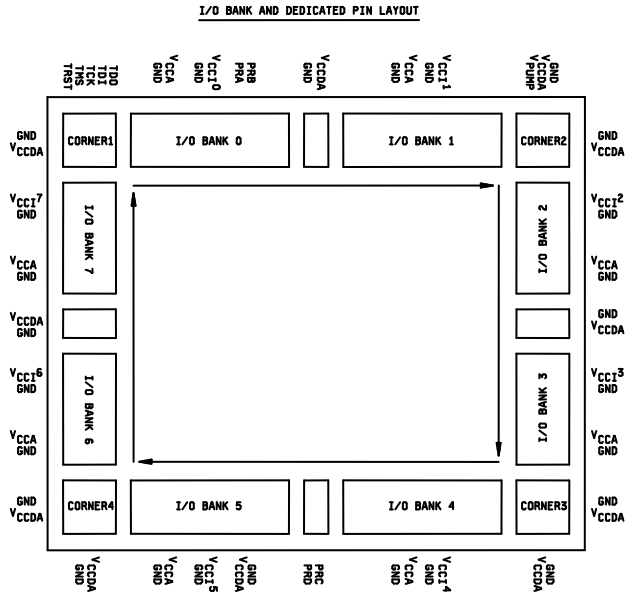
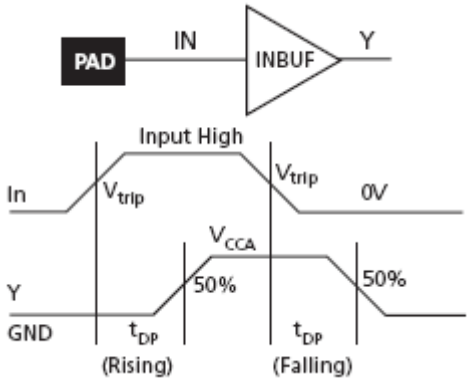
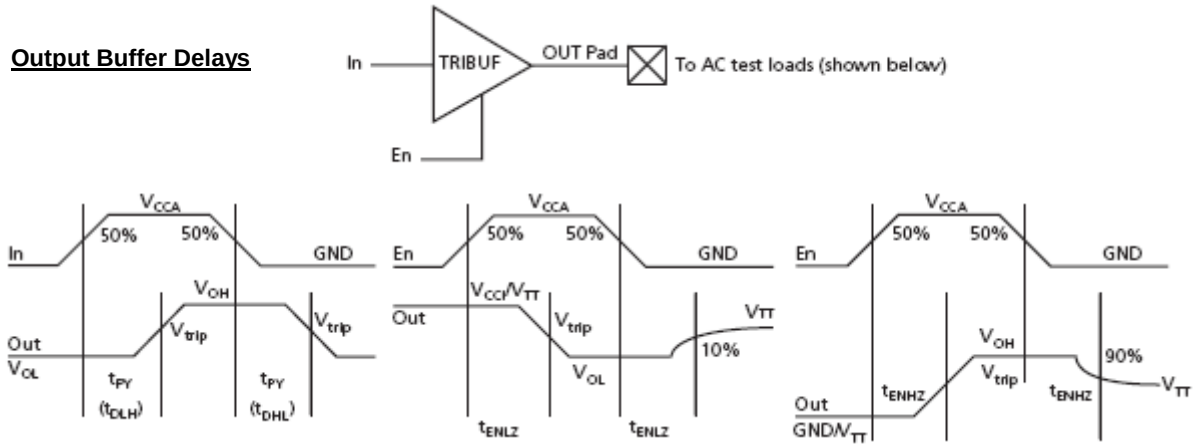


FIGURE 3. Logic Block Diagrams - Continued.

Input Buffer Delays



Output Buffer Delays



I/O Module

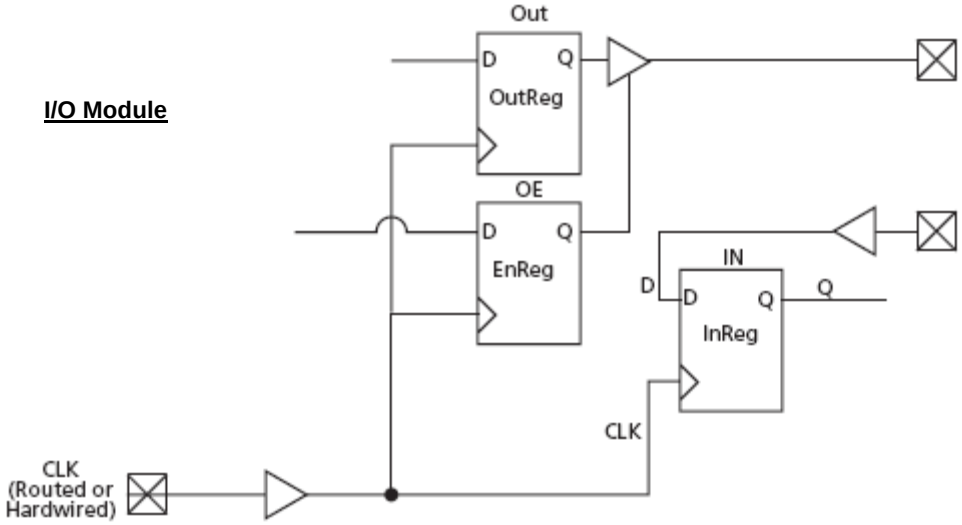


FIGURE 3. Logic Block Diagrams - Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Constant acceleration method 2001 of MIL-STD-883 shall be performed to condition B for devices built with case outline X, Y, Z, U, M, T, and N.

c. Binning program performed prior to burn-in.

d. Interim and final electrical test parameters shall be as specified in table IIA herein.

e. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

f. Additional screening for devices 03, 04, 07, 08, 11, 12, 15 and 16 shall include:

(1) Internal visual, TM 2010 condition A

(2) 100% x-ray (top view only)

(3) 100% PIND (PIND is included for all devices (01 through 16))

(4) Serialization (Serialization is included for all devices (01 through 16))

(5) Static Burn-in, delta, read and record, PDA (3% functional)

(6) Seal Fine Gross Leak Test

(7) Lot specific group B with RGA

g. Devices built with case outlines Z, T, and N are equivalent to the same device built with case outline Y and M plus the solder column attachment. All required screening for devices built with case outline Z, T, and N are processed prior to the solder column attachment (same as case outline Y and M). After solder column attachment, Group A subgroups 1 and 7 shall be performed to verify device functionality.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency equal or less than 1 MHz. Sample size is on a minimum of three devices with no failures on a minimum of five worst case pins from each device.

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's technical review board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on a minimum of three devices with zero failures. Latch-up test shall be considered destructive. Information contained in JESD 78 may be used for reference.

e. Programmed device (see 3.2.3.2) - For device classes Q and V, subgroups 7, 8A, and 8B shall include verifying the functionality of the device.

f. Unprogrammed devices shall be tested for programmability and dc and ac performance compliance to the requirements of group A, subgroups 1 and 7. The programming procedure used and the data generated shall be maintained by the device manufacturer and shall be made available to the preparing or acquiring activities.

Note: The following steps are done prior to burn-in screening.

(1) Programming requirements shall be based on wafer lot and the Enhanced Lot Acceptance (ELA) design shall be used. Sample size shall achieve 14 programmed devices with the maximum of five allowable programming failures 19(5). In the occurrence of six or more programming failures, the wafer lot shall be put on hold until its programmability can be resolved, otherwise, the wafer lot shall be designated to be programmed by manufacturer only and be delivered to acquiring activities accepting lower programming yield.

Note: Programming reliability is determined by programming algorithm (see 4.6 below), all parts passed programming shall be considered as reliable since it is verified with ELA; and programming yield shall not be used as a reliability indicator. Field programming yield cannot be guaranteed, and manufacturer will replace all field programming rejects when the provided manufacturer's programming procedure is followed.

(2) Retesting of devices due to failure shall be in accordance with the manufacture's Quality Control Monitor (QCMON) for the purpose of determining the failure as True or False as defined in the QCMON.

(3) The 14 programmed devices shall be subjected to burn-in for 168 hours at T_A = +125°C. If any functional or parametric failures are detected during pre and post burn-in tests, TRB shall review the FA results to reject the wafer lot, repeat the test after corrective actions, or request for additional testing with no additional failures.

(4) In addition to the 168 hours of burn-in, two ELA programmed devices shall be characterized for thermal stability at an ambient temperature up to 135°C, by measuring I_{CC} current immediately after oven has reached the specified temperature and again 40 minutes later. Wafer lots that exhibits thermal runaway (when I_{CC} current rapidly increases without bound) shall be rejected. (Note: This is a new test implemented with wafer lots fabricated in 2007 and beyond).

g. Two dice are sampled from each wafer. The dice are cross sectioned at the programmable element (antifuse) and a sample of electron micrographs (XSEM) are inspected. All wafers passing XSEM inspection are ELA processed. Any construction issues observed will result in the wafer in question being quarantined until its reliability can be assured by conducting ELA testing (see 4.4.1.f.(1) herein) with devices from the quarantined wafers. XSEM micrographs and inspection report data shall be maintained by the device manufacturer and shall be made available to the preparing or acquiring activities.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Additional reliability qualification test (Enhanced Antifuse Qualification or EAQ) for the programmable element (antifuse) shall be required for initial qualification and after any process (including programming algorithm) or design changes which may affect the reliability of the programmable element (antifuse). The test data shall be maintained by the manufacturer and shall be made available to the preparing or acquiring activity upon request.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883. Group C sample size will be 22(0).

a. T_A = +125°C, minimum.

b. Test duration: 1000 hours for class Q and 2000 hours for class V.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

a. Constant acceleration method 2001 of MIL-STD-883 shall be performed to condition B for devices built with case outlines X, Y, Z, U, M, T, and N.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

4.4.5 Additional criteria for conformance inspection. All required conformance inspection for devices built with case outline Z, T, and N are processed without the solder column attachment (same as case outline Y and M).

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/ 8/

Line no.	Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class Q	Device class V
1	Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9
2	Static burn-in (method 1015)	Not required	Required
3	Same as line 1		1*Δ, 7*
4	Dynamic burn-in (method 1015)	Required	Required
5	Same as line 1		1*Δ, 7*
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1Δ, 2, 3, 7, 8A, 8B, 9, 10, 11
9	Group D end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7, 8A, and 8B functional tests shall verify the functionality for unprogrammed devices or that the altered item drawing pattern exists for programmed devices.
4/ * indicates PDA applies to subgroups 1 and 7.
5/ ** see 4.4.1c.
6/ Δ indicates delta limit (see table IIB) shall be required and the delta values shall be computed with reference to the previous interim electrical parameters.
7/ See 4.4.1d.
8/ Device 05 – 08 are selected items at line number 6. (Final electrical parameters).

TABLE IIB. Delta limits at +25°C for burn-in and lifetest.

Parameter 1/	Device types
	ALL
I_{CCA}	± 10 mA of measured value in table I
I_{CCI}	± 2.5 mA of measured value in table I
I_{CCDA}	± 1 mA of measured value in table I
I_{IL} / I_{IH} 2/	± 0.3 μA of measured value in table I
I_{IL} / I_{IH} 3/ (w. Pull_Up and Pull Down resistor options)	± 25 μA
BIN_FAST / BIN_SLOW 4/ 5/	± 300 ns

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta (Δ).

2/ The I_{IL} / I_{IH} are measured for blank devices. Measurement is made with I/O configured as LVTTL. Programmed devices without the optional pull-up and pull-down resistors also comply with this limit.

3/ For programmed devices with the optional pull-up and pull-down resistors selected.

I_{IL} / I_{IH} parametric limits shown in table I are without the optional pull-up and pull-down resistors selected, to calculate I_{IL} / I_{IH} with optional pull-up and pull-down resistors selected, use the table below:

Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values				
I/O Configuration (V_{CCI})	R (Pull-Up, kΩ[2])		R (Pull-Down, kΩ[2])	
	Min.	Max.	Min.	Max.
3.3V	35	65	30	60
2.5V	50	75	40	85
1.8V	80	140	70	130
1.5V	100	210	90	180

These maximum values are provided for informational reasons only.

$R_{PULL\text{-}DOWN\text{-}MAX} = V_{OLspec} / I_{OLspec}$

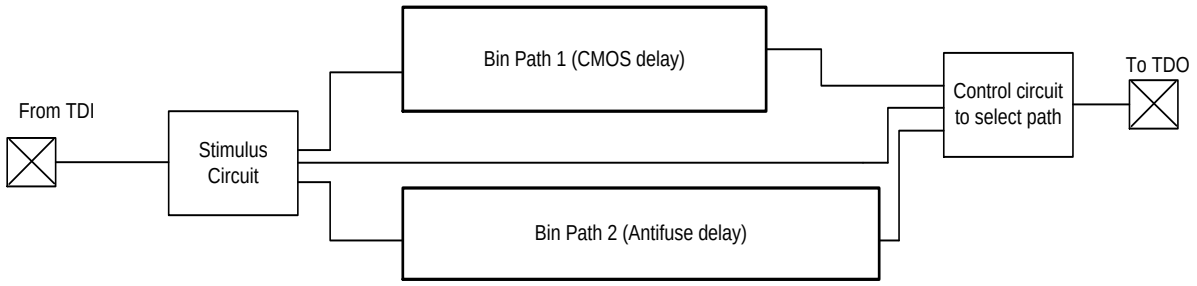
$R_{PULL\text{-}UP\text{-}MAX} = (V_{CCImax} – V_{OHspec}) / I_{OHspec}$

Minimum output buffer resistance values depend on V_{CCI}, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the manufacturer's website (see 6.7 herein).

Continued on next page…

TABLE IIB. Delta limits at +25ºC for burn-in and lifetest - Continued.

4/ The binning circuit has two different paths to measure the delay due to antifuse contribution and transistor contribution. Below shows a simplified schematic of the two binning circuit paths used to measure and characterize speed grades by comparing to timing models.



The "Bin Path 1 (BIN_FAST)" path is composed of inverter chains to measure the delay due to transistors. The "Bin Path 2 (BIN_SLOW)" path is mainly composed of metal tracks connected to ground via un-programmed antifuses to emulate capacitive loading due to antifuses. In addition to the antifuse capacitive loading, the "Bin Path 2" also has in series to the path, a fixed amount of antifuses that get programmed to emulate delays of programmed antifuses.

5/ Binning circuit measurement is done by applying stimulus signals through the TDI pin. The stimulus circuit will apply the necessary signals to toggle one path and output the signal to TDO pin. A formula is extracted by correlating the measured bin speeds of the two binning circuit paths and the characterization data. For each device, during the speed grading in the screening process, the BIN_FAST and BIN_SLOW measurement are used by the formula to determine the speed grade of each part.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

4.6 Programming procedures. Programming support is provided through manufacturer's programming software (see 6.7 herein), a single-sited programmer controlled from a PC with manufacturer's programming software. During programming, each antifuse is programmed and verified by the programming algorithm to ensure correct programming. At the end of the programming, there are integrity tests to ensure that programming is completed properly. The programming procedure is specified by the manufacturer and available at manufacturer's website. The programming procedures shall be maintained by the manufacturer and shall be made available to the preparing or acquiring activity upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Design characteristics. The complexity of the devices covered by this document will require the user/designer to be familiar with additional design characteristics of the device. Contact the manufacturer for design and functional support. Updated versions of device manufacturer's software, device data sheet, IBIS models, and application notes may be obtained directly from device manufacturer's website.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 12-11-09

Approved sources of supply for SMD 5962-04221 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-0422101QMC	0J4Z0	RTAX2000S-LG1152B
5962-0422101QNA	0J4Z0	RTAX2000S-CGS624B
5962-0422101QTA	0J4Z0	RTAX2000S-CG1152B
5962-0422101QUC	0J4Z0	RTAX2000S-CQ256B
5962-0422101QXC	0J4Z0	RTAX2000S-CQ352B
5962-0422101QYC	0J4Z0	RTAX2000S-LG624B
5962-0422101QZA	3/	RTAX2000S-CGB624B
5962-0422101VMC	0J4Z0	RTAX2000S-LG1152V
5962-0422101VNA	0J4Z0	RTAX2000S-CGS624V
5962-0422101VTA	0J4Z0	RTAX2000S-CG1152V
5962-0422101VUC	0J4Z0	RTAX2000S-CQ256V
5962-0422101VXC	0J4Z0	RTAX2000S-CQ352V
5962-0422101VYC	0J4Z0	RTAX2000S-LG624V
5962-0422102QMC	0J4Z0	RTAX2000S-1LG1152B
5962-0422102QNA	0J4Z0	RTAX2000S-1CGS624B
5962-0422102QTA	0J4Z0	RTAX2000S-1CG1152B
5962-0422102QUC	0J4Z0	RTAX2000S-1CQ256B
5962-0422102QXC	0J4Z0	RTAX2000S-1CQ352B
5962-0422102QYC	0J4Z0	RTAX2000S-1LG624B
5962-0422102QZA	3/	RTAX2000S-1CGB624B
5962-0422102VMC	0J4Z0	RTAX2000S-1LG1152V
5962-0422102VNA	0J4Z0	RTAX2000S-1CGS624V
5962-0422102VTA	0J4Z0	RTAX2000S-1CG1152V
5962-0422102VUC	0J4Z0	RTAX2000S-1CQ256V
5962-0422102VXC	0J4Z0	RTAX2000S-1CQ352V
5962-0422102VYC	0J4Z0	RTAX2000S-1LG624V
5962-0422103QMC	0J4Z0	RTAX2000S-LG1152E
5962-0422103QNA	0J4Z0	RTAX2000S-CGS624E
5962-0422103QTA	0J4Z0	RTAX2000S-CG1152E

See notes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-0422103QUC	0J4Z0	RTAX2000S-CQ256E
5962-0422103QXC	0J4Z0	RTAX2000S-CQ352E
5962-0422103QYC	0J4Z0	RTAX2000S-LG624E
5962-0422103QZA	3/	RTAX2000S-CGB624E
5962-0422104QMC	0J4Z0	RTAX2000S-1LG1152E
5962-0422104QNA	0J4Z0	RTAX2000S-1CGS624E
5962-0422104QTA	0J4Z0	RTAX2000S-1CG1152E
5962-0422104QUC	0J4Z0	RTAX2000S-1CQ256E
5962-0422104QXC	0J4Z0	RTAX2000S-1CQ352E
5962-0422104QYC	0J4Z0	RTAX2000S-1LG624E
5962-0422104QZA	3/	RTAX2000S-1CGB624E
5962-0422105QMC	0J4Z0	RTAX2000SL-LG1152B
5962-0422105QNA	0J4Z0	RTAX2000SL-CGS624B
5962-0422105QTA	0J4Z0	RTAX2000SL-CG1152B
5962-0422105QUC	0J4Z0	RTAX2000SL-CQ256B
5962-0422105QXC	0J4Z0	RTAX2000SL-CQ352B
5962-0422105QYC	0J4Z0	RTAX2000SL-LG624B
5962-0422105VMC	0J4Z0	RTAX2000SL-LG1152V
5962-0422105VNA	0J4Z0	RTAX2000SL-CGS624V
5962-0422105VTA	0J4Z0	RTAX2000SL-CG1152V
5962-0422105VUC	0J4Z0	RTAX2000SL-CQ256V
5962-0422105VXC	0J4Z0	RTAX2000SL-CQ352V
5962-0422105VYC	0J4Z0	RTAX2000SL-LG624V
5962-0422106QMC	0J4Z0	RTAX2000SL-1LG1152B
5962-0422106QNA	0J4Z0	RTAX2000SL-1CGS624B
5962-0422106QTA	0J4Z0	RTAX2000SL-1CG1152B
5962-0422106QUC	0J4Z0	RTAX2000SL-1CQ256B
5962-0422106QXC	0J4Z0	RTAX2000SL-1CQ352B
5962-0422106QYC	0J4Z0	RTAX2000SL-1LG624B
5962-0422106VMC	0J4Z0	RTAX2000SL-1LG1152V
5962-0422106VNA	0J4Z0	RTAX2000SL-1CGS624V
5962-0422106VTA	0J4Z0	RTAX2000SL-1CG1152V
5962-0422106VUC	0J4Z0	RTAX2000SL-1CQ256V
5962-0422106VXC	0J4Z0	RTAX2000SL-1CQ352V

See notes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-0422106VYC	0J4Z0	RTAX2000SL-1LG624V
5962-0422107QMC	0J4Z0	RTAX2000SL-LG1152E
5962-0422107QNA	0J4Z0	RTAX2000SL-CGS624E
5962-0422107QTA	0J4Z0	RTAX2000SL-CG1152E
5962-0422107QUC	0J4Z0	RTAX2000SL-CQ256E
5962-0422107QXC	0J4Z0	RTAX2000SL-CQ352E
5962-0422107QYC	0J4Z0	RTAX2000SL-LG624E
5962-0422108QMC	0J4Z0	RTAX2000SL-1LG1152E
5962-0422108QNA	0J4Z0	RTAX2000SL-1CGS624E
5962-0422108QTA	0J4Z0	RTAX2000SL-1CG1152E
5962-0422108QUC	0J4Z0	RTAX2000SL-1CQ256E
5962-0422108QXC	0J4Z0	RTAX2000SL-1CQ352E
5962-0422108QYC	0J4Z0	RTAX2000SL-1LG624E
5962-0422109QXC	0J4Z0	RTAX2000D-CQ352B
5962-0422109VXC	0J4Z0	RTAX2000D-CQ352V
5962-0422110QXC	0J4Z0	RTAX2000D-1CQ352B
5962-0422110VXC	0J4Z0	RTAX2000D-1CQ352V
5962-0422111QXC	0J4Z0	RTAX2000D-CQ352E
5962-0422112QXC	0J4Z0	RTAX2000D-1CQ352E
5962-0422113QXC	0J4Z0	RTAX2000DL-CQ352B
5962-0422113VXC	0J4Z0	RTAX2000DL-CQ352V
5962-0422114QXC	0J4Z0	RTAX2000DL-1CQ352B
5962-0422114VXC	0J4Z0	RTAX2000DL-1CQ352V
5962-0422115QXC	0J4Z0	RTAX2000DL-CQ352E
5962-0422116QXC	0J4Z0	RTAX2000DL-1CQ352E

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source.

Vendor CAGE number	Vendor name and address
0J4Z0	Actel Corporation 2061 Stierlin Court. Mountain View, CA 94043