REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add five vendors, CAGE 61772, CAGE 04713, CAGE 60991, CAGE 50088, and CAGE 65786. Add 04 new device types. Add case outline letter Y.	88-06-17	Michael A. Frye
B	Boilerplate update, part of 5 year review. ksr	05-09-29	Raymond Monnin
C	Updated body of drawing to reflect current requirements. - glg	11-01-05	Charles Saffle

CURRENT CAGE CODE 67268

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED

REV																				
SHEET																				
REV	C	C	C	C	C	C	C													
SHEET	15	16	17	18	19	20	21													

REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Rick Officer

CHECKED BY
Raymond Monnin

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
24 June 1986

REVISION LEVEL
C

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

MICROCIRCUIT, DIGITAL, CMOS, MEMORY, 64K X 1, STATIC RAM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**14933**	**5962-86015**

SHEET 1 OF 21

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-86015	01	X	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit	Acess time
01	see 6.6	64K x 1-bit, SRAM, TS	35 ns
02	see 6.6	64K x 1-bit, SRAM, TS	35 ns (data retention)
03	see 6.6	64K x 1-bit, SRAM, TS	45 ns
04	see 6.6	64K x 1-bit, SRAM, TS	45 ns (data retention)
05	see 6.6	64K x 1-bit, SRAM, TS	55 ns
06	see 6.6	64K x 1-bit, SRAM, TS	55 ns (data retention)
07	see 6.6	64K x 1-bit, SRAM, TS	70 ns
08	see 6.6	64K x 1-bit, SRAM, TS	70 ns (data retention)

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See Figure 1	22	dual-in-line package
Y	See Figure 2	22	dual-in-line package
Z	See Figure 3	22	chip carrier package

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Input voltage range	-0.5 V dc to V_{CC} + 0.5 V dc
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+270°C
Thermal resistance, junction-to-case (θ_{JC})	
Case X	+15°C / W 1/
Case Y	+30°C / W 1/
Case Z	+30°C / W 1/
Output voltage applied	-0.5 V dc to +7.0 V dc
Output current	50 mA
Maximum power dissipation (P_D)	1.0 W
Maximum junction temperature (T_J)	+150°C

1.4 Recommended operating conditions.

Supply voltage range	4.5 V dc minimum to 5.5 V dc maximum
Input high voltage	2.2 V dc to V_{CC} +0.5 V
Input low voltage	-0.5 V dc to +0.8 V dc
Fanout current with output high (each)	4.0 mA
Case operating temperature range (T_C)	-55°C to +125°C

1/ When a thermal resistance value is listed in MIL-STD-1835, it shall supersede the value stated herein.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 4.

3.2.2 Truth table. The truth table shall be as specified on figure 5.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 6.

3.2.4 Case outlines. The case outlines shall be in accordance with figure 1 and 1.2.2 herein.

3.2.5 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection only. Each coated microcircuit inspection lot (see inspection lot as defined in MIL-PRF-38535) shall be subjected to and pass the internal moisture content test at 5000 ppm (see method 1018 of MIL-STD-883). The frequency of the internal water vapor testing shall not be decreased unless approved by the preparing activity for class M. The TRB will ascertain the requirements as provided by MIL-PRF-38535 for classes Q and V. Samples may be pulled any time after seal.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime 's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} ,C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect input or output capacitance.

d. Subgroups 7 and 8 test sufficient to verify truth table of figure 5.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ 3/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	I_{OH} = -4.0 mA, V_{IH} = 2.2 V, V_{IL} = 0.8 V	1, 2, 3	All	2.4		V
Low level output voltage	V_{OL}	I_{OL} = +8.0 mA, V_{IL} = 0.8 V, V_{IH} = 2.2 V	1, 2, 3	All		0.4	V
High impedance (off-state) output leakage current	I_{OLZ}	$\overline{CS} \geq V_{IH}$, V_{OH} = 0.0 V, V_{CC} = 5.5 V	1, 2, 3	All	-10	10	µA
	I_{OHZ}	$\overline{CS} \geq V_{IH}$, V_{OH} = 5.5 V, V_{CC} = 5.5 V	1, 2, 3	All	-10	10	µA
High level input leakage current	I_{IH}	V_{IH} = 5.5 V, V_{CC} = 5.5 V	1, 2, 3	All	-10	10	µA
Low-level input leakage current	I_{IL}	V_{IL} = 0.0 V, V_{CC} = 5.5 V	1, 2, 3	All	-10	10	µA
Operating supply current	I_{CC1}	D_{OUT} = open, $\overline{CS}$ = V_{IL}, V_{CC} = 5.5 V	1, 2, 3	03,05,07		105	mA
				01,02,04, 06,08		90	
DC supply current	I_{CC2}	D_{OUT} = open, $\overline{CS}$ = V_{IL}, Minimum read cycle time, V_{CC} = 5.5 V	1, 2, 3	03,05,07		120	mA
				02		70	
				01,04,06, 08		95	
Standby supply current (TTL)	I_{CC3}	$\overline{CS} \geq V_{IH}$, V_{CC} = 5.5 V, Inputs = 0.8 V or 2.2 V	1, 2, 3	03.05,07		50	mA
				01,02,04, 06,08		35	
Full standby supply current (CMOS)	I_{CC4}	$\overline{CS} \geq V_{CC}$ - 0.2 V, V_{CC} = 5.5 V, Inputs: $\geq V_{CC}$ - 0.2 V or $\leq$ 0.2 V	1, 2, 3	All		20	mA
Data retention current 4/	I_{CCDR}	V_{DR} = 2.0 V, $\overline{CS} \geq V_{CC}$ - 0.2 V, Inputs: $\geq V_{CC}$ - 0.2 V or $\leq$ 0.2 V	1, 2, 3	02,04,06, 08		1	mA
Input capacitance	C_{IN}	V_{IN} = 0.0 V, 5/, V_{CC} = 5.0 V, f = 1 MHz	4	All		8	pF
Output capacitance	C_{OUT}	V_{OUT} = 0.0 V (see 4.3.1c)		All		10	pF
Data retention voltage 4/	V_{DR}	$\overline{CS}$ = V_{DR}, Inputs: $\geq V_{DR}$ - 0.2 V or $\leq$ 0.2 V	1, 2, 3	02,04,06, 08	2.0	5.5	V
Functional tests		See 4.3.1d, V_{IL} = 0.0 V, V_{IH} = 3.0 V	7, 8	All			

See footnotes at end of table

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Address access time	t_{AVQV}		9, 10, 11	07,08		70	ns
				05,06		55	
				03,04		45	
				01,02		35	
Output hold time	t_{AXQX}		9, 10, 11	All	3		ns
Read cycle time	t_{ELEH}		9, 10, 11	07,08	70		ns
				05,06	55		
				03,04	45		
				01,02	35		
Chip enable access time	t_{ELQV}		9, 10, 11	07,08		70	ns
				05,06		55	
				03,04		45	
				01,02		35	
Chip enable to output active	t_{ELQX}	6/	9, 10, 11	All	5		ns
Chip disable to output disable 7/	t_{EHQZ}	6/	9, 10, 11	All	0	40	ns
Write cycle time	t_{AVAV}		9, 10, 11	07,08	70		ns
				05,06	55		
				03,04	45		
				01,02	35		
Chip enable to end of write	t_{ELWH}		9, 10, 11	05,06,07, 08	55		ns
				03,04	40		
				01,02	30		
Address valid to write high	t_{AVWH}		9, 10, 11	05,06,07, 08	55		ns
				03,04	40		
				01,02	30		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write high to address don't care	t_{WHAX}		9, 10, 11	All	5		ns
Write pulse width	t_{WLEH}		9, 10, 11	01,02	25		ns
				03-08	40		
Address setup to beginning of write	t_{AVWL}		9, 10, 11	01,02	5		ns
				03-08	15		
Data valid to write high	t_{DVWH}		9, 10, 11	01,02	20		ns
				03,04,05, 06	25		
				07,08	30		
Write high to data don't care	t_{WHDX}		9, 10, 11	All	5		ns
Write enable to output disable 7/	t_{WLQZ}	6/	9, 10, 11	01,02	0	20	ns
				03-06	0	30	
				07,08	0	35	
Output active after end of write	t_{WHQX}	6/	9, 10, 11	All	0		ns
Address setup before chip enable	t_{AVEL}		9, 10, 11	All	5		ns
Chip enable high to address don't care	t_{EHAX}		9, 10, 11	All	5		ns
Data valid to chip enable high	t_{DVEH}		9, 10, 11	01,02	20		ns
				03,04, 05,06	25		
				07,08	30		
Chip disable to data retention time 8/	t_{CDR}	4/	9, 10, 11	02,04	45		ns
				06,08	70		
Data retention recovery time 8/	t_R	4/	9, 10, 11	02,04	45		ns
				06,08	70		
Chip select to power-up time 8/	t_{PU}		9, 10, 11	All		0	ns
Chip deselect to power-down time 8/	t_{PD}		9, 10, 11	01-04	0	45	ns
				05-08	0	70	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

1/ Unless otherwise specified, T_C = -55°C to +125°C and V_{CC} = 4.5 V to 5.5 V. All voltage referenced to GND.

2/ AC measurement assume input transistor time ≤ 5 ns and input levels are from GND to 3.0 V. Timing reference levels are 1.5 V.

3/ See figure 7 for ac timing waveforms and loading.

4/ Data retention devices only.

5/ Effective capacitance calculated from C = ΔV = 3 V and V_{CC} = 5.0 V or measured with a capacitance meter.

6/ Transition to high impedance state is measured ±500 mV from steady state voltage with load specified on figure 7. This parameter is sampled and not 100 percent tested.

7/ Minimum limit not tested and is included for user guidelines.

8/ May not be tested, but shall be guaranteed to the limits specified in table I.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8A, 8B, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3, 7, 8

* PDA applies to subgroups 1.

CASE X

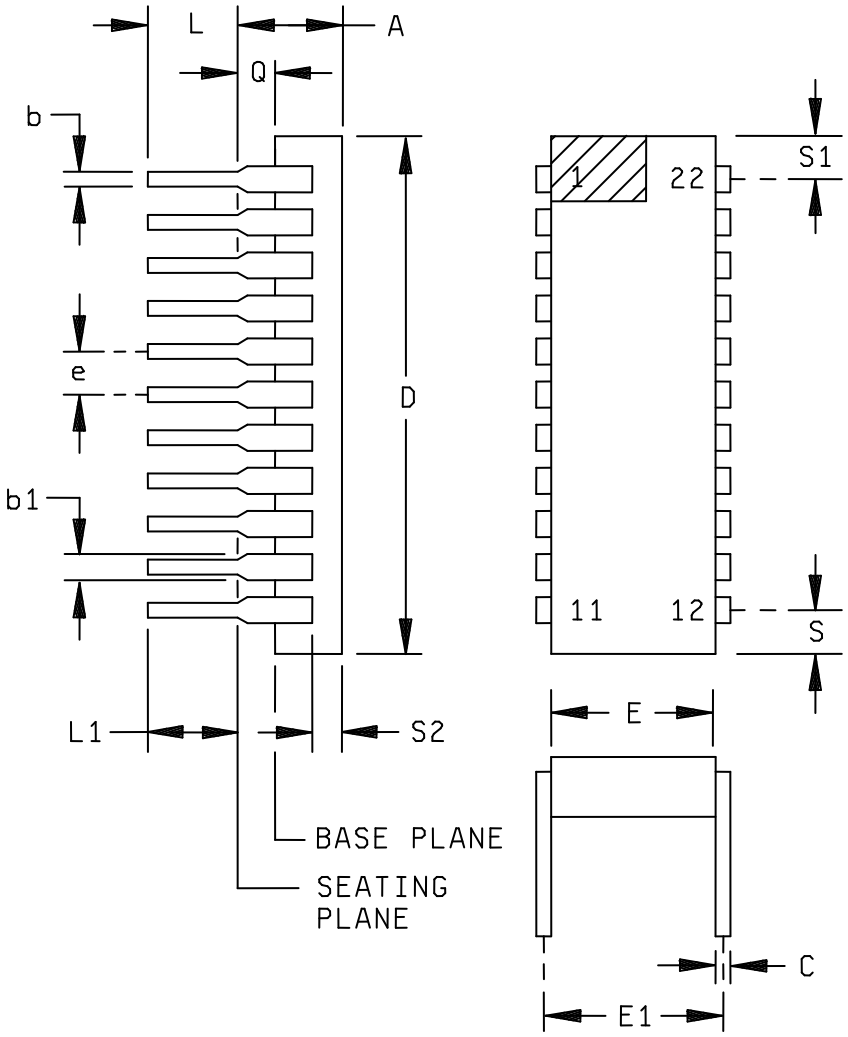


FIGURE 1. 22-lead dual-in-line package.

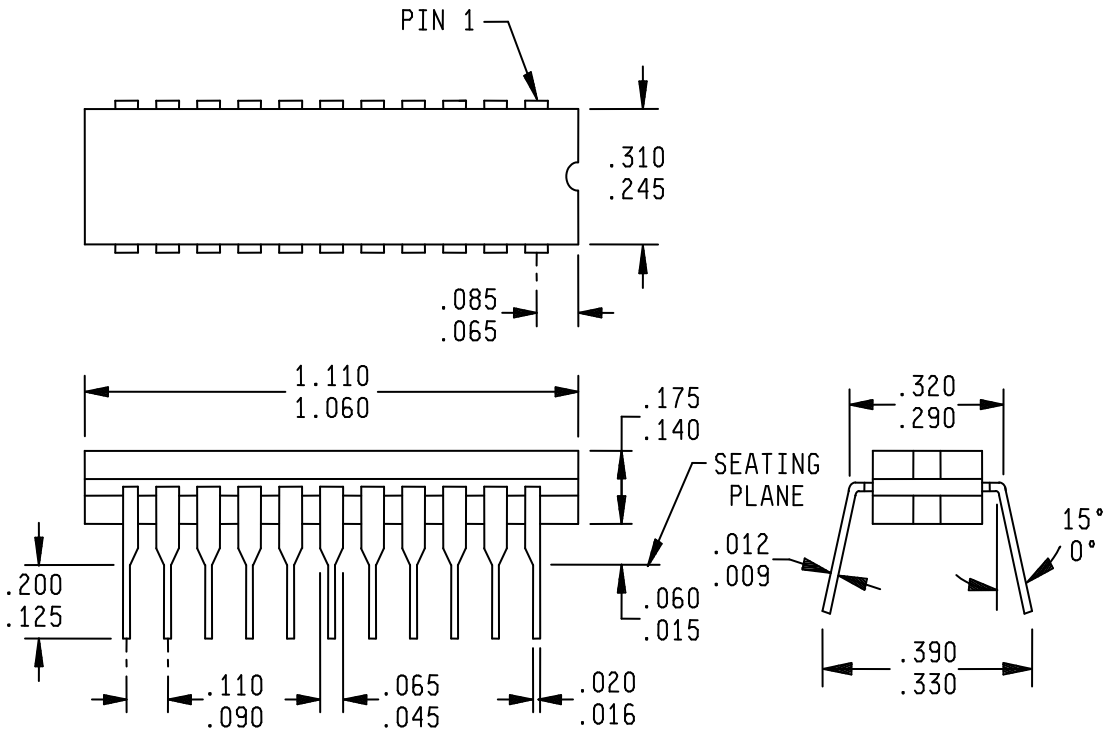
Symbol	Min	Max
A	---	.200
b	.014	.023
b1	.030	.065
c	.008	.015
D	---	1.260
E	.220	.310
E1	.290	.320
e	.100 BSC	
L	.125	.200
L1	.150	---
Q	.015	.060
S	---	.080
S1	.005	---
S2	.005	---
N	22	

Inches	mm
.005	0.13
.008	0.20
.014	0.36
.015	0.38
.023	0.58
.030	0.76
.060	1.52
.080	2.08
.125	3.18
.150	3.81
.200	5.08
.220	5.59
.290	7.37
.310	7.87
.320	8.13
1.260	32.00

Notes:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.

FIGURE 1. 22-lead dual-in-line package - Continued.

CASE Y



Inches	mm		Inches	mm
.009	0.22		.140	3.55
.012	0.30		.175	4.44
.015	0.38		.200	5.08
.016	0.40		.245	6.22
.020	0.50		.290	7.36
.045	1.14		.310	7.87
.060	1.52		.320	8.12
.065	1.65		.330	8.38
.085	2.15		.390	9.90
.090	2.28		1.060	26.92
.110	2.79		1.110	28.19
.125	3.17			

Notes:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.

FIGURE 2. 22-lead dual-in-line package.

CASE Z

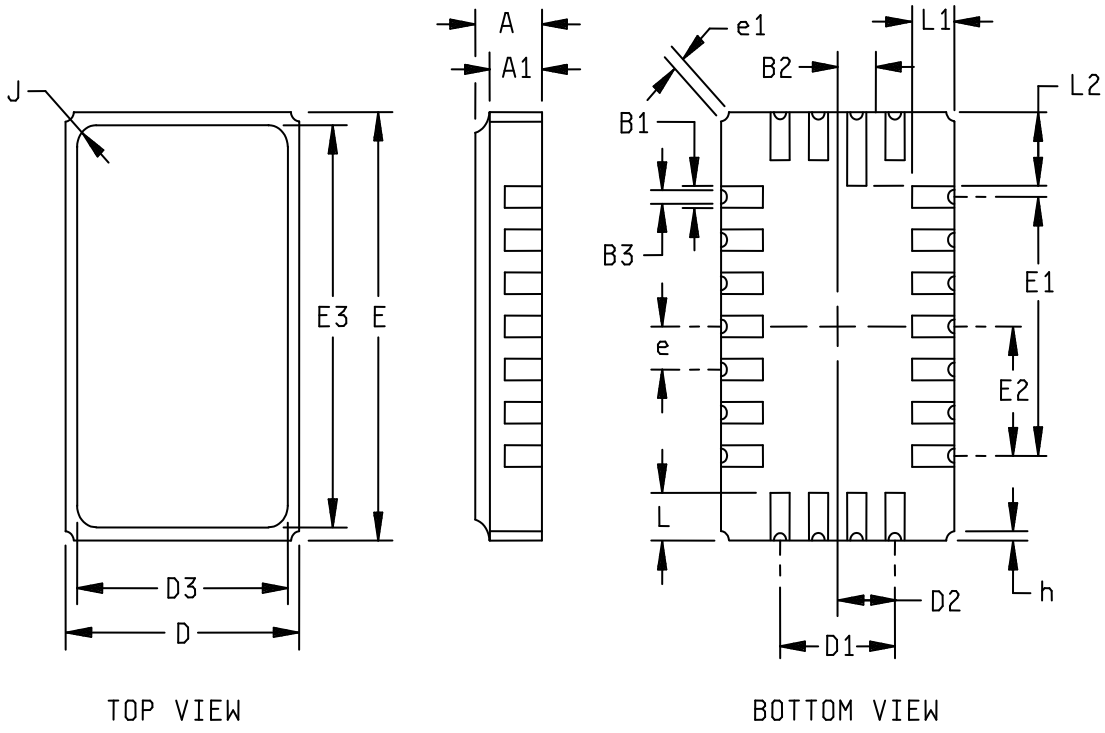


FIGURE 3. 22-terminal chip carrier package.

Symbol	Case Z			
	Inches		Milimeters	
	Min	Max	Min	Max
A	.060	.120	1.52	3.05
A1	.050	.088	1.27	2.24
B1	.022	.028	0.56	0.71
B2	.072 REF		1.83 REF	
B3	.006	.041	0.15	1.03
D	.280	.305	7.11	7.75
D1	.150 BSC		0.38 BSC	
D2	.075 BSC		1.91 BSC	
D3	---	.305	---	7.75
E	.480	.496	12.15	12.29
E1	.300 BSC		7.62 BSC	
E2	.150 BSC		3.81 BSC	
E3	---	.496	---	12.29
e	.050 BSC		1.27 BSC	
e1	.015	---	0.38	---
h	.025 REF		0.64 REF	
j	.025 REF		0.64 REF	
L	.039	.055	0.99	1.40
L1	.039	.055	0.99	1.40
L2	.075	.095	1.91	2.41
ND	4	---	101.6	---
NE	7	---	177.8	---
N	22	---	558.8	---

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.

FIGURE 3. 22-terminal chip carrier package.

Device Types	All
Case Outlines	X, Y and Z
Terminal Number	Terminal Symbol
1	A_0
2	A_1
3	A_2
4	A_3
5	A_4
6	A_5
7	A_6
8	A_7
9	D_{OUT}
10	$\overline{WE}$
11	GND
12	$\overline{CS}$
13	D_{IN}
14	A_8
15	A_9
16	A_{10}
17	A_{11}
18	A_{12}
19	A_{13}
20	A_{14}
21	A_{15}
22	V_{CC}

FIGURE 4. Terminal connections.

Mode	$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	Power level
Standby	H	X	X	High Z	Standby
Read	L	H	X	D	Active
Write	L	L	D	High Z	Active
Data retention	V_{DR}	X	X	High Z	Data retention

High Z = High impedance
D = Valid data bit
X = Don't care

FIGURE 5. Truth table.

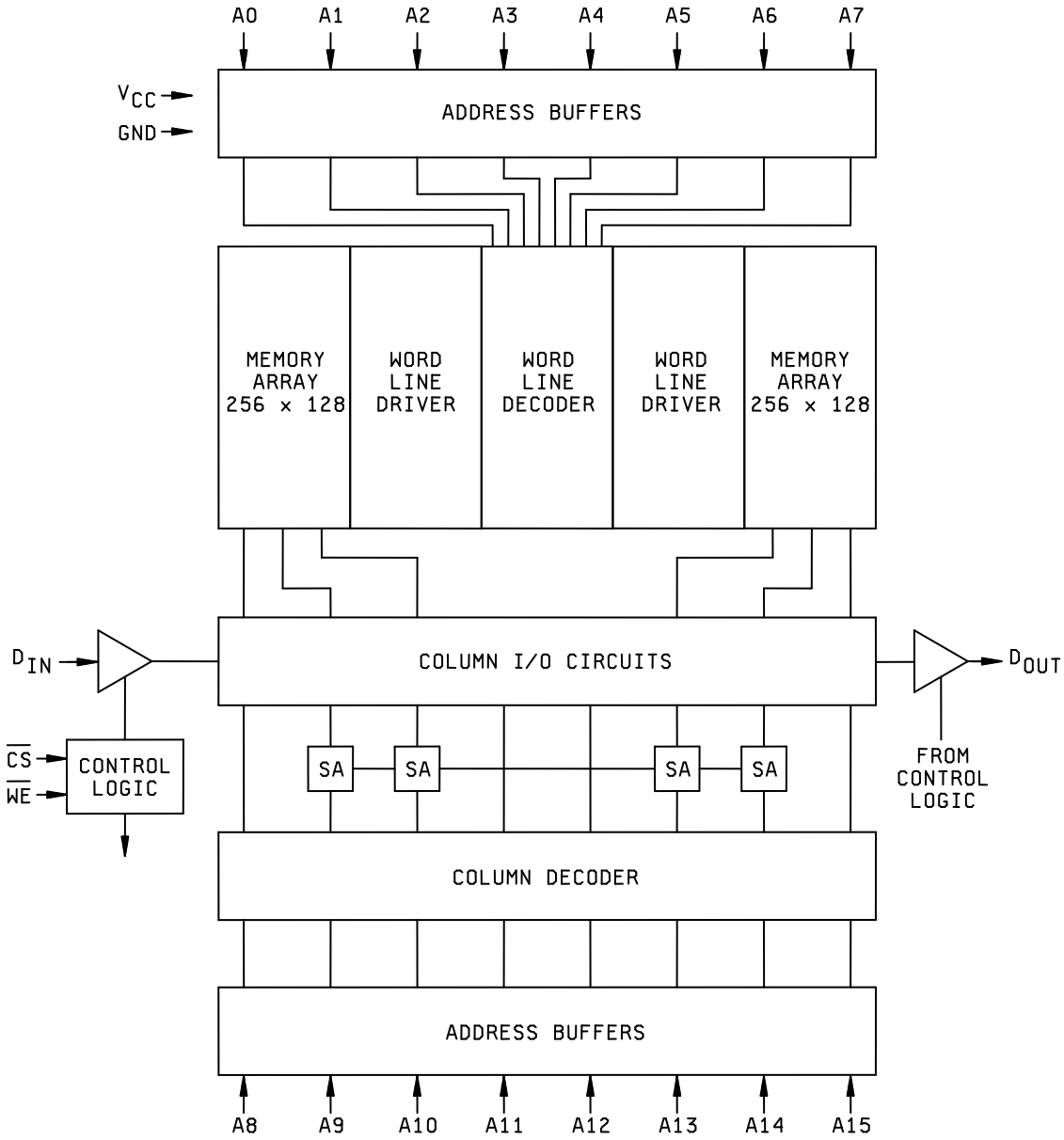


FIGURE 6. Functional block diagram.

Read cycle 1 (where $\overline{CS}$ is active prior to or within 5 ns of address change, $\overline{WE}$ = V_{IH}).

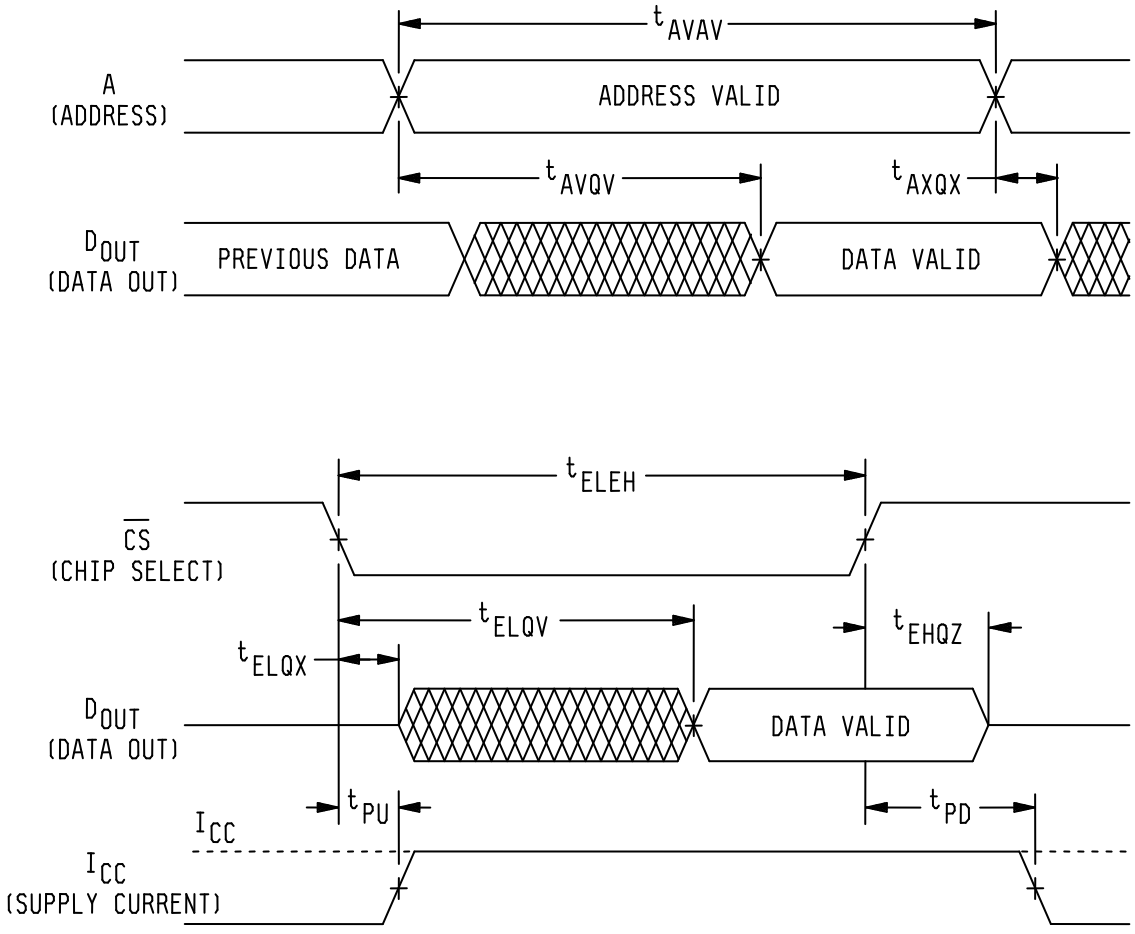


FIGURE 7. AC timing waveforms and loading.

Write cycle 1. This write cycle is $\overline{WE}$ controlled, when $\overline{CS}$ is active (LOW) prior to $\overline{WE}$ becoming active (LOW), in this write cycle the data out may become active, requiring observance of t_{WLQZ} to avoid data bus contention in common I/O applications. At the end of the write cycle the data out may become active if $\overline{WE}$ becomes inactive (HIGH) prior to $\overline{CS}$ becoming inactive (HIGH).

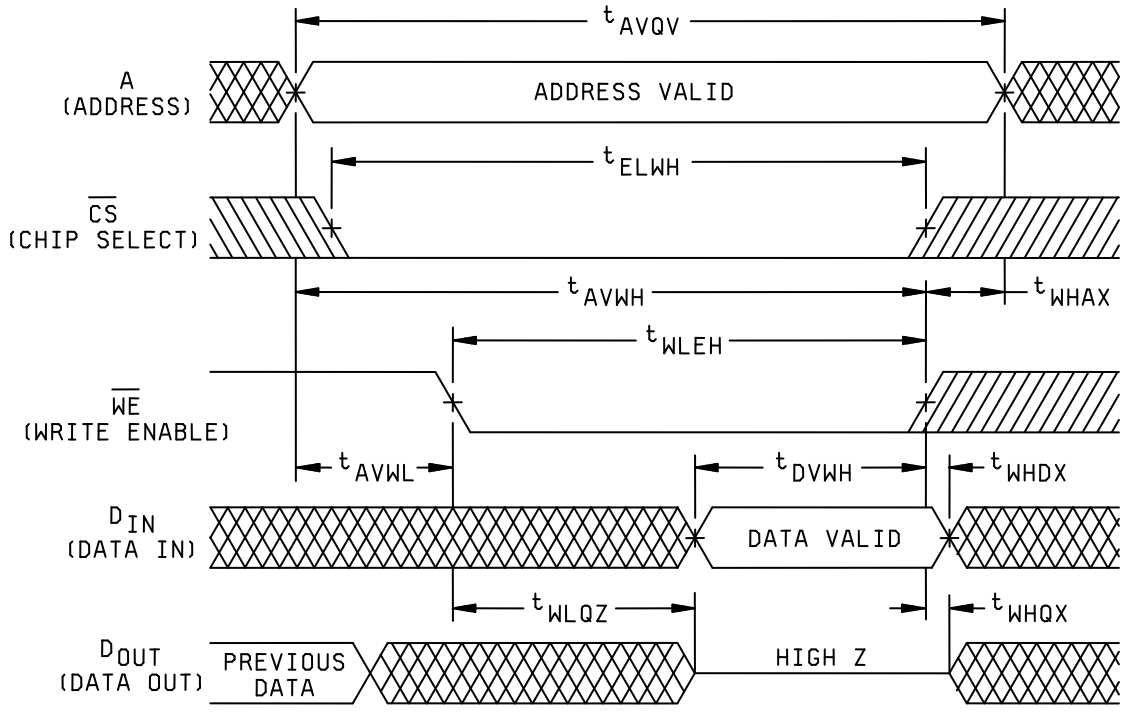


FIGURE 7. AC timing waveforms and loading - Continued.

Write cycle 2. This write cycle is $\overline{CS}$ controlled, where $\overline{WE}$ is active (LOW) prior to or coincident with $\overline{CS}$ becoming active (LOW). In this write cycle the data out remains in the high impedance state (3 state) at the beginning of the write cycle, precluding potential data contention in common I/O application.

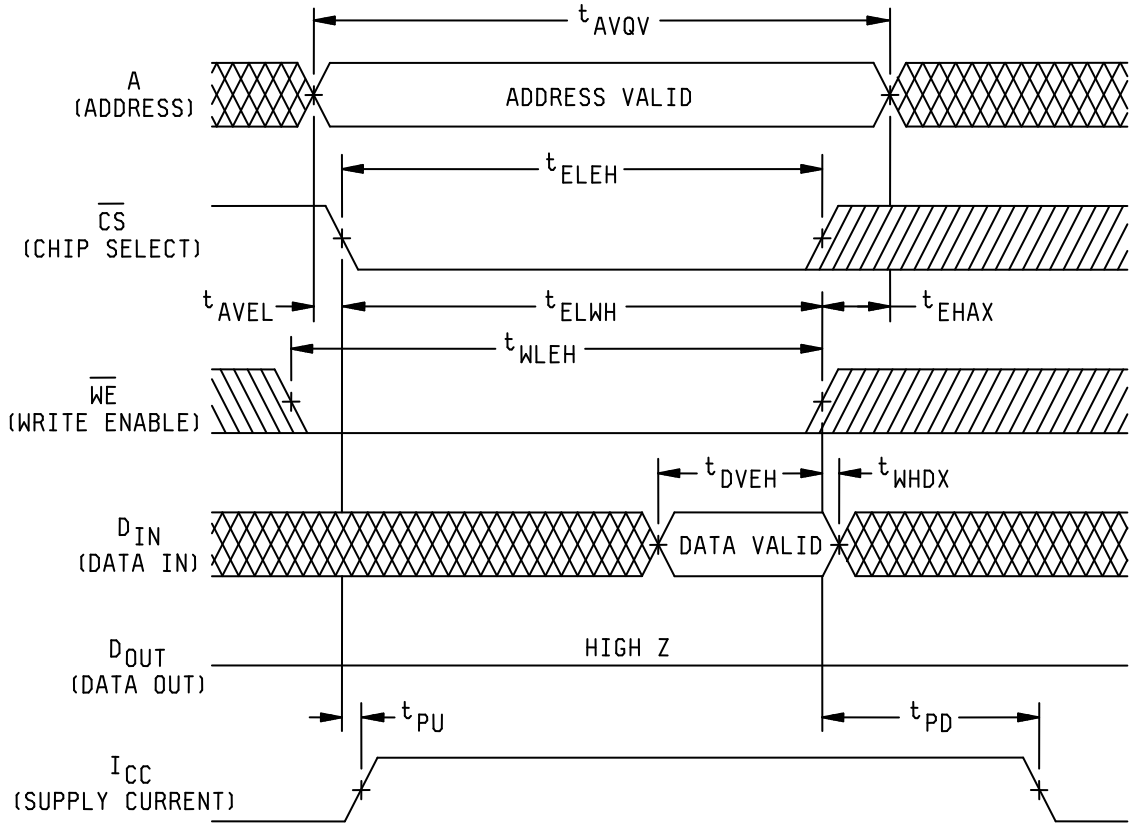


FIGURE 7. AC timing waveforms and loading - Continued.

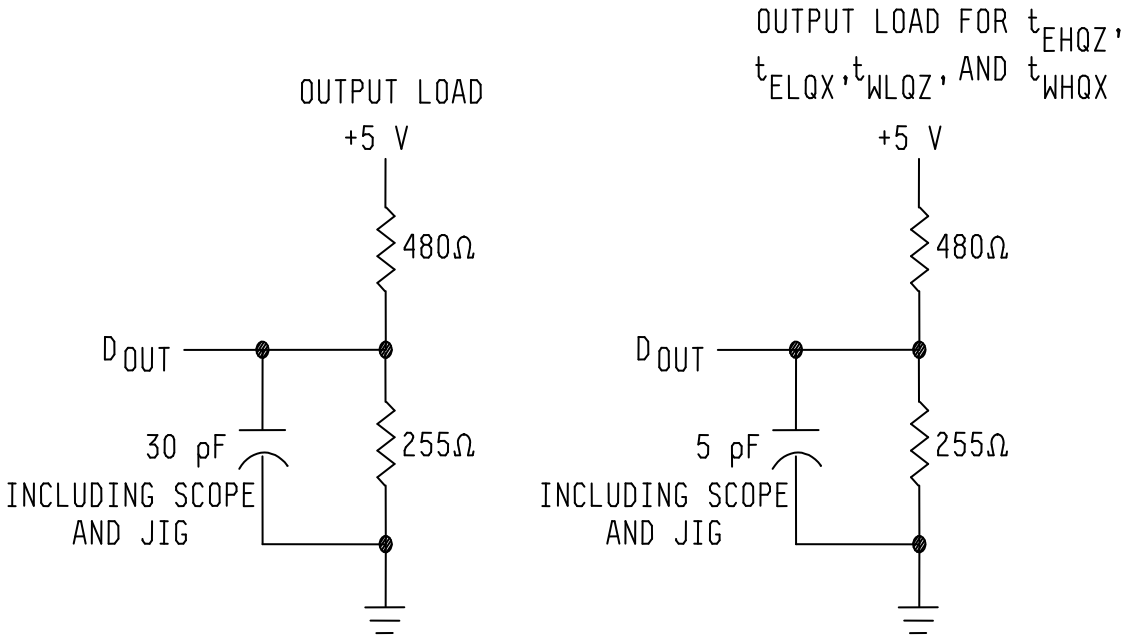
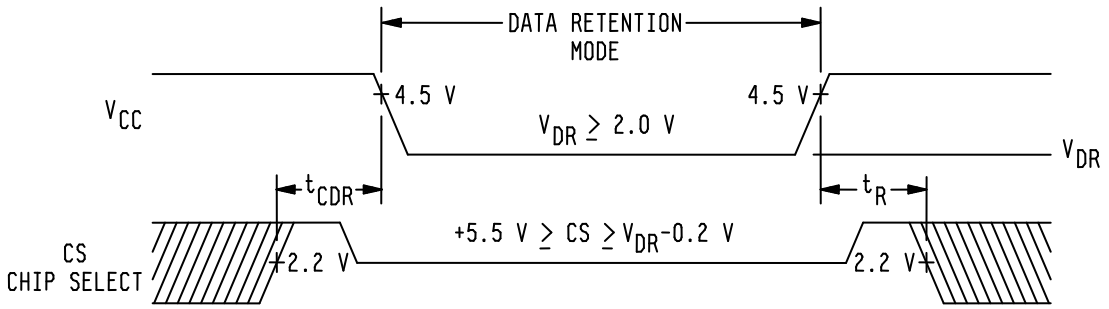
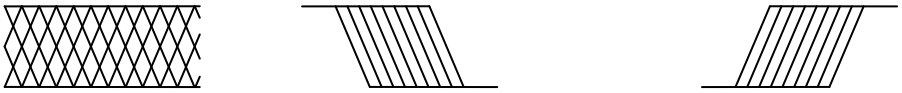


FIGURE 7. AC timing waveforms and loading - Continued.

DATA RETENTION WAVEFORM



AC WAVEFORM LEGEND



INVALID OR DON'T CARE

TRANSITION FROM HIGH TO LOW LEVEL, MAY OCCUR ANY TIME DURING THIS PERIOD

TRANSITION FROM LOW TO HIGH LEVEL, MAY OCCUR ANY TIME DURING THIS PERIOD

FIGURE 7. AC timing waveforms and loading - Continued.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-0547.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 11-01-05

Approved sources of supply for SMD 86015 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/	Reference military specification part number
5962-8601501XA	3/ 3/ 3DTT2	F1600DMQB35 6287-35/BXAJC P4C187-35CMB	
5962-8601501YA	3/ 3/ 3DTT2	CY7C187-35DMB IDT7187S35DB P4C187-35DMB	
5962-8601501ZA	3/ 3/ 3/ 3DTT2	F1600-35LMQ35 CY7C187-35LMB 6287-35M/BUAJC P4C187-35LMB	
5962-8601502XA	3/ 3/ 3/ 3DTT2	F1601DMQB35 MKX 41H87P835 6287-35/BXAJC P4C187L-35CMB	
5962-8601502YA	3/ 3/ 3DTT2	CY7C187N35DMB MKX 41H87J835 P4C187L-35DMB	
5962-8601502ZA	3/ 3/ 3/ 3/ 3DTT2	CY7C187L-35DMB F1601-35LMQB35 MKX 41H87E835 6287-35M/BUAJC P4C187L-35LMB	
5962-8601503XA	3/ 3/ 3/ 3/ 3DTT2	F1600DMQB45 IMS1600S-45M IDT7187S45DB 6287-45/BXAJC P4C187-45CMB	
5962-8601503YA	3/ 3/ 3DTT2	CY7C187-45DMB IDT7187S45DB P4C187-45DMB	
5962-8601503ZA	3/ 3/ 3/ 3/ 3/ 3DTT2	F1600LMQB45 CY7C187-45LMB IDT7187S45LB 6287-45M/BUAJC IMS1600N-45M P4C187-45LMB	M38510/29202BUA

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/	Reference military specification part number
5962-8601504XA	3/ 3/ 3/ 3/ 3DTT2	F1601DMQB45 MKX 41H87P845 IDT7187L45DB 6287-45/BXAJC P4C187L-45CMB	
5962-8601504YA	3/ 3/ 3/ 3DTT2	CY7C187L-45DMB MKX 41H87J845 IDT7187L45DB P4C187L-45DMB	
5962-8601504ZA	3/ 3/ 3/ 3/ 3/ 3DTT2	CY7C187L-45LMB MKX41H87E845 F1601LMQB45 IDT7187L45LB 6287-45M/BUAJC P4C187L-45LMB	
5962-8601505XA	3/ 3/ 3/ 3DTT2	F1600DMQB55 IDT7187S55DB IMS1600S-55M P4C187-55CMB	
5962-8601505YA	3/ 3DTT2	IDT7187S55DB P4C187-55DMB	
5962-8601505ZA	3/ 3/ 3/ 3DTT2	F1600LMQB5 IDT7187S55LB IMS1600N-55M P4C187-55LMB	M38510/29201BUA
5962-8601506XA	3/ 3/ 3/ 3/ 3DTT2	F1601DMQB55 IDT7187L55DB IMS1601S-55M MKX 41H87P855 P4C187L-55CMB	
5962-8601506YA	3/ 3/ 3DTT2	MKX 41H87J855 IDT7187L55DB P4C187L-55DMB	
5962-8601506ZA	3/ 3/ 3/ 3/ 3DTT2	F1601LMQB55 IDT7187L55LB IMS1601N-55M MKX 41H87E855 P4C187L-55LMB	M38510/29203BUA

See notes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 1/	Reference military specification part number
5962-8601507XA	3/ 3/ 3DTT2	IMS1601S-70M IDT7187S70DB P4C187-70CMB	
5962-8601507YA	3/ 3DTT2	IDT7187S70DB P4C187-70DMB	
5962-8601507ZA	3/ 3/ 3DTT2	IMS1600N-70M IDT7187S70LB P4C187-70LMB	
5962-8601508XA	3/ 3/ 3DTT2	IMS1601S-70LM IDT7187L70DB P4C187L-70CMB	
5962-8601508YA	3/ 3DTT2	IDT7187L70DB P4C187L-70DMB	
5962-8601508ZA	3/ 3/ 3DTT2	IMS1601N-70LM IDT7187L70LB P4C187L-70LMB	M38510/29204BUA

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
3DTT2	Pyramid Semiconductor Corporation 1340 Bordeaux Drive Sunnyvale, CA 94089

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.