REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Make changes to table I, table II, 4.3.1, 6.4, and figure 3. Editorial changes throughout.	89-01-27	M. A. Frye
B	Add device type 02. Add one vendor, CAGE 44270. Make changes to table I, figure 2, and figure 3. Make editorial changes throughout.	90-03-28	M. A. Frye
C	Update to current requirements. Editorial changes throughout. - drw	03-09-12	Raymond Monnin

REV																				
SHEET																				
REV																				
SHEET																				
REV STATUS				REV			C	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Rick C. Officer

CHECKED BY
Charles E. Besore

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
88-04-21

REVISION LEVEL
C

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, LINEAR, CMOS ARINC BUS INTERFACE, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-86880**

SHEET 1 OF 14

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-86880	01	Q	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function
01	HS3282	CMOS ARINC bus interface circuit 1/
02	HI8282	CMOS ARINC bus interface circuit 1/

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Q	CDIP2-T40 or GDIP1-T40	40	dual-in-line
X	CQCC1-N44	44	square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 2/

Supply voltage (V_{CC})	7.0 V dc
Voltage at any pin (except 2, 3, 4, and 5)	GND – 0.3 V dc to V_{CC} + 0.3 V dc
Voltage at pins 2, 3, 4, and 5	-29 V dc to +29 V dc
Storage temperature range (Tstg)	-65°C to +150°C
Power dissipation (P_D):	
Case Q	1.875 W at +25°C 3/
Case X	1.25 W at +25°C 3/
Maximum junction temperature (T_J)	+175°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	5.0 V dc
Ambient operating temperature range (T_A)	-55°C to +125°C
ARINC inputs:	
Logic “1” input voltage (V_{IH})	6.7 V dc minimum to 13 V dc maximum
Logic “0” input voltage (V_{IL})	-6.7 V dc minimum to -13 V dc maximum
Null input voltage (V_{IN})	-2.5 V dc minimum to +2.5 V dc maximum
Common mode voltage (V_{CH})	-5 V dc minimum to +5 V dc maximum

1/ This circuit was designed to be compatible with the Aeronautical Radio, Incorporated (ARINC), specification 429 serial communications protocol. The applicable specifications are designed in this drawing.
2/ All voltages are referenced to V_{SS}.
3/ Derate above +25°C, 12.5 mW/°C for case Q and 8.3 mW/°C for case X.

1.4 Recommended operating conditions - continued.

Bi-directional inputs:
Logic “1” input voltage (V_{IH})..... 2.1 V dc minimum
Logic “0” input voltage (V_{IL})..... 0.7 V dc maximum
All other inputs:
Logic “1” input voltage (V_{IH})..... 3.5 V dc minimum
Logic “0” input voltage (V_{IL})..... 0.7 V dc maximum

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Switching waveforms. The switching waveforms shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Logic "1" output	V_{OH}	I_{OH} = -1.5 mA, V_{CC} = 5.0 V	1, 2, 3	All	2.7		V
Logic "0" output	V_{OL}	I_{OH} = 1.8 mA, V_{CC} = 5.0 V	1, 2, 3	All		0.4	V
Output capacitance	C_O	T_A = +25°C 1/	4	All		15	pF
Supply current (standby)	I_{CC1}	V_{CC} = 5.25 V, V_{IN} = 0 V	1, 2, 3	All		20	mA
Supply current (operation)	I_{CC2}	V_{CC} = 5.25 V 2/	1, 2, 3	All		20	mA
Input leakage 3/	I_{IL}	V_{IN} = 0 V	1, 2, 3	01	-75		µA
		V_{IN} = 0 V, maximum pull-up current		02	-20		
	I_{IH}	$V_{IN} = V_{CC}$	1, 2, 3	All		10	µA
Input leakage (bi-directional input)	I_I	$0 V \le V_{IN} \le V_{CC}$	1, 2, 3	All	-1.5	1.5	µA
Input leakage (ARINC input)	I_{IL}	V_{IN} = 0 V	1, 2, 3	All	-450		µA
	I_{IH}	$V_{IN} = V_{IH}$	1, 2, 3	01		200	µA
		V_{CC} = 5.25 V, $V_{IN} = V_{CC}$		02		200	
Input impedance to V_{CC} (ARINC input)	R_H		4, 5, 6	All	12		kΩ
Input capacitance to V_{CC} (ARINC input)	C_H	T_A = +25°C 1/	4	All		20	pF
Input capacitance to GND (ARINC input)	C_G	T_A = +25°C 1/	4	All		20	pF
Differential input impedance (ARINC input)	R_I		4, 5, 6	All	12		kΩ
Input capacitance (all other inputs)	C_I	T_A = +25°C 1/	4	All		25	pF
Input impedance to GND (ARINC input)	R_G		4, 5, 6	All	12		kΩ
Differential input capacitance (ARINC input)	C_I	T_A = +25°C 1/	4	All		20	pF
Clock frequency	F_C	V_{CC} = 4.75 V and 5.25 V, 50% duty cycle 5/	7, 8	All		1	MHz
Data rate	F_D	V_{CC} = 4.75 V and 5.25 V	7, 8	All		100	kHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 4/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Data select to data enable time	t_{SELEN}	See figure 3		9, 10, 11	All	20		ns
Output data disable time	t_{DATAEN}	See figure 3 1/		9, 10, 11	01		80	ns
					02		150	
Control word register strobe pulse width	t_{CWSTR}	See figure 3		9, 10, 11	All	130		ns
Transmitter ready delay time	$t_{TX/R}$	See figure 3		9, 10, 11	All		840	ns
Data word setup time	t_{DWSET}	See figure 3		9, 10, 11	All	110		ns
Data word hold time	t_{DWHLD}	See figure 3		9, 10, 11	01	0		ns
					02	20		
Enable transmit to output data valid time	t_{ENDAT}	See figure 3	FD = 12.5 kbps	9, 10, 11	All		200	µs
			FD = 100 kbps				25	
Output data bit time	t_{BIT}	See figure 3	FD = 12.5 kbps	9, 10, 11	All	39.6	40.4	µs
			FD = 100 kbps			4.95	5.05	
Output data null time	t_{NUL}	See figure 3	FD = 12.5 kbps	9, 10, 11	All	39.6	40.4	µs
			FD = 100 kbps			4.95	5.05	
Data transmission word to $t_{X/R}$ set time	$t_{DTX/R}$	See figure 3		9, 10, 11	01		400	ns
		See figure 3	FD = 12.5 kbps		02		38.5	µs
			FD = 100 kbps				3.5	
Enable transmit turnoff time	t_{ENTXR}	See figure 3		9, 10, 11	All	0		ns
Data word gap time	t_{GAP}	See figure 3	FD = 12.5 kbps	9, 10, 11	All	316.8	323.2	µs
			FD = 100 kbps			39.6	40.4	
Data enable to parallel load delay time	t_{ENPL}	See figure 3		9, 10, 11	All	0		ns
Data enable hold for parallel hold time	t_{PLEN}	See figure 3		9, 10, 11	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

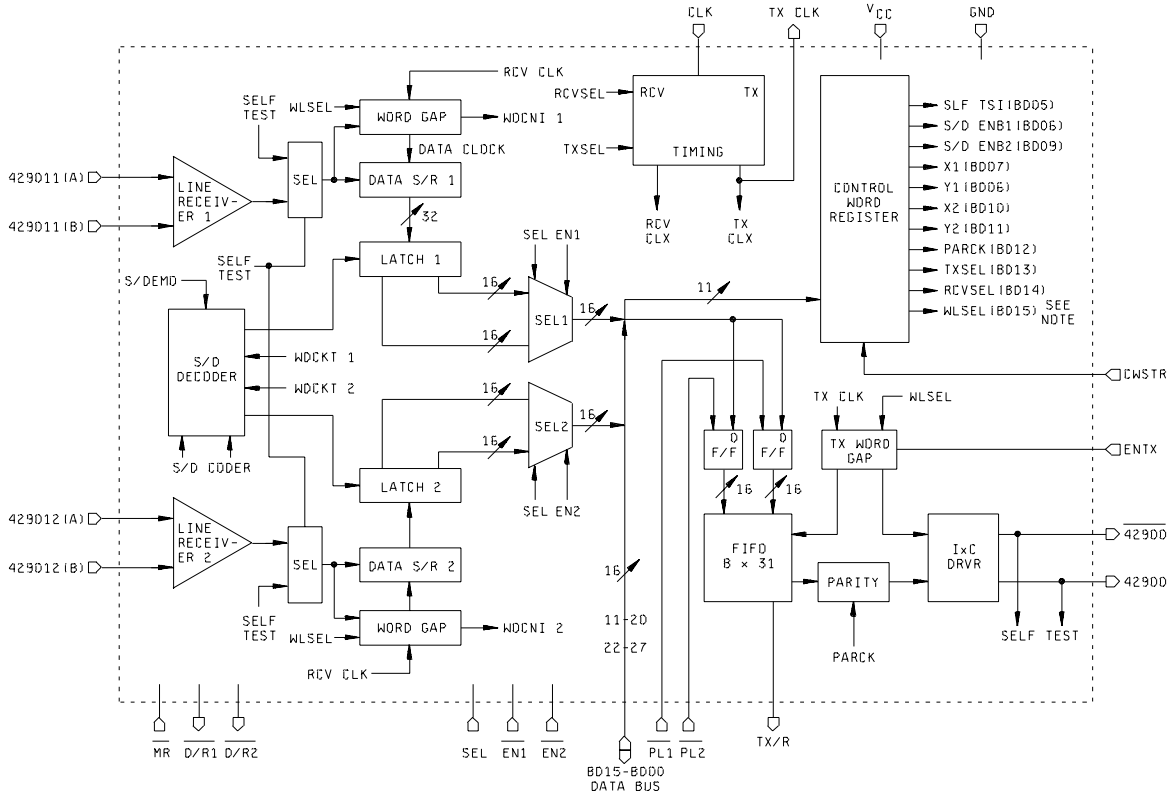
Test	Symbol	Conditions 4/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Enable transmit delay time	$t_{TX/REN}$	See figure 3	9, 10, 11	All	0		ns
Control word setup time	t_{CWSET}	See figure 3	9, 10, 11	01	130		ns
				02	140		
Control word hold time	t_{CWHLD}	See figure 3	9, 10, 11	01	0		ns
				02	40		
Parallel load pulse width	t_{PL}	See figure 3	9, 10, 11	All	200		ns
Parallel load 1 to parallel 2 delay	t_{PL12}	See figure 3	9, 10, 11	All	0		ns
Clock rise time	t_{LHC}	See figure 3 1/	9, 10, 11	01		10	ns
Master reset pulse width	t_{MR}	See figure 3	9, 10, 11	01	200		ns
				02	400		
Receiver device ready time from 32ND data bit	$t_{D/R2}$	See figure 3 6/ FD = 12.5 kbps	9, 10, 11	All		128	µs
		FD = 100 kbps				16	
Device ready to enable time	$t_{D/REN}$	See figure 3	9, 10, 11	All	0		ns
Data enable pulse width	t_{EN}	See figure 3	9, 10, 11	01	200		ns
				02	240		
Data enable to data enable time	t_{ENEN}	See figure 3	9, 10, 11	All	50		ns
Data enable to device ready time	$t_{EN/R}$	See figure 3	9, 10, 11	All		200	ns
Output data valid to enable time	t_{ENDATA}	See figure 3	9, 10, 11	All		200	ns
Data enable to data select time	t_{ENSEL}	See figure 3	9, 10, 11	01	20		ns
				02	50		

1/ Guaranteed but only tested initially and after design changes.
2/ V_{IN} = Logic "1" for all inputs except pins 8 and 33 which are logic "0".
3/ For case Q: Pins 8, 9, 10, 28, 29, 33, 34, 37, and 39.
For case X: Pins 10, 11, 12, 31, 32, 36, 37, 41, and 43.
4/ AC test conditions: V_{CC} = 5.0 V.
5/ 60 to 40 percent duty cycle is acceptable.
6/ Same delay for 25-bit word format. Device 01 only.

Device types	01 and 02	
Case outlines	Q	X
Terminal number	Terminal symbol	
1	V_{CC}	V_{CC}
2	429D11(A)	429D11(A)
3	429D11(B)	429D11(B)
4	429D12(A)	429D12(A)
5	429D12(B)	429D12(B)
6	$\overline{D/R1}$	N/C
7	$\overline{D/R2}$	N/C
8	SEL	$\overline{D/R1}$
9	$\overline{EN1}$	$\overline{D/R2}$
10	$\overline{EN2}$	SEL
11	BD15	$\overline{EN1}$
12	BD14	$\overline{EN2}$
13	BD13	BD15
14	BD12	BD14
15	BD11	BD13
16	BD10	BD12
17	BD09	BD11
18	BD08	N/C
19	BD07	BD10
20	BD06	BD09
21	GND	BD08
22	BD05	BD07

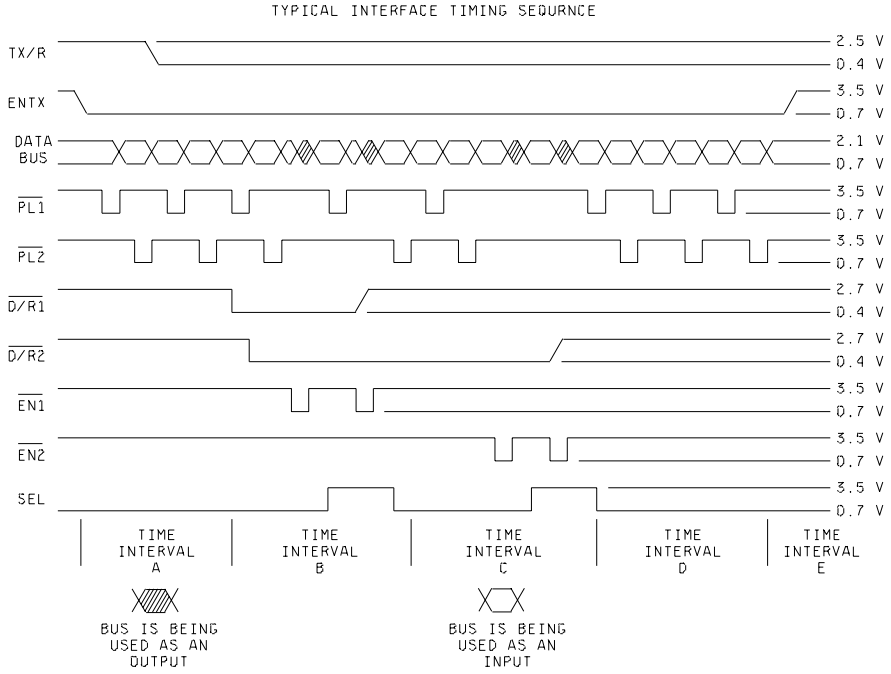
Device types	01 and 02	
Case outlines	Q	X
Terminal number	Terminal symbol	
23	BD04	BD06
24	BD03	GND
25	BD02	BD05
26	BD01	BD04
27	BD00	BD03
28	$\overline{PL1}$	BD02
29	$\overline{PL2}$	BD01
30	TX/R	BD00
31	429D0	$\overline{PL1}$
32	$\overline{429D0}$	$\overline{PL2}$
33	ENTX	TX/R
34	$\overline{CWSTR}$	429D0
35	N/C	$\overline{429D0}$
36	N/C	ENTX
37	CLK	$\overline{CWSTR}$
38	TX CLK	N/C
39	$\overline{MR}$	N/C
40	N/C	N/C
41	- - -	CLK
42	- - -	TX CLK
43	- - -	$\overline{MR}$
44	- - -	N/C

FIGURE 1. Terminal connections.



Note: For device type 02 only, W_{LSEL} (BD15) is always equal to a logic “0” for ARINC 429 applications.

FIGURE 2. Block diagram.



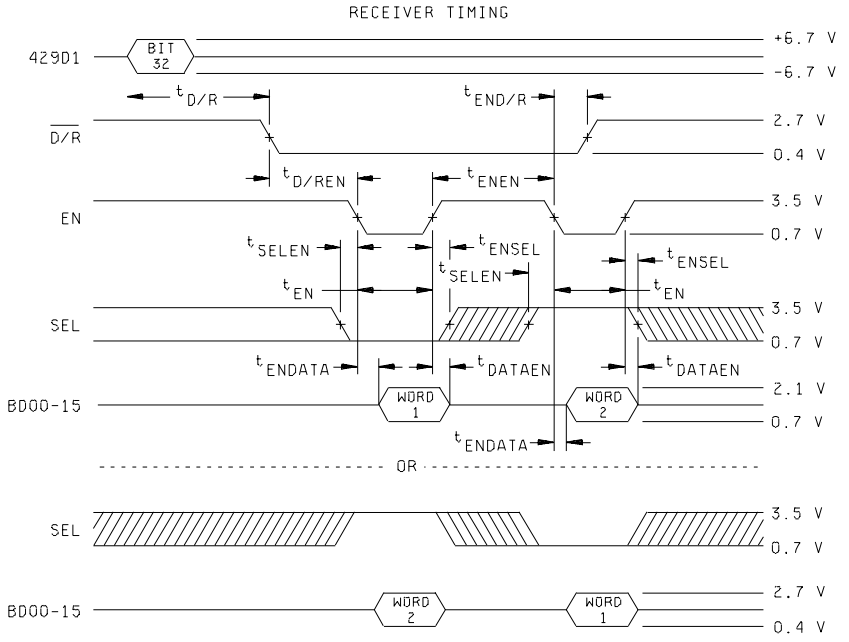


FIGURE 3. Switching waveforms.

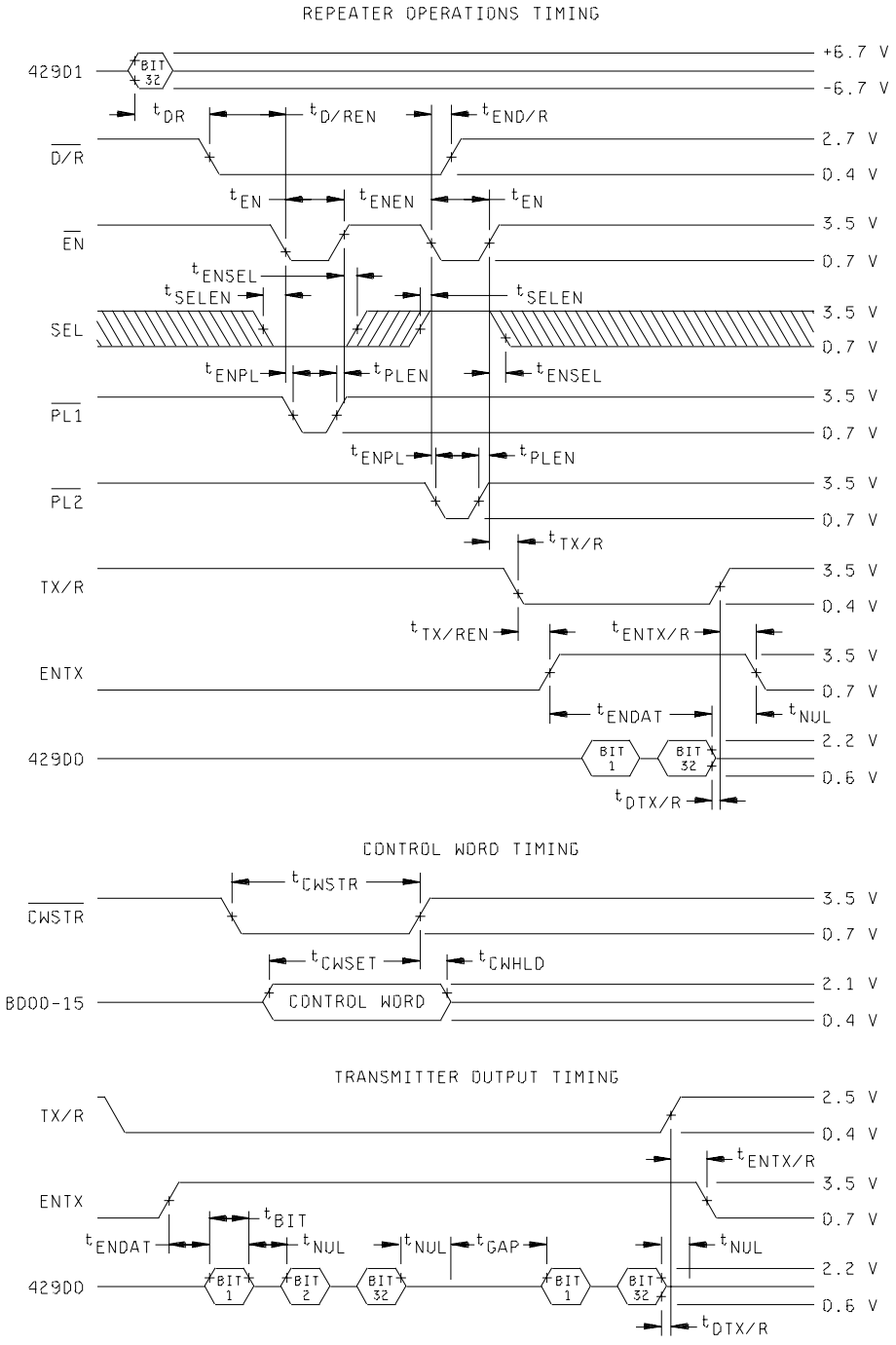


FIGURE 3. Switching waveforms – continued.

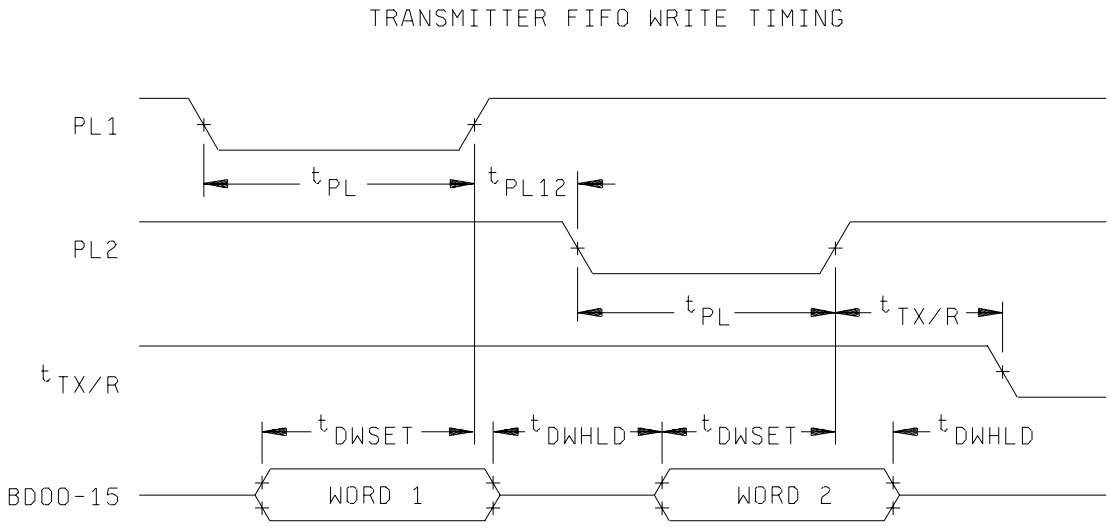


FIGURE 3. Switching waveforms – continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 9
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. Sample size is 15 devices, all input and output terminals tested, and no failures.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 03-09-12

Approved sources of supply for SMD 5962-86880 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8688001QA	34371	HS1-3282/883
5962-8688001XA	34371	HS4-3282/883
5962-8688002QA	44270	HI-8282CM-03
5962-8688002XA	3/	HI-8282SM-01

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34371	Intersil Corporation 2401 Palm Bay Blvd PO Box 883 Melbourne, FL 32902-0883
44270	Holt Integrated Circuits, Inc. 23351 Madero Mission Viejo, CA 92691-2730