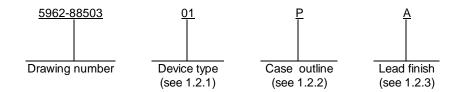
								F	REVISI	ONS										
LTR					[DESCR	RIPTION	١					DA	ATE (Y	R-MO-E	DA)		APPI	ROVE)
С	vend	Redrawn with changes. Table I changes. Delete vendor CAG vendor CAGE 1ES66 for device types 01, 02, and 03. Add ve for device types 01 through 09 sbr					or CAG Add ver	E 1581 ndor C <i>P</i>	8. Add AGE 60	496	92-10-22		M. A. Frye							
D	Char	nges in	accorda	ance wi	th NOF	R 5962-	R015-9	13 sbi	r					92-1	2-04			M. <i>A</i>	A. Frye	
Е	Char	nges in	accorda	ance wi	th NOF	R 5962-	R154-9)4 drv	v					93-0	5-04			M. <i>A</i>	A. Frye	
F	Char	nges in	accorda	ance wi	th NOF	R 5962-	R267-9	4 - sbr						94-0	8-29			M. <i>A</i>	A. Frye	
G	Redr	raw. Ind	corporat	te NOR	's. Edi	itorial cl	hanges	throug	hout d	drw				00-0	4-12		F	Raymor	nd Mon	nin
Н	Add	device t	ype 10.	. Add c	ase ou	tline "X	". Edito	rial cha	anges th	nrougho	out dr	w		03-0	6-03		F	Raymor	nd Mon	nin
J		nge latc								_				03-0	7-28		F	Raymor	nd Mon	nin
REV SHEET REV SHEET				THE	ORIGII	NAL FI	RST PA	AGE OI	F THIS	DRAW	ING H	AS BEI	EN REI	PLACE	D.					
SHEET	l'S			THE		NAL FII	RST P#	AGE OI	F THIS	DRAW	ING H	AS BEI	EN REI	PLACE	D.	Н	Н			
SHEET REV SHEET REV STATU OF SHEETS				REV	, EET											H 10	H 11			
SHEET REV SHEET REV STATU OF SHEETS PMIC N/A	3			REV SHE PREI	EET PAREC	D BY larcia B	J	H 2	Н	Н	H 5	J 6	H 7	H 8	Н 9	10	11 COL	_	SUS	
SHEET REV SHEET REV STATU OF SHEETS PMIC N/A STA		CUIT		REV SHE PREI	EET PAREC	D BY larcia B	J 1	H 2	Н	Н	H 5	J 6	H 7	H 8	Н 9 Y СЕІ JS, О	10 NTER	11 COL 43216	_	SUS	
SHEET REV SHEET REV STATU OF SHEETS PMIC N/A STAMICR DF THIS DRAW FOR	ANDAF ROCIRO RAWIN	CUIT G AVAILAI	BLE	REV SHE PREI	CKED	D BY larcia B BY Ray M	J 1	H 2	Н	H 4	H 5	J 6	H 7	H 8 UPPL UMBI	H 9	NTER HIO 4 cc.dl	11 R COL 43216 a.mil	3	SUS	
SHEET REV SHEET REV STATU OF SHEETS PMIC N/A STAMICR DF THIS DRAW FOR	ANDAR ROCIRO RAWIN VING IS A USE BY PARTMEN ENCIES O	CUIT G AVAILAI ALL NTS OF THE	<u> </u>	REV SHE PREI	PAREC M CKED	D BY larcia B BY Ray N D BY D. A. C	J 1 3. Kelleh	H 2	Н	H 4	H 5	J 6	H 7	H 8 UPPL UMBI D://ww	H 9	NTER HIO 4 cc.dl	11 R COL 43216 a.mil	3	SUS	
SHEET REV SHEET REV STATU OF SHEETS PMIC N/A ST. MICR DF THIS DRAW FOR DEP AND AGI DEPARTM	ANDAR ROCIRO RAWIN VING IS A USE BY PARTMEN ENCIES O	CUIT G AVAILAI ALL NTS OF THE DEFEN	<u> </u>	REV SHE PREI	PAREC M CKED	D BY Ray M D BY D. A. C APPRO	J 1 3. Kelleh Monnin DiCenzo	H 2	Н	H 4	H 5	J 6 EFEN CIRCUS, MO	H 7	H 8 UPPL UMBU D://ww	H 9	NTER HIO 4 cc.dl	11 R COL 43216 a.mil	FET		

1. SCOPE

- 1.1 <u>Scope</u>. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.
 - 1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 <u>Device types</u>. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function	Output current
01	TSC426, MIC426	Dual power MOSFET driver	1.5 A dc
02	TSC427, MIC427	Dual power MOSFET driver	1.5 A dc
03	TSC428, MIC428	Dual power MOSFET driver	1.5 A dc
04	MIC4423	Dual high power MOSFET driver	3.0 A dc
05	MIC4424	Dual high power MOSFET driver	3.0 A dc
06	MIC4425	Dual high power MOSFET driver	3.0 A dc
07	MIC4426	Dual power MOSFET driver with latch proof output for inductive loads	1.5 A dc
08	MIC4427	Dual power MOSFET driver with latch proof output for inductive loads	1.5 A dc
09	MIC4428	Dual power MOSFET driver with latch proof output for inductive loads	1.5 A dc
10	AS404	Dual high power MOSFET driver	2.0 A dc

1.2.2 <u>Case outlines</u>. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	<u>Terminals</u>	Package style
2	CQCC1-N20	20	Square leadless chip carrier
Н	GFP1-F10 or CDFP2-F10	10	Flat pack
Р	GDIP1-T8 or CDIP2-T8	8	Dual-in-line
Χ	CDFP3-F10	10	Flat pack

1.2.3 $\underline{\text{Lead finish}}$. The lead finish is as specified in MIL-PRF-38535, appendix A.

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-88503
DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000		REVISION LEVEL H	SHEET 2

1.3 Absolute maximum ratings.

Supply voltage (V_S) :	
Device types 01 through 03	20 V dc
Device types 04 through 10	22 V dc
Input voltage (V _{IN}):	
Device types 01 through 03	V _S + 0.3 V dc to GND - 0.3 V dc
Device types 04 through 10	Vs + 0.5 V dc to GND - 5.0 V dc
Output current (per pin, capacitance load):	
Device types 01, 02, 03, 07, 08, and 09	1.5 A dc
Device type 10	
Device types 04, 05, and 06	
Peak supply current or GND current (per pin)	
Storage temperature range	
Maximum power dissipation (P _D):	
Case P and X	800 mW 1/
Case 2	
Lead temperature (soldering, 10 seconds)	
Junction temperature (T _J)	
Thermal resistance, junction-to-case (θ _{JC})	
1.4 Recommended operating conditions.	
1.4 Itocommended operating conditions.	
Supply voltage range	$4.5 \text{ V dc} \le V_S \le 18 \text{ V dc}$
Ambient operating temperature range (T _A)	

2. APPLICABLE DOCUMENTS

2.1 <u>Government specification, standards, and handbooks</u>. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.

MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

- $\underline{1}$ / Derate linearly at 6.4 mW/°C above $T_A = +25$ °C.
- 2/ Derate linearly at 14.4 mW/°C above T_A = +25°C.

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2.2 <u>Order of precedence</u>. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

- 3.1 <u>Item requirements</u>. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.
- 3.2 <u>Design, construction, and physical dimensions</u>. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.
 - 3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.
 - 3.2.2 <u>Terminal connections</u>. The terminal connections shall be as specified on figure 1.
- 3.3 <u>Electrical performance characteristics</u>. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.
- 3.4 <u>Electrical test requirements</u>. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.
- 3.5 <u>Marking</u>. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.
- 3.5.1 <u>Certification/compliance mark</u>. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.
- 3.6 <u>Certificate of compliance</u>. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.
- 3.7 <u>Certificate of conformance</u>. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.
- 3.8 <u>Notification of change</u>. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.
- 3.9 <u>Verification and review</u>. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

STANDARD	
MICROCIRCUIT DRAWING	

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		TABLE I. Electrical performar	nce characterist	ics.			
Test	Symbol	Conditions $-55^{\circ}C \le T_A \le +125^{\circ}C$ $4.5 \text{ V} \le V_S \le 18 \text{ V}$	Group A subgroups	Device type	Limits		Unit
		unless otherwise specified			Min	Max	
Logic "1" input voltage	V _{IH}		1, 2, 3	All	2.4		V
Logic "0" input voltage	VIL		1, 2, 3	All		0.8	V
Input voltage range	V _{IN}		1, 2, 3	01, 02, 03	0	Vs	V
	(max)			04, 05, 06, 07, 08, 09, 10	-5	V _S + 0.5	
Input current	I _{IN}	$0 \text{ V} \leq V_{IN} \leq V_{S}$	1	01, 02, 03		±1	μΑ
			2, 3			±10	
			1	04, 05, 06,		±1	
			2, 3	07, 08, 09, 10		±10	
		-5 V ≤ V _{IN} ≤ 0V	1, 2, 3	04, 05, 06,		±10	mA
				07, 08, 09, 10			
High output voltage	V _{OH}	R _L = ∞, <u>1</u> /	1, 2, 3	All	V _S – 25mV		V
Low output voltage	V _{OL}	R _L = ∞, <u>1</u> /	1, 2, 3	All		25	mV
Output resistance	R _{O1}	Apply V _{IN} to force V _{OUT} high,	1, 2, 3	01, 02, 03		20	Ω
		$I_{OUT} = 10 \text{ mA}, V_S = 18 \text{ V}$		04, 05, 06, 10		8	
				07, 08, 09		15	
	R _{O2}	Apply V_{IN} to force V_{OUT} low,	1, 2, 3	01, 02, 03,		15	
		$I_{OUT} = 10 \text{ mA}, V_S = 18 \text{ V}$		07, 08, 09			
				04, 05, 06, 10		8	
Power supply current	I _{S1}	V _{IN} = 3.0 V (both inputs)	1	01, 02, 03,		8.0	mA
			2, 3	07, 08, 09		12	
			1	04, 05, 06,		2.5	
			2, 3	10		4.0	
	I _{S2}	V _{IN} = 0.0 V (both inputs)	1	01, 02, 03,		0.4	
			2, 3	07, 08, 09		0.6	
			1	04, 05, 06,		0.25	
			2, 3	10		0.40	

See footnotes at end of table.

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TABLE I. <u>Electrical performance characteristics</u> - continued. Conditions $-55^{\circ}C \le T_A \le +125^{\circ}C$ Limits Unit Group A Device Symbol Test $4.5~V \leq V_S \leq 18~V$ subgroups type unless otherwise specified Min Max 04, 05, 06, I <u>2</u>/ -500 500 Latch-up protection mΑ 07, 08, 09 10 -100 100 $V_{S} = 18 \ V$ 9, 10, 11 01, 02, 03 60 Rise time <u>3</u>/, <u>4</u>/ 9 04, 05, 06, 35 10, 11 10 60 07, 08, 09 30 10, 11 40 t_{F} $V_S = 18 V$ 9, 10, 11 01, 02, 03 40 Fall time ns 07, 08, 09 <u>3</u>/, <u>4</u>/ 9 04, 05, 06, 35 10, 11 10 60 $V_{S} = 18 \ V$ 9, 10, 11 01, 02, 03 60 Delay time t_{D1} ns <u>3</u>/, <u>4</u>/ 9 04, 05, 06, 75 100 10, 11 10 9 07, 08, 09 30 10, 11 40 01, 02, 03 120 t_{D2} 9, 10, 11 9 04, 05, 06, 75 10, 11 10 100 07, 08, 09 50 10, 11 60

- 1/ Guaranteed by design.
- 2/ Tested initially and after any design changes which may affect the performance of the device.
- 3/ Subgroups 10 and 11 are guaranteed if not tested to the limits as specified in table I herein.
- 4/ For device types 01, 04, and 07, see figure 2. For device types 02, 05, and 08, see figure 3. For device types 03, 06, 09, and 10, inverting drivers, see figure 2. For device types 03, 06, 09, and 10, noninverting drivers, see figure 3.

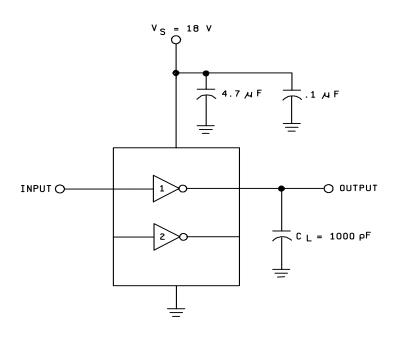
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Device types	01, 04, and 07		02, 05, and 08		03, 06, and 09		06	08	10
Case outlines	Р	2	Р	2	Р	2	Н	Н	Х
Terminal number	Terminal	symbol	Terminal	symbol	Terminal	symbol	Te	rminal symb	ol
1	NC	NC	NC	NC	NC	NC	NC	NC	NC
2	IN A	NC	IN A	NC	IN A	NC	IN A	IN A	IN A
3	GND	NC	GND	NC	GND	NC	GND	GND	GND
4	IN B	IN A	IN B	IN A	IN B	IN A	IN B	IN B	IN B
5	OUTB	NC	OUT B	NC	OUT B	NC	NC	NC	NC
6	Vs	GND	Vs	GND	Vs	GND	NC	NC	NC
7	OUT A	NC	OUT A	NC	OUT A	NC	OUT B	OUT B	OUT B
8	NC	IN B	NC	IN B	NC	IN B	Vs	Vs	Vs
9		NC		NC		NC	OUT A	OUT A	OUT A
10		NC		NC		NC	NC	NC	NC
11		NC		NC		NC			
12		NC		NC		NC			
13		NC		NC		NC			
14		OUTB		OUT B		OUT B			
15		NC		NC		NC			
16		Vs		Vs		Vs			
17		NC		NC		NC			
18		OUT A		OUT A		OUT A			
19		NC		NC		NC			
20		NC		NC		NC			

NC = No connection

FIGURE 1. <u>Terminal connections</u>.

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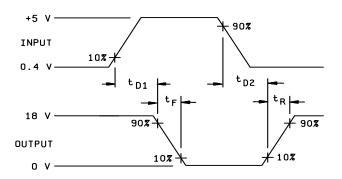
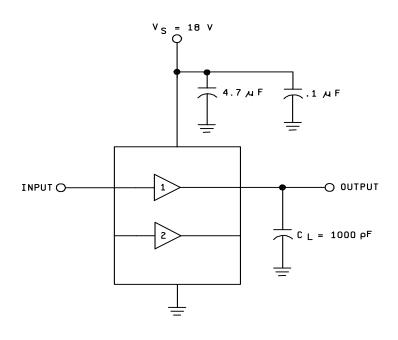


FIGURE 2. Inverting driver switching time.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000 SIZE A FEVISION LEVEL H SHEET 8



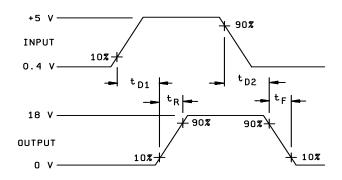


FIGURE 3. Noninverting driver switching time.

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4. QUALITY ASSURANCE PROVISIONS

- 4.1 <u>Sampling and inspection</u>. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.
- 4.2 <u>Screening</u>. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:
 - a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}C$, minimum.
 - b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	
Final electrical test parameters (method 5004)	1*, 2, 3
Group A test requirements (method 5005)	1, 2, 3, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1

^{*} PDA applies to subgroup 1.

- 4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.
 - 4.3.1 Group A inspection.
 - a. Tests shall be as specified in table II herein.
 - b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.
 - c. O/V (latch-up) tests shall be measured only for initial qualification and after process or design changes which may affect the performance of the device. Latch-up tests shall be considered destructive. Test all applicable pins on three devices with zero failures.

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^{**} Subgroups 10 and 11, if not tested shall be guaranteed to the specified limits in table I.

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}C$, minimum.
 - Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

- 5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.
- 6. NOTES
- 6.1 <u>Intended use</u>. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.
- 6.2 <u>Replaceability</u>. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.
- 6.3 <u>Configuration control of SMD's</u>. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.
- 6.4 <u>Record of users</u>. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.
- 6.5 <u>Comments</u>. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.
- 6.6 <u>Approved sources of supply</u>. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD		
MICROCIRCUIT DRAWING		

DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000

SIZE A		5962-88503
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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 03-07-28

Approved sources of supply for SMD 5962-88503 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103.

Standard Microcircuit drawing PIN 1/	Vendor CAGE number	Vendor Similar PIN <u>2</u> /
5962-88503012C	1ES66	TSC426MNP/883B
5962-8850301PA	1ES66	TSC426MJA/883B
	<u>3</u> /	MIC426AJBQ
5962-88503022C	1ES66	TSC427MNP/883B
5962-8850302PA	1ES66	TSC427MJA/883B
	<u>3</u> /	MIC427AJBQ
5962-88503032C	1ES66	TSC428MNP/883B
5962-8850303PA	1ES66	TSC428MJA/883B
	<u>3</u> /	MIC428AJBQ
5962-88503042A	<u>3</u> /	TSC4423MNP/883
5962-8850304PA	<u>3</u> /	TSC4423MJA/883
	<u>3</u> /	MIC4423AJBQ
5962-88503052A	<u>3</u> /	TSC4424MNP/883
5962-8850305PA	60496	MIC4424AJBQ
	<u>3</u> /	TSC4424MJA/883
5962-88503062A	<u>3</u> /	TSC4425MNP/883
5962-8850306HA	<u>3</u> /	MIC4425AWBQ
5962-8850306PA	<u>3</u> /	MIC4425AJBQ
5962-88503072A	<u>3</u> /	TSC4426MNP/883
5962-8850307PA	60496	MIC4426AJBQ
5962-88503082A	<u>3</u> /	TSC4427MNP/883
5962-8850308HA	<u>3</u> /	MIC4427AWBQ
5962-8850308PA	60496	MIC4427AJBQ
5962-88503092A	<u>3</u> /	TSC4428MNP/883
5962-8850309PA	60496	MIC4428AJBQ
5962-8850310XA	0EU86	AS404F10

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ Not available from an approved source of supply.

STANDARD MICROCIRCUIT DRAWING BULLETIN - continued

DATE: 03-07-28

Vendor CAGE
numberVendor name
and address1ES66Maxim Integrated Products
120 San Gabriel Drive
Sunnyvale, CA 94538-512560496Micrel, Inc.
1849 Fortune Drive
San Jose, CA 95131-17240EU86Austin Semiconductor Inc.
8701 Cross Park Dr.

Austin, TX 78754-4566

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