REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R041-92.	91-11-25	M. L. Poelking
B	Changes in accordance with NOR 5962-R211-93.	93-08-13	M. L. Poelking
C	Add device class level V. Update boilerplate throughout. - LTG	97-07-17	T. M. Hess
D	Update boilerplate to MIL-PRF-38535 requirements. - LTG	01-06-14	Thomas M. Hess
E	Update boilerplate to current MIL-PRF-38535 requirements. - CFS	07-06-11	Thomas M. Hess

REV																				
SHEET																				
REV	E	E	E	E	E	E	E	E	E	E										
SHEET	15	16	17	18	19	20	21	22	23	24										

REV STATUS	REV	E	E	E	E	E	E	E	E	E	E	E	E	E	E
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Todd D. Creek

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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Ray Monnin

APPROVED BY
Don Cool

DRAWING APPROVAL DATE
10 June 1988

REVISION LEVEL
E

MICROCIRCUIT, DIGITAL, CMOS, BUS CONTROLLER REMOTE TERMINAL
MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-88628**

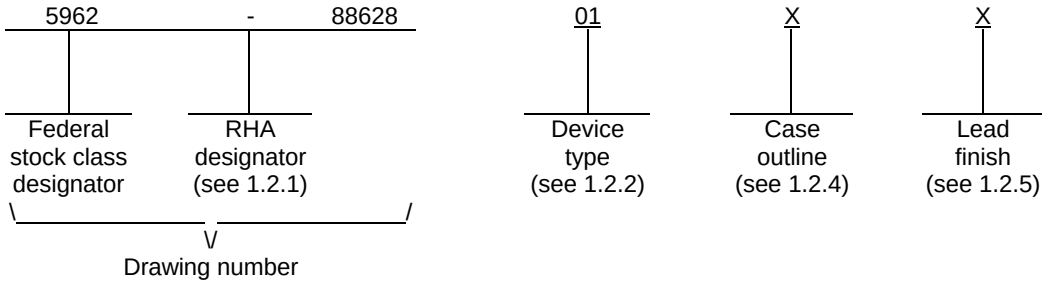
SHEET 1 OF 24

1. SCOPE

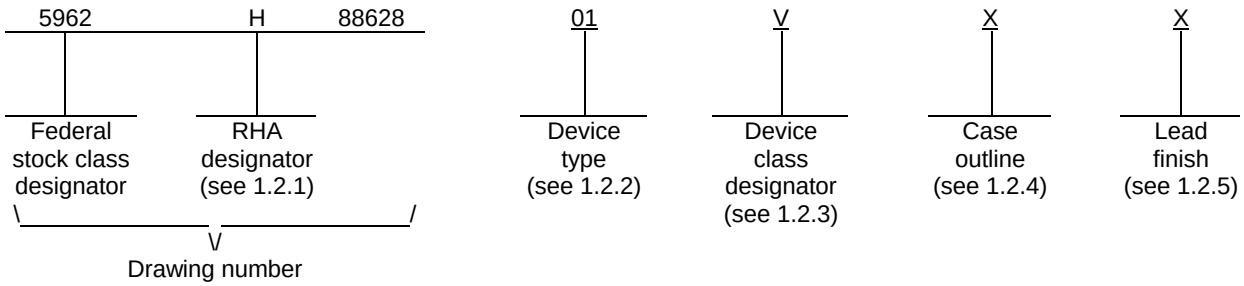
1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following examples.

For device classes M and Q:



For device class V:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	UT1553 BCRT	Bus controller remote terminal

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as listed below. Since the device class designator has been added after the original issuance of this drawing, device classes M and Q designators will not be included in the PIN and will not be marked on the device.

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
T	CQCC1-F132	132	Unformed-lead chip carrier
X	CMGA15-P84	84	Pin grid array
Y	CQCC2-J84	84	"J" lead chip carrier
Z	CQCC1-N84	84	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage range ..... -0.3 V dc to +7.0 V dc
DC input/dc output voltage range ..... -0.3 V dc to (V_{CC}) +0.3 V dc
Storage temperature range ..... -65°C to +150°C
Maximum power dissipation (P_D) ..... 300 mW 2/
Maximum junction temperature (T_J) ..... +175°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Latchup immunity (I_{LU}) ..... ±150 mA
Output short-circuit current (I_{OS}):
A(0-15), D(0-15), $\overline{DMAR}$, $\overline{DMACK}$, $\overline{STDINTL}$, and $\overline{HPINT}$ ..... 100 mA
All other outputs ..... 200 mA

1.4 Recommended operating conditions.

Supply voltage (V_{DD}) ..... 4.5 V dc to 5.5 V dc
Case operating temperature range (T_C) ..... -55°C to +125°C

1.5 Radiation features.

Total dose (Dose rate = 50 – 300 Rads(Si)/s) ..... ≥ 1 x 10^6 Rads (Si)
Single event phenomenon (SEP) effective
linear energy threshold, no upsets or latchup (see 4.4.4.4) ..... ≥ 55 MeV/(mg/cm^2) 3/
Dose rate upset (20 ns pulse) 4/
Dose rate latchup 4/
Dose rate survivability 4/
Neutron irradiated ..... > 1 X 10^{14} 3/

1.6 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests
(MIL-STD-883, test method 5012) ..... 86.5 percent

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Must withstand the added P_D due to short circuit test, e.g. I_{OS}.
3/ Limits are guaranteed by design or process but not production tested unless specified by the customer through the purchase order or contract.
4/ When characterized as a result of the procuring activities request, the condition will be specified.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation or contract.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices

(Copies of these documents are available online at http://www.astm.org or from ASTM International 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA 19428-2959.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 2.

3.2.4 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 3.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $4.5\ V \le V_{DD} \le 5.5\ V$ $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Low level input voltage, TTL inputs	V_{IL}			1, 2, 3	All		0.8	V
High level input voltage, TTL inputs 2/	V_{IH}			1, 2, 3	All	2.0		V
Input leakage current, TTL inputs	I_{IN}	$V_{IN} = V_{DD}$ or V_{SS}		1, 2, 3	All	-1	1	µA
			M, D, P, L, R, F, G, H	1	All	-10	10	
Inputs with pulldown resistors		$V_{IN} = V_{DD}$		1, 2, 3	All	-1	1	
			M, D, P, L, R, F, G, H	1	All	-10	10	
Inputs with pull-up resistors		$V_{IN} = V_{SS}$		1, 2, 3	All	-550	-80	
			M, D, P, L, R, F, G, H	1	All	-900	-150	
Low level output voltage, TTL outputs	V_{OL}	$I_{OL} = 3.2$ mA		1, 2, 3	All		0.4	V
High level output voltage, TTL outputs	V_{OH}	$I_{OH} = -400$ µA		1, 2, 3	All	2.4		V
Three-state output leakage current TTL outputs	I_{OZ}	$V_{OUT} = V_{DD}$ or V_{SS}		1, 2, 3	All	-10	10	µA
Short-circuit output current 3/ 4/	I_{OS}	$V_{DD} = 5.5$ V, $V_{OUT} = V_{DD}$		1, 2, 3	All		100	mA
		$V_{DD} = 5.5$ V, $V_{OUT} = 0$ V		1, 2, 3	All	-100		
Quiescent current 5/	Q_{IDD}			1, 2, 3	All		3	mA
Input capacitance 6/	C_{IN}	See 4.4.1c		4	All		15	pF
Output capacitance 6/	C_{OUT}			4	All		20	pF
Bidirect I/O capacitance 6/	C_{IO}			4	All		25	pF
Functional test		See 4.4.1b		7, 8	All			

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $4.5\ V \le V_{DD} \le 5.5\ V$ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{DMAG}$ (L) to $\overline{DMACK}$ (L)	t_{PHL1}	See figure 3. 7/	9, 10, 11	All	0	45	ns
MCLK (H) to $\overline{RRD}$ (L)	t_{IOHL1}		9, 10, 11	All	0	60	ns
$\overline{RWR}$ (L) to DATA valid 8/	t_{OOZL1}		9, 10, 11	All	0	30	ns
MCLK (H) to MCLKD2 (H)	t_{PLH1}		9, 10, 11	All	0	40	ns
MCLK (H) to $\overline{RWR}$ (L)	t_{IOHL2}		9, 10, 11	All	0	60	ns
$\overline{RD}$ + $\overline{CS}$ (L) to DATA valid	t_{PHL2}		9, 10, 11	All	0	60	ns
$\overline{RD}$ (L) to $\overline{RRD}$ (L)	t_{PHL3}		9, 10, 11	All	0	30	ns
$\overline{WR}$ (L) to $\overline{RWR}$ (L)	t_{PHL4}		9, 10, 11	All	0	30	ns
$\overline{MEMSCI}$ (L) to $\overline{MEMSCO}$ (L)	t_{PHL5}		9, 10, 11	All	0	30	ns

1/ RHA devices supplied to this drawing are characterized at all levels M, D, L, R, F, G and H of irradiation. However, this device is only tested at the 'H' level. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

2/ Radiation hardened technology shall have a V_{IH} pre-irradiation of 2.2 V.

3/ Guaranteed to the limit specified in table I, if not tested.

4/ Not more than one output may be shorted at a time for a maximum duration of one second.

5/ All inputs with internal pull-ups should be left floating. All other inputs should be tied high or low.

6/ The capacitance measurements shall be made between the indicated terminal and ground at a frequency of 1 MHz at T_C of +25°C. The dc bias of the measuring instrument shall 0 ±0.1 V. The ac signal amplitude shall be less than 50 mV RMS.

7/ Switching tests are performed with $V_{IH} = V_{DD}$ and V_{IL} = 0.0 V as input test conditions and output transition times are measured at 1.4 V.

8/ Timing is not valid for RT timer field of message status word. The timer value may update during a DMA memory write.

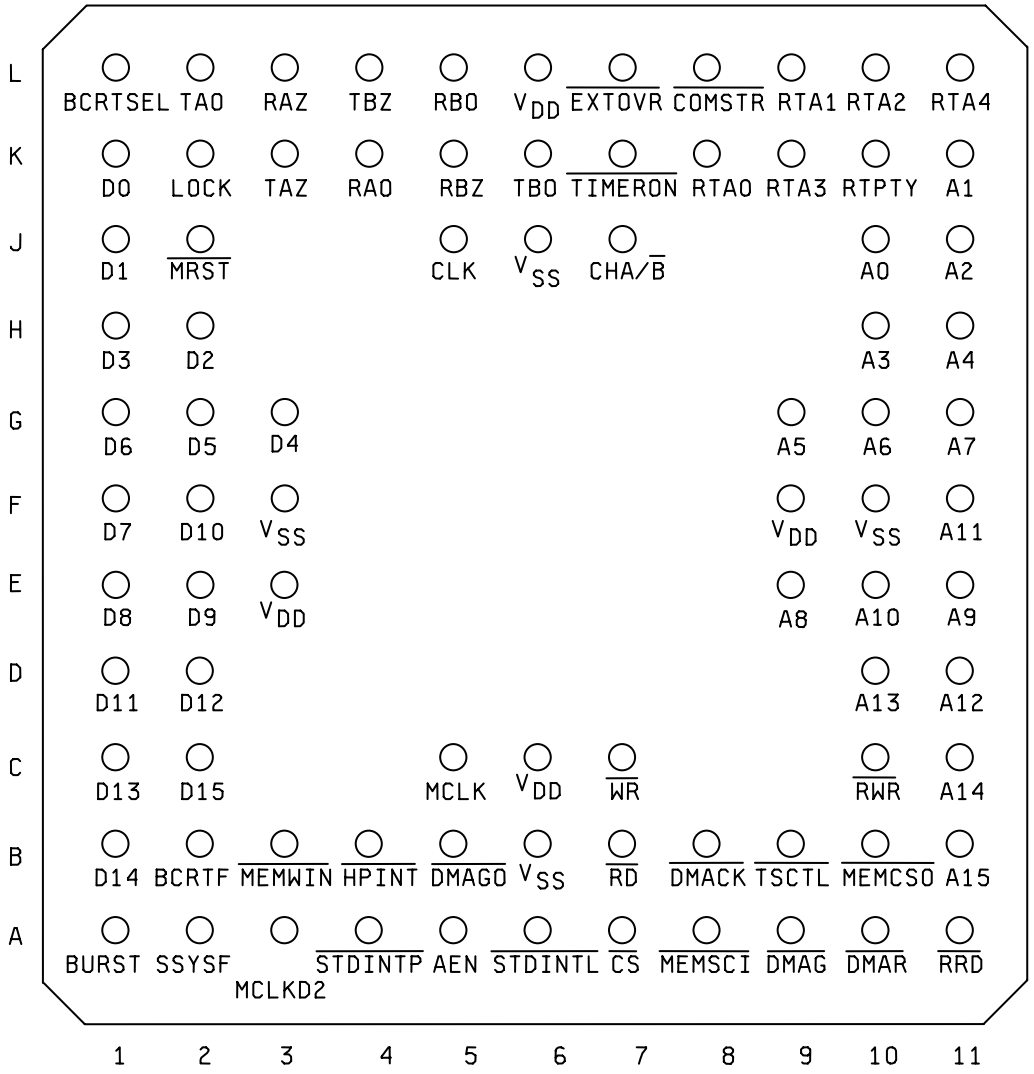
TABLE IB. SEP test limits. 1/ 2/

Device type	T_A = Temperature ±10°C 3/	V_{CC} = 4.5 V		Bias for latch-up test V_{CC} =5.5 V no latch-up LET 3/
		Effective LET No upsets [MEV/(mg/cm^2)]	Maximum device cross section (Cm^2) (LET = 120)	
All	+25°C	≥ 55	≤ 6.7 x 10^{-5}	≤ 80

NOTE: Devices that contain cross coupled resistance must be tested at the maximum rated T_A.

1/ For SEP test conditions, see 4.4.4.4 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Worst case temperature T_A = +125°C.

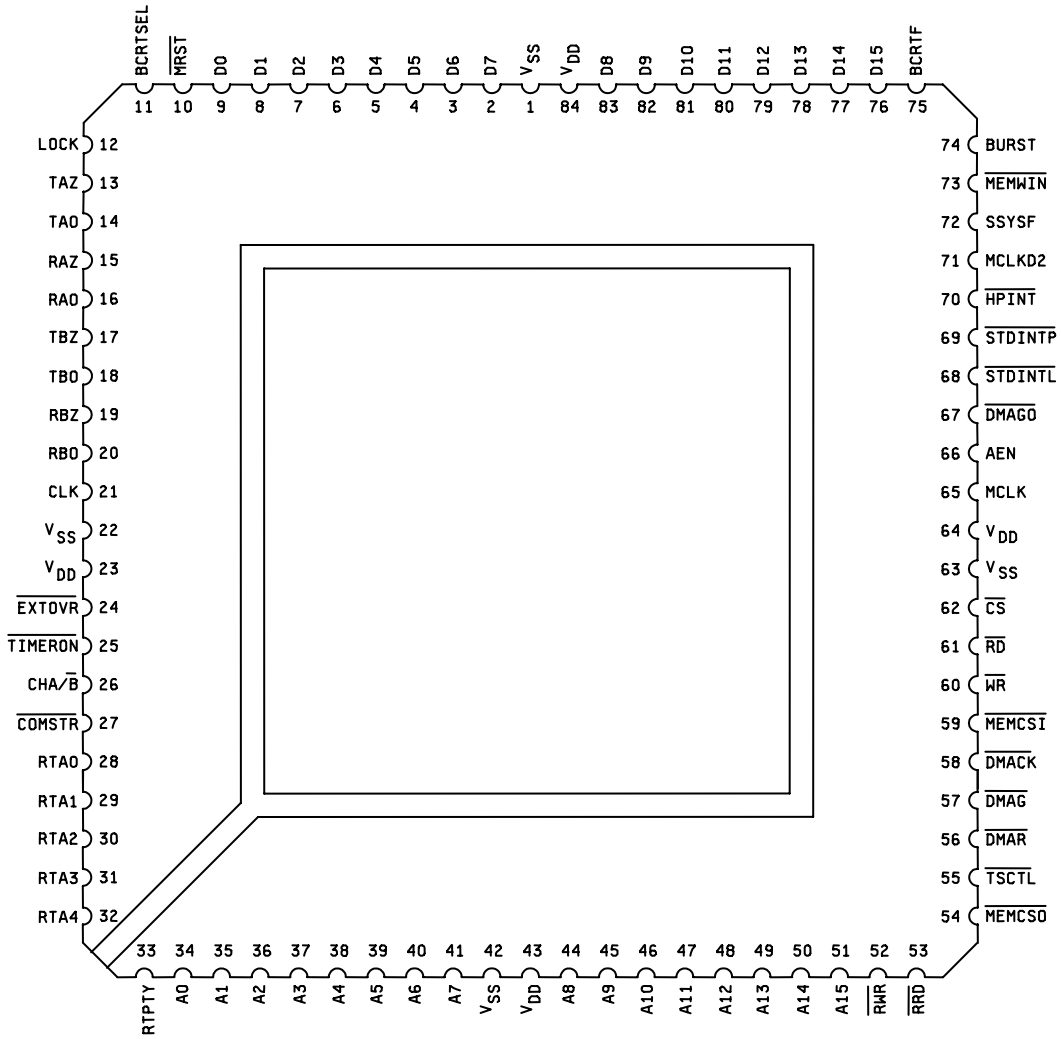
Case X



NOTE: $\overline{\text{MEMWIN}}$ is an internal test pin only and should be considered a floating pin and not for use.

FIGURE 1. Terminal connections.

Cases Y and Z



NOTE: $\overline{\text{MEMWIN}}$ is an internal test pin only and should be considered a floating pin and not for use.

FIGURE 1. Terminal connections - Continued.

Case T

Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	V_{SS}	34	V_{DD}	67	V_{SS}	100	V_{DD}
2	LOCK	35	RTPTY	68	MEMCSO	101	BCRTF
3	TAZ	36	A0	69	TSCTL	102	D15
4	TAO	37	A1	70	DMAR	103	D14
5	NC	38	NC	71	NC	104	NC
6	NC	39	NC	72	DMAG	105	D13
7	RAZ	40	A2	73	NC	106	NC
8	NC	41	A3	74	DMACK	107	D12
9	RAO	42	A4	75	MEMCSI	108	D11
10	TBZ	43	NC	76	NC	109	NC
11	TBO	44	NC	77	WR	110	D10
12	NC	45	A5	78	NC	111	NC
13	RBZ	46	NC	79	RD	112	D9
14	NC	47	A6	80	NC	113	NC
15	RBO	48	NC	81	CS	114	D8
16	V_{SS}	49	V_{SS}	82	V_{SS}	115	V_{DD}
17	V_{DD}	50	V_{DD}	83	V_{DD}	116	V_{SS}
18	CLK	51	A7	84	NC	117	NC
19	NC	52	A8	85	MCLK	118	D7
20	EXTOVR	53	MC	86	AEN	119	D6
21	NC	54	A9	87	NC	120	D5
22	TIMERON	55	NC	88	DMAGO	121	NC
23	NC	56	A10	89	STDINTL	122	D4
24	CHA/B	57	A11	90	STDINTP	123	NC
25	COMSTR	58	A12	91	NC	124	D3
26	NC	59	NC	92	HPINT	125	D2
27	RTAO	60	A13	93	NC	126	NC
28	NC	61	A14	94	MCLKD2	127	D1
29	RTA1	62	NC	95	NC	128	NC
30	RTA2	63	A15	96	SSYSF	129	D0
31	RTA3	64	RWR	97	TEST	130	MRST
32	RTA4	65	RRD	98	BURST	131	BCRTSEL
33	V_{SS}	66	V_{DD}	99	V_{SS}	132	V_{DD}

NOTES:
1. The following terminals are active low: 20, 22, B of terminal 24, 25, 64, 65, 68, 69, 70, 72, 74, 75, 77, 79, 81, 88, 89, 90, 92, and 130.
2. NC = No connection.

FIGURE 1. Terminal connections - Continued.

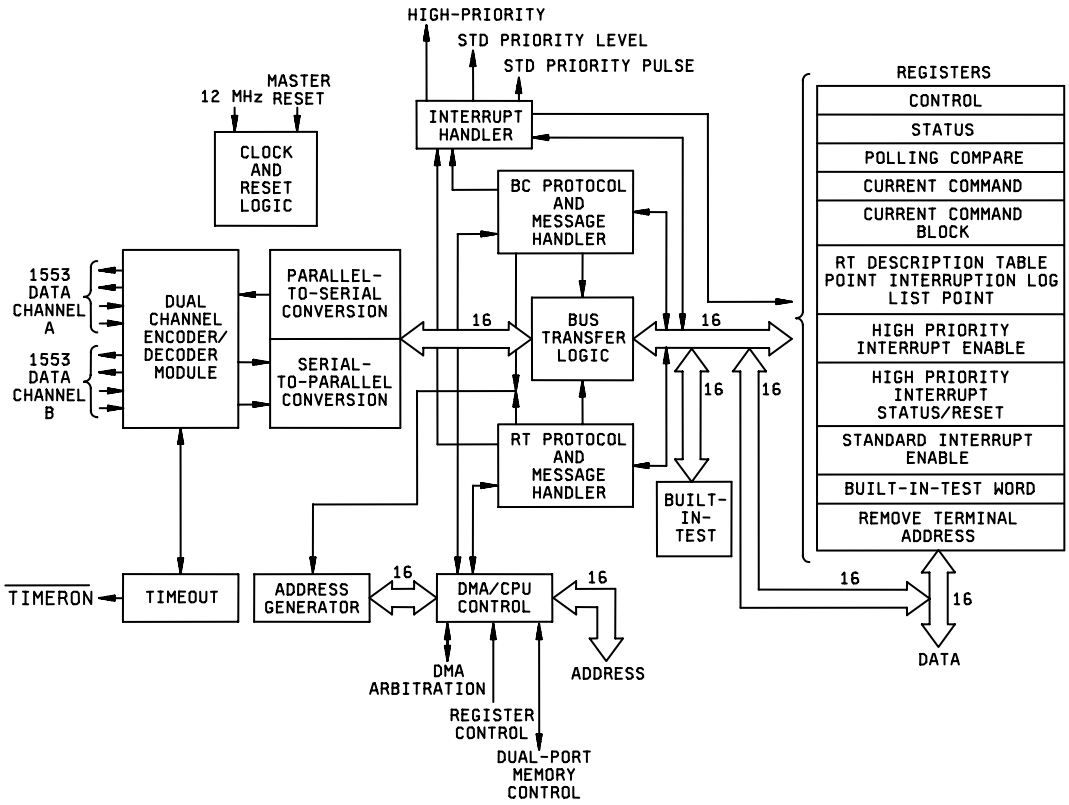
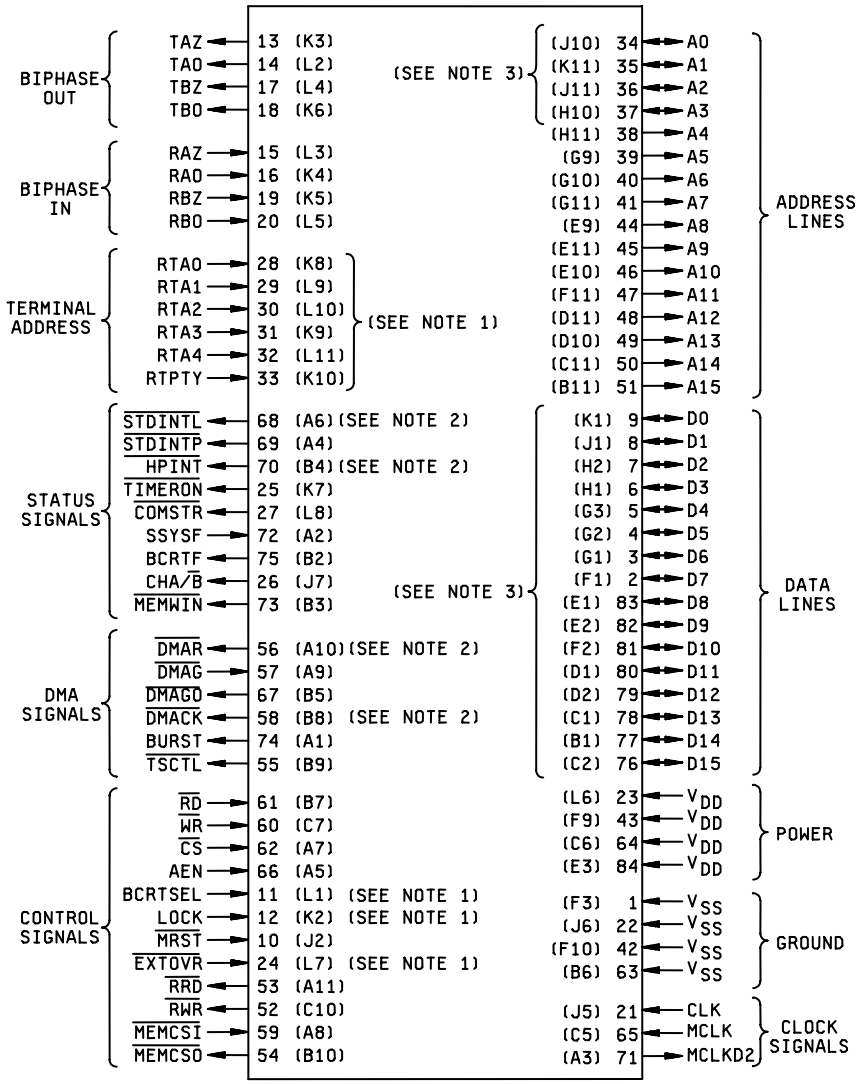
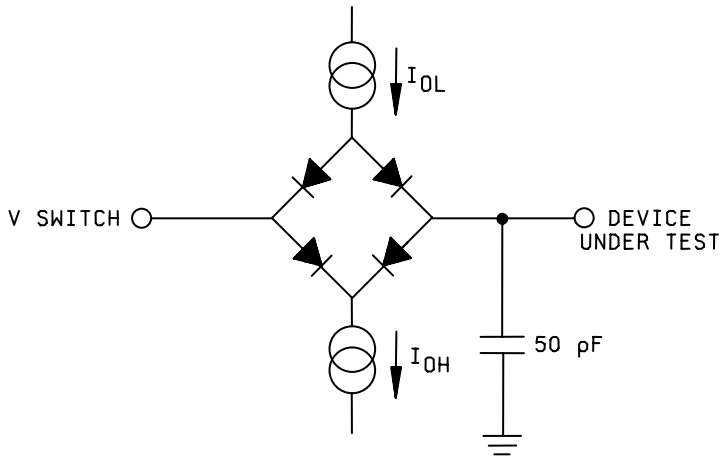


FIGURE 2. Functional block diagram.



NOTES:
1. Pin internally pulled up.
2. Pin at high impedance when not asserted.
3. Bidirectional pin.
4. Case outline X lead identification in parenthesis, cases Y and Z are not in parenthesis.
5. MEMWIN is an internal test pin only and should be considered a floating pin and not for use.

FIGURE 2. Functional block diagram - Continued.



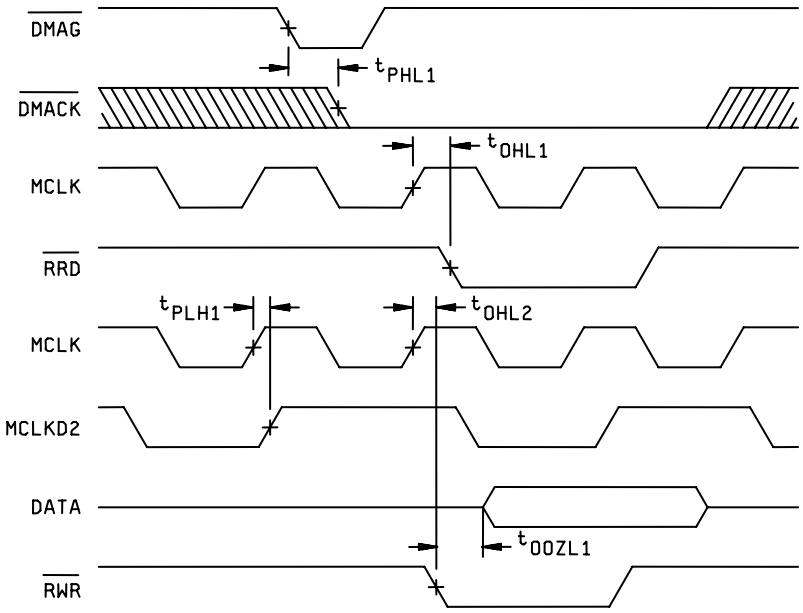


FIGURE 3. Switching waveforms and test circuit.

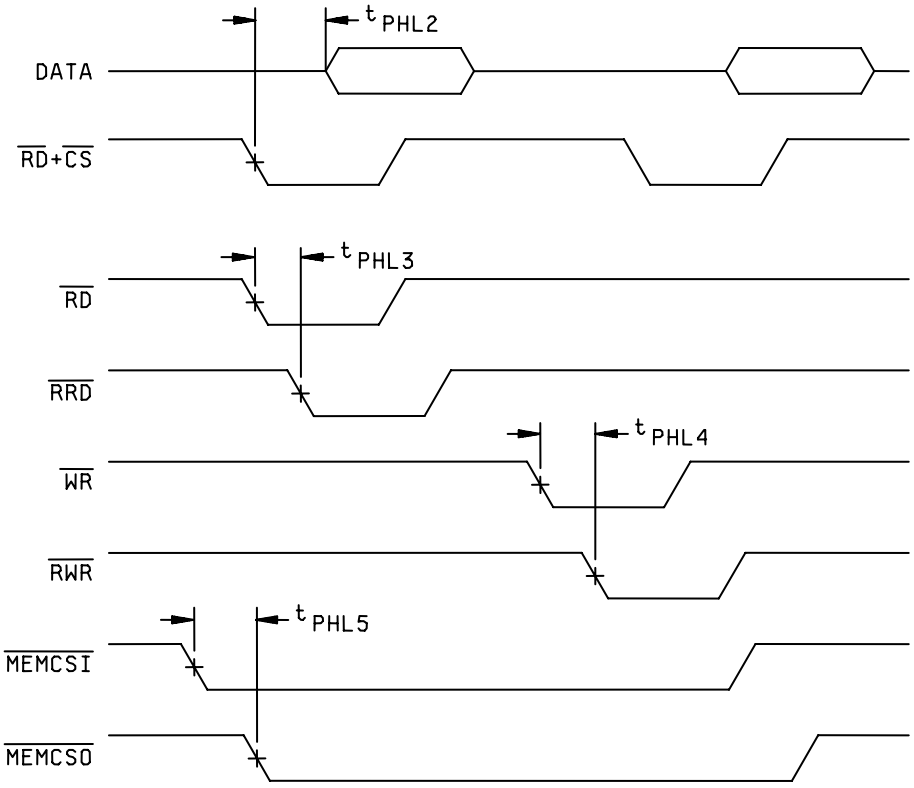


FIGURE 3. Switching waveforms and test circuit - Continued.

Open	V_{DD} = 5 V ±0.5 V	Ground
13 (K3), 14 (L2), 17 (L4), 18 (K6), 25 (K7), 26 (J7), 27 (L8), 38 (H11), 39 (G9), 40 (G10), 41 (G11), 44 (E9), 45 (E11), 46 (E10), 47 (F11), 48 (D11), 49 (D10), 50 (C11), 51 (B11), 52 (C10), 53 (A11), 54 (B10), 55 (B9), 56 (A10), 58 (B8), 67 (B5), 68 (A6), 69 (A4), 70 (B4), 71 (A3), 73 (B3), 74 (A1), 75 (B2), 76 (C2), 77 (B1), 78 (C1), 79 (D2), 80 (D1), 81 (F2), 82 (E2), 83 (E1)	10 (J2), 11 (L1), 12 (K2), 23 (L6), 24 (L7), 28 (K8), 43 (F9), 57 (A9), 59 (A8), 61 (B7), 64 (C6), 84 (E3)	1 (F3), 2 (F1), 3 (G1), 4 (G2) 5 (G3), 6 (H1), 7 (H2), 8 (J1), 9 (K1), 15 (L3), 16 (K4), 19 (K5), 20 (L5), 21 (J5), 22 (J6), 29 (L9), 30 (L10), 31 (K9), 32 (L11), 33 (K10), 34 (J10), 35 (K11), 36 (J11), 37 (H10), 42 (F10), 60 (C7), 62 (A7), 63 (B6), 65 (C5), 66 (A5), 72 (A2)

NOTE: Pin grid array pin identification is in parenthesis. Flat pack pin number is not in parenthesis.

FIGURE 4. Radiation exposure circuit.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.6 herein).

c. Subgroup 4 (C_{IN}, C_{OUT}, and $C_{I/O}$) shall be measured only for the initial test and after process or design changes which may affect capacitance. One pin of each input/output driver (buffer) type shall be tested on each sample device.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	---
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9, 10, 11	1/ 1, 2, 3, 7, 8, 9, 10, 11	2/ 3/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 7, 8A	1, 2, 7, 8A	3/ 1, 2, 7, 8A
Group D end-point electrical parameters (see 4.4)	1, 2, 7, 8A	1, 2, 7, 8A	1, 2, 7, 8A
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.
3/ Delta limits as specified in table IIB herein shall be required when specified and the Delta values shall be completed with reference to the zero hour electrical parameter.

TABLE IIB. Delta limits.

Parameter	Condition	Limits
I_{DDQ}	T_A = 25°C	±10% of measured value or 35 μA, whichever is greater

NOTE: If device is tested at or below 35 μA no deltas are required. Delta's are performed at room temperature.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.
b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A, and as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Neutron testing. When required by the customer, Neutron testing shall be performed in accordance with method 1017 of MIL-STD-883 and herein. All device classes must meet the post irradiation end-point electrical parameter limits as defined inn table IA, for the subgroups specified in table IIA herein at T_A = +25°C ±5°C after an exposure of 2 x 10^{12} neutrons/cm^2 (minimum).

4.4.4.3 Dose rated induced latchup testing. When required by the customer, dose rate induced latchup testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.4 Dose rate upset testing. When required by the customer, dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein.

a. Transient dose rate upset testing for class M devices shall be performed at initial qualification and after any design or process changes which may affect the RHA performance of the devices. Test 10 devices with zero defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535. Device parametric parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-PRF-38535.

4.4.4.5 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° < \text{angle} < 60°$). No shadowing of the ion beam due to fixturing or package related affects is allowed.

b. The fluence shall be ≥ 100 errors or $\geq 10^7$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature $\pm$10°C.

f. Bias conditions shall be V_{CC} = 4.5 V dc for the upset measurements and V_{CC} = 5.5 V dc for the latchup measurements.

g. For SEP test limits, see table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331, or as follows:

Name	Pin number		Type	Active	Description
	Cases Y, Z	Case X			
A0	34	J10	I/O		Bit 0 (LSB) of the address bus
A1	35	K11	I/O		Bit 1 of the address bus
A2	36	J11	I/O		Bit 2 of the address bus
A3	37	H10	I/O		Bit 3 of the address bus
A4	38	H11	OUT		Bit 4 of the address bus
A5	39	G9	OUT		Bit 5 of the address bus
A6	40	G10	OUT		Bit 6 of the address bus
A7	41	G11	OUT		Bit 7 of the address bus
A8	44	E9	OUT		Bit 8 of the address bus
A9	45	E11	OUT		Bit 9 of the address bus
A10	46	E10	OUT		Bit 10 of the address bus
A11	47	F11	OUT		Bit 11 of the address bus
A12	48	D11	OUT		Bit 12 of the address bus
A13	49	D10	OUT		Bit 13 of the address bus
A14	50	C11	OUT		Bit 14 of the address bus
A15	51	B11	OUT		Bit 15 of the address bus
D0	9	K1	I/O		Bit 0 (LSB) of the data bus
D1	8	J1	I/O		Bit 1 of the data bus
D2	7	H2	I/O		Bit 2 of the data bus
D3	6	H1	I/O		Bit 3 of the data bus
D4	5	G3	I/O		Bit 4 of the data bus
D5	4	G2	I/O		Bit 5 of the data bus
D6	3	G1	I/O		Bit 6 of the data bus
D7	2	F1	I/O		Bit 7 of the data bus
D8	83	E1	I/O		Bit 8 of the data bus
D9	82	E2	I/O		Bit 9 of the data bus
D10	81	F2	I/O		Bit 10 of the data bus
D11	80	D1	I/O		Bit 11 of the data bus
D12	79	D2	I/O		Bit 12 of the data bus
D13	78	C1	I/O		Bit 13 of the data bus
D14	77	B1	I/O		Bit 14 of the data bus
D15	76	C2	I/O		Bit 15 of the data bus

Name	Pin number		Type	Active	Description
	Cases Y, Z	Case X			
$\overline{\text{DMAR}}$	56	A10	OUT	ZL	DMA request
$\overline{\text{DMAG}}$	57	A9	IN	AL	DMA grant
$\overline{\text{DMAGO}}$	67	B5	OUT	AL	DMA grant out
$\overline{\text{DMACK}}$	58	B8	OUT	ZL	DMA acknowledge
$\overline{\text{CS}}$	62	A7	IN	AL	Chip select
$\overline{\text{RD}}$	61	B7	IN	AL	Read
$\overline{\text{WR}}$	60	C7	IN	AL	Write
$\overline{\text{MEMCSO}}$	54	B10	OUT	AL	Memory chip select out
$\overline{\text{MEMCSI}}$	59	A8	IN	AL	Memory chip select in
$\overline{\text{RRD}}$	53	A11	OUT	AL	RAM read
$\overline{\text{RWR}}$	52	C10	OUT	AL	RAM write
$\overline{\text{TSCTL}}$	55	B9	OUT	AL	Three state control
AEN	66	A5	IN	AH	Address enable
$\overline{\text{STDINTL}}$	68	A6	OUT	ZL	Standard interrupt level
$\overline{\text{STDINTP}}$	69	A4	OUT	AL	Standard interrupt pulse
$\overline{\text{HPINT}}$	70	B4	OUT	ZL	High priority interrupt
CLK	21	J5	IN		Clock
MCLK	65	C5	IN		Memory clock
MCLKD2	71	A3	OUT		Memory clock divided by two
TAZ	13	K3	OUT		Transmit (channel) A Z
TAO	14	L2	OUT		Transmit (channel) A O
TBZ	17	L4	OUT		Transmit (channel) B Z
TBO	18	K6	OUT		Transmit (channel) B O
RAZ	15	L3	IN		Receive (channel) A Z
RAO	16	K4	IN		Receive (channel) A O
RBZ	19	K5	IN		Receive (channel) B Z
RBO	20	L5	IN		Receive (channel) B O
$\overline{\text{TIMERON}}$	25	K7	OUT	AL	(RT) timer on
CHA/$\overline{\text{B}}$	26	J7	OUT		Channel A/$\overline{\text{B}}$
$\overline{\text{MRST}}$	10	J2	IN	AL	Master reset
$\overline{\text{COMSTR}}$	27	L8	OUT	AL	(RT) command strobe
BCRTSEL	11	L1	IN		BC/$\overline{\text{RT}}$ select

Name	Pin number		Type	Active	Description
	Cases Y, Z	Case X			
RTA0	28	K8	IN		Remote terminal address bit 0 (LSB)
RTA1	29	L9	IN		Remote terminal address bit 1
RTA2	30	L10	IN		Remote terminal address bit 2
RTA3	31	K9	IN		Remote terminal address bit 3
RTA4	32	L11	IN		Remote terminal address bit 4
RTPTY	33	K10	IN	AH	Remote terminal (address) parity
SSYSF	72	A2	IN	AH	Subsystem fail
BCRTF	75	B2	OUT	AH	BCRT fail
BURST	74	A1	OUT	AL	Burst (DMA cycle)
$\overline{\text{MEMWIN}}$	73	B3	OUT		Memory (access) window
LOCK	12	K2	IN	AH	Lock
$\overline{\text{EXTOVR}}$	24	L7	IN	AL	External override
V_{DD}	23	L6	PWR		+5 V
V_{DD}	43	F9	PWR		+5 V
V_{DD}	64	C6	PWR		+5 V
V_{DD}	84	E3	PWR		+5 V
V_{SS}	1	F3	GND		Ground
V_{SS}	22	J6	GND		Ground
V_{SS}	42	F10	GND		Ground
V_{SS}	63	B6	GND		Ground

NOTES:
1. $\overline{\text{MEMWIN}}$ is an internal test pin only and should be considered a floating pin and not for use.
2. Abbreviations:
   - AL = Active low
   - AH = Active high
   - ZL = Active low – inactive state is high impedance.
3. Address and data busses are all active high and in the high impedance state when idle.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Additional information. A copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

e. Occurrence of latchup (SEP).

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 07-06-11

Approved sources of supply for SMD 5962-88628 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8862801XA	65342	UT1553 BCRTGA
5962-8862801XC	65342	UT1553 BCRTGC
5962-8862801YA	65342	UT1553 BCRTWA
5962-8862801YC	65342	UT1553 BCRTWC
5962-8862801ZA	65342	UT1553 BCRTAA
5962-8862801ZC	65342	UT1553 BCRTAC
5962-8862801TA	65342	UT1553 BCRTFA
5962-8862801TC	65342	UT1553 BCRTFC
5962H8862801XA	65342	UT1553 BCRTGAH
5962H8862801XC	65342	UT1553 BCRTGCH
5962H8862801YA	65342	UT1553 BCRTWAH
5962H8862801YC	65342	UT1553 BCRTWCH
5962H8862801ZA	65342	UT1553 BCRTAAH
5962H8862801ZC	65342	UT1553 BCRTACH
5962H8862801TA	65342	UT1553 BCRTFAH
5962H8862801TC	65342	UT1553 BCRTFCH
5962H8862801VXA	65342	UT1553 BCRTVGAH
5962H8862801VXC	65342	UT1553 BCRTVGCH
5962H8862801VYA	65342	UT1553 BCRTVWAH
5962H8862801VYC	65342	UT1553 BCRTVWCH
5962H8862801VZA	65342	UT1553 BCRTVAAH
5962H8862801VZC	65342	UT1553 BCRTVACH
5962H8862801VTA	65342	UT1553 BCRTVFAH
5962H8862801VTC	65342	UT1553 BCRTVFCH

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65342	Aeroflex Colorado Springs, Inc. 4350 Centennial Blvd. Colorado Springs, CO 80907-3486