REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Added device types 03, 04, 05, and 06. Added electrical test limits for device types 03, 04, 05, and 06 to table I. Added vendor CAGE code 34335. Editorial changes throughout.	90-05-09	William K. Heckman
B	Added device types 07, 08, 09, and 10. Added electrical parameters testing to table I for device types 07, 08, 09, and 10. Added a new package for device type 07. Editorial changes throughout.	92-03-25	Monica L. Poelking
C	Added vendor CAGE code 0C7V7. Update boilerplate to MIL-PRF-38535 requirements. – LTG	02-12-18	Thomas M. Hess

REV																				
SHEET																				
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C						
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28						

REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Tim H. Noh

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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS

AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Tim H.Noh

APPROVED BY
William K. Heckman

MICROCIRCUIT, DIGITAL, CMOS, SERIAL COMMUNICATION CONTROLLER, MONOLITHIC SILICON

DRAWING APPROVAL DATE
89-02-06

REVISION LEVEL	SIZE	CAGE CODE	
C	A	**67268**	**5962-88689**

SHEET 1 OF 28

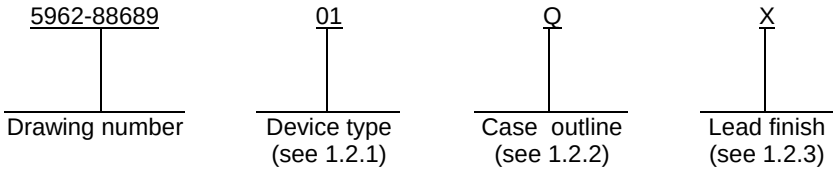
DSCC FORM 2233
APR 97

5962-E130-03

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Frequency	Circuit function
01	Z85C3006	6.0 MHz	Serial communication controller
02	Z85C3008	8.0 MHz	Serial communication controller 2/
03	AM85C30-10	10.0 MHz	Serial communication controller with SDLC enhancements 1/
04	AM85C30-12	12.0 MHz	Serial communication controller with SDLC enhancements
05	AM85C30-16	16.0 MHz	Serial communication controller with SDLC enhancements 1/
06	AM85C30-08	8.0 MHz	Serial communication controller with SDLC enhancements 1/
07	Z85C3010	10.0 MHz	Serial communication controller 3/
08	Z8523010	10.0 MHz	Serial communication controller with SDLC enhancements 1/
09	Z8523016	16.0 MHz	Serial communication controller with SDLC enhancements 1/
10	Z8523008	8.0 MHz	Serial communication controller with SDLC enhancements 1/

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Q	GDIP1-T40 or CDIP2-T40	40	Dual-in-line package
X	GQCC1-J44	44	Square “J” lead chip carrier
Y	CQCC1-N44	44	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1/ Device types 03, 05, 06, 08, 09, and 10 are not functionally identical.

2/ Device type 02 is not functionally identical with device types 06 or 10.

3/ Device type 07 is not functionally identical with device types 03 or 08.

1.3 Absolute maximum ratings.

V_{CC} supply voltage range (referenced to ground)..... -0.3 V dc to +7.0 V dc
Voltage on any pin (referenced to ground)..... -0.3 V dc to +7.0 V dc
Storage temperature range (T_{STG})..... -65°C to +150°C
Maximum power dissipation (P_D)..... 0.5 W
Lead temperature (soldering, 10 seconds) ..... +270°C
Maximum operating junction temperature (T_J) ..... +180°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage (V_{CC})..... 4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage (V_{IH}) ..... 2.2 V dc
Maximum low level input voltage (V_{IL}) ..... 0.8 V dc
Frequency of operation:
  Device type 01 ..... 0.5 MHz to 6.0 MHz
  Device types 02, 06, 10 ..... 0.5 MHz to 8.0 MHz
  Device types 03, 07, 08 ..... 0.5 MHz to 10 MHz
  Device type 04 ..... 0.5 MHz to 12.5 MHz
  Device types 05 and 09 ..... 0.5 MHz to 16.4 MHz
Case operating temperature range (T_C) ..... -55°C to +125°C
Clock rise and fall times:
  Device type 09 ..... 5 ns maximum
  Device type 05 ..... 8 ns maximum
  Device types 01, 02, 03, 04, 06, 07, 08, 10 ..... 10 ns maximum

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Timing waveforms and test circuits. The timing waveforms and test circuits shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 and QML-38535 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V ±10% unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High input voltage	V_{IH}		1, 2, 3	All	2.2	V_{CC}+0.3 2/	V
Low input voltage	V_{IL}		1, 2, 3	All	-0.3 2/	0.8	V
Logic low output voltage	V_{OL}	I_{OL} = 2.0 mA, V_{CC} = 4.5 V	1, 2, 3	All		0.5	V
Logic high output voltage	V_{OH1}	I_{OH} = -1.6 mA, V_{CC} = 4.5 V	1, 2, 3	All	2.4		V
	V_{OH2}	I_{OH} = -250 µA, V_{CC} = 4.5 V	1, 2, 3	All	V_{CC}-0.8		V
Power supply current	I_{CC}	V_{IH} = 4.8 V V_{IL} = 0.2 V V_{CC} = 5.0 V Oscillator off	1, 2, 3	01,02,06		30	mA
			1, 2, 3	03,07,08		18	
			1, 2, 3	04,05,09		22	
			1, 2, 3	10		15	
Output leakage current low	I_{LOL}	V_{OUT} = 0.4 V, V_{CC} = 5.5 V	1, 2, 3	All	-10		µA
Output leakage current high	I_{LOH}	V_{OUT} = 2.4 V, V_{CC} = 5.5 V	1, 2, 3	All		+10	
Input low current	I_{IL}	V_{IN} = 0.4 V, V_{CC} = 5.5 V	1, 2, 3	All	-10		
Input high current	I_{IH}	V_{IN} = 2.4 V, V_{CC} = 5.5 V	1, 2, 3	All		+10	
Input capacitance	C_{IN}	fc = 1.0 MHz See 4.3.1c	4	All		10	pF
Output cpacitance	C_{OUT}		4	All		15	
Bidirectional capacitance	$C_{I/O}$		4	All		20	
Functional test		See 4.3.1d V_{CC} = 4.5 V, 5.5 V	7, 8	All			
Maximum frequency	f_{MAX}	See figure 3 V_{CC} = 4.5 V	9, 10, 11	05, 09	16.0		MHz
				04	12.0		
				03,07,08	10.0		
				02,06,10	8.0		
				01	6.0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V ±10% unless otherwise specified	Group A subgroups	Ref no.	Device type	Limits		Unit
						Min	Max	
PCLK low width	t_{wPCL}	See figure 3, read and write, interrupt, reset, and cycle timings. C_L = 50 pF ±10% V_{CC} = 4.5 V	9, 10, 11	1	01	70	1000	ns
					02,06,10	50	1000	
					03,07,08	40	1000	
					04	34	1000	
					05, 09	26	1000	
PCLK high width	t_{wPCH}		9, 10, 11	2	01	70	1000	ns
					02,06,10	50	1000	
					03,07,08	40	1000	
					04	34	1000	
					05, 09	26	1000	
PCLK fall time 2/ 3/	t_{fPC}		9, 10, 11	3	01,02,03, 04,06,07, 08, 10		10	ns
					05		8	
					09		5	
PCLK rise time 2/ 3/	t_{rPC}		9, 10, 11	4	01,02,03, 04,06,07, 08, 10		10	ns
					05		8	
					09		5	
PCLK cycle time	t_{cPC}		9, 10, 11	5	01	165	2000	ns
					02,06,10	125	2000	
					03,07,08	100	2000	
					04	80	2000	
					05, 09	61	2000	
Address to $\overline{WR}$ ↓ setup time	$t_{sA(WR)}$		9, 10, 11	6	01	80		ns
					02,06,10	70		
					03,07,08	50		
					04	45		
					05, 09	35		
Address to $\overline{WR}$ ↑ hold time	$t_{hA(WR)}$		9, 10, 11	7	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V ±10% unless otherwise specified	Group A subgroups	Ref no.	Device type	Limits		Unit
						Min	Max	
Address to $\overline{RD}$ ↓ setup time	$t_{sA(RD)}$	See figure 3, read and write, interrupt, reset, and cycle timings. C_L = 50 pF ±10% V_{CC} = 4.5 V	9, 10, 11	8	01	80		ns
					02,06,10	70		
					03,07,08	50		
					04	45		
					05, 09	35		
Address to $\overline{RD}$ ↑ hold time	$t_{hA(RD)}$		9, 10, 11	9	All	0		ns
$\overline{INTACK}$ to PCLK ↑ setup time 4/	$t_{sIA(PC)}$		9, 10, 11	10	01,02,03, 06,07,08, 10	20		ns
					04,05,09	15		
$\overline{INTACK}$ to $\overline{WR}$ ↓ setup time 5/	$t_{sIAi(WR)}$		9, 10, 11	11	01	160		ns
					02,06,10	145		
					07	130		
					03, 08	120		
					04	95		
					05, 09	70		
$\overline{INTACK}$ to $\overline{WR}$ ↑ hold time	$t_{hIA(WR)}$		9, 10, 11	12	All	0		ns
$\overline{INTACK}$ to $\overline{RD}$ ↓ setup time 5/	$t_{sIAi(RD)}$		9, 10, 11	13	01	160		ns
					02,03,06, 07,08,10	145		
					04	95		
					05, 09	70		
$\overline{INTACK}$ to $\overline{RD}$ ↑ hold time 4/	$t_{sIAi(RD)}$		9, 10, 11	14	All	0		ns
$\overline{INTACK}$ to PCLK ↑ hold time	$t_{hIA(PC)}$		9, 10, 11	15	01	100		ns
					02,06,10	40		
					03,07,08	30		
					04	20		
					05, 09	15		
$\overline{CE}$ low to $\overline{WR}$ ↓ setup time	$t_{sCEL(WR)}$		9, 10, 11	16	All	0		ns
$\overline{CE}$ to $\overline{WR}$ ↑ hold time	$t_{hCE(WR)}$		9, 10, 11	17	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V ±10% unless otherwise specified	Group A subgroups	Ref no.	Device type	Limits		Unit
						Min	Max	
$\overline{CE}$ high to $\overline{WR}$ ↓ setup time	$t_{sCEh(WR)}$	See figure 3, read and write, interrupt, reset, and cycle timings. C_L = 50 pF ±10% V_{CC} = 4.5 V	9, 10, 11	18	01	70		ns
					02,06,10	60		
					03,07,08	50		
					04	40		
					05, 09	30		
$\overline{CE}$ low to $\overline{RD}$ ↓ setup time 5/	$t_{sCEL(RD)}$		9, 10, 11	19	All	0		ns
$\overline{CE}$ to $\overline{RD}$ ↑ hold time 5/	$t_{hCE(RD)}$		9, 10, 11	20	All	0		ns
$\overline{CE}$ high to $\overline{RD}$ ↓ setup time 5/	$t_{sCEh(RD)}$		9, 10, 11	21	01	70		ns
					02,06,10	60		
					03,07,08	50		
					04	40		
					05, 09	30		
$\overline{RD}$ low width 5/	t_{wRDL}		9, 10, 11	22	01	200		ns
					02,06,10	150		
					03,07,08	125		
					04	90		
					05, 09	75		
$\overline{RD}$ ↓ to read data active delay 2/	$t_{dRD(DRA)}$		9, 10, 11	23	All	0		ns
$\overline{RD}$ ↑ to read data not valid delay 2/	$t_{dRDr(DR)}$		9, 10, 11	24	All	0		ns
$\overline{RD}$ ↓ to read data valid delay	$t_{dRDf(DR)}$		9, 10, 11	25	01		180	ns
					02,06,10		140	
					03,07,08		125	
					04		90	
					05, 09		70	
$\overline{RD}$ ↑ to read data float delay 2/ 6/	$t_{dRD(DRZ)}$		9, 10, 11	26	01		45	ns
					02,06,10		40	
					03,07,08		35	
					09		30	
					04		25	
					05		20	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V ±10% unless otherwise specified	Group A subgroups	Ref no.	Device type	Limits		Unit
						Min	Max	
Address required valid to read data valid delay	$t_{dA(DR)}$	See figure 3, read and write, interrupt, reset, and cycle timings. C_L = 50 pF ±10% V_{CC} = 4.5 V	9, 10, 11	27	01		280	ns
					02,06,10		220	
					07		180	
					03, 08		160	
					04		120	
					05, 09		100	
$\overline{WR}$ low width	t_{wWRL}		9, 10, 11	28	01	200		ns
					02,06,10	150		
					03,07,08	125		
					04	90		
					05, 09	75		
$\overline{WR}$ ↓ to write data valid	$t_{sDW(WR)}$		9, 10, 11	29	03,06,07		35	ns
					04		25	
					05,08,09, 10		20	
					01, 02		0	
WRITE data to $\overline{WR}$ hold time	$t_{hDW(WR)}$		9, 10, 11	30	All	0		ns
$\overline{WR}$ ↓ to wait valid delay 7/	$t_{dWR(W)}$		9, 10, 11	31	01		200	ns
					02,06,10		170	
					07		160	
					03, 08		100	
					04		70	
					05, 09		50	
$\overline{RD}$ ↓ to wait valid delay 7/	$t_{dRD(W)}$		9, 10, 11	32	01		200	ns
					02,06,10		170	
					07		160	
					03, 08		100	
					04		70	
					05, 09		50	
$\overline{WR}$ ↓ to $\overline{W/REQ}$ not valid delay	$t_{dWRf(REQ)}$		9, 10, 11	33	01		200	ns
					02,06,10		170	
					07		160	
					03, 08		120	
					04		100	
					05, 09		70	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V ±10% unless otherwise specified	Group A subgroups	Ref no.	Device type	Limits		Unit
						Min	Max	
$\overline{RD}$ ↓ to $\overline{W/REQ}$ not valid delay	$t_{dRDf(REQ)}$	See figure 3, read and write, interrupt, reset, and cycle timings. C_L = 50 pF ±10% V_{CC} = 4.5 V	9, 10, 11	34	01		200	ns
					02,06,10		170	
					07		160	
					03, 08		120	
					04		100	
					05, 09		70	
$\overline{WR}$ ↓ to $\overline{DTR/REQ}$ not valid delay	$t_{dWRr(REQ)}$		9, 10, 11	35	All		4.0 t_{cPC}	ns
$\overline{WR}$ ↓ to $\overline{DTR/REQ}$ not valid delay	$t_{dWRr(EREQ)}$ 8/		9, 10, 11	35	03,06,08, 10		120	ns
					04		100	
					05, 09		70	
$\overline{RD}$ ↑ to $\overline{DTR/REQ}$ not valid delay	$t_{dRDr(REQ)}$		9, 10, 11	36	All		4.0 t_{cPC}	ns
PCLK ↓ to $\overline{INT}$ valid delay 7/	$t_{dPC(INT)}$		9, 10, 11	37	01,02,06, 07, 10		500	ns
					03		400	
					04		350	
					08		320	
					05, 09		175	
$\overline{INTACK}$ to $\overline{RD}$ ↓ (acknowledge) delay 9/	$t_{dIAi(RD)}$		9, 10, 11	38	01	200		ns
					02,06,10	150		
					03,07,08	125		
					04	95		
					05, 09	50		
$\overline{RD}$ (acknowledge) width	t_{wRDA}		9, 10, 11	39	01	200		ns
					02,06,10	150		
					03,07,08	125		
					04	95		
					05, 09	75		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V ±10% unless otherwise specified	Group A subgroups	Ref no.	Device type	Limits		Unit
						Min	Max	
$\overline{RD}$ ↓ (acknowledge) to read data valid delay	$t_{dRDA(DR)}$	See figure 3, read and write, interrupt, reset, and cycle timings. C_L = 50 pF ±10% V_{CC} = 4.5 V	9, 10, 11	40	01		180	ns
					02,03,06, 07,08,10		140	
					04		90	
					05, 09		70	
IEI to $\overline{RD}$ ↓ (acknowledge) setup time	$t_{sIEI(RDA)}$		9, 10, 11	41	01	100		ns
					02,03,06, 07,08,10	95		
					04	65		
					05, 09	50		
IEI to $\overline{RD}$ ↑ (acknowledge) hold time	$t_{hIEI(RDA)}$		9, 10, 11	42	All	0		ns
IEI to IEO delay time	$t_{dIEI(IEO)}$		9, 10, 11	43	01		100	ns
					02,03,06, 07,08,10		95	
					04		65	
					05, 09		45	
PCLK ↑ to IEO delay	$t_{dPC(IEO)}$		9, 10, 11	44	01		250	ns
					02,03,06, 07		200	
					08		175	
					04		130	
					05, 09		80	
$\overline{RD}$ ↓ to $\overline{INT}$ inactive delay 7/	$t_{dRA(INT)}$		9, 10, 11	45	01,02,06, 07		500	ns
					03, 10		450	
					08		320	
					04		260	
					05, 09		200	
$\overline{RD}$ ↑ to $\overline{WR}$ ↓ delay for no reset 2/	$t_{dRD(WRQ)}$		9, 10, 11	46	01,02,03, 06,07,08, 10	15		ns
					04,05,09	10		
$\overline{WR}$ ↑ to $\overline{RD}$ ↓ delay for no reset 2/	$t_{dWRQ(RD)}$		9, 10, 11	47	01	30		ns
					02,03,06, 07,08,10	15		
					04,05,09	10		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V ±10% unless otherwise specified	Group A subgroups	Ref no.	Device type	Limits		Unit
						Min	Max	
$\overline{WR}$ and $\overline{RD}$ coincident low for reset 2/	t_{wRES}	See figure 3, read and write, interrupt, reset, and cycle timings. C_L = 50 pF ±10% V_{CC} = 4.5 V	9, 10, 11	48	01	200		ns
					02,03,06, 10	150		
					07, 08	100		
					04	85		
					05, 09	75		
Valid access recovery time 2/ 10/	t_{rC}		9, 10, 11	49	01,02,06, 07,08,09, 10	4.0 t_{cPC}		ns
					03,04,05	3.5 t_{cPC}		
PCLK ↓ to W/REQ valid delay	$t_{dPC(REQ)}$	See figure 3, general timings. C_L = 50 pF ±10% V_{CC} = 4.5 V	9, 10, 11	1	01,02,06, 07, 10		250	ns
					03, 08		150	
					04		120	
					05, 09		80	
PCLK ↓ to wait inactive delay	$t_{dPC(W)}$		9, 10, 11	2	01,02,06, 07, 10		350	ns
					03, 08		250	
					04		220	
					05, 09		180	
$\overline{RxC}$ ↑ to PCLK ↑ setup time (PCLK ÷ 4 case only) 11/ 12/	$t_{sRXC(PC)}$		9, 10, 11	3	01	70	t_{wPCL}	ns
					02, 06	60	t_{wPCL}	
					07	40	t_{wPCL}	
					03,04,05, 08,09,10	0		
RxD to $\overline{RxC}$ ↑ setup time (X1 mode) 11/	$t_{sRXD(RXCr)}$		9, 10, 11	4	All	0		ns
RxD to $\overline{RxC}$ ↑ hold time (X1 mode) 11/	$t_{hRXD(RXCf)}$		9, 10, 11	5	01,02,06, 07, 10	150		ns
					03, 08	125		
					04	100		
					05, 09	50		
RxD to $\overline{RxC}$ ↓ setup time (X1 mode) 11/ 13/	$t_{sRXD(RXCf)}$		9, 10, 11	6	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{CC} = 5.0\ V \pm 10\%$ unless otherwise specified	Group A subgroups	Ref no.	Device type	Limits		Unit
						Min	Max	
RxD to $\overline{RxC}$ ↓ hold time (X1 mode) 11/ 13/	$t_{hRXD(RXCf)}$	See figure 3, general timings. $C_L = 50\ pF \pm 10\%$ $V_{CC} = 4.5\ V$	9, 10, 11	7	01,02,06, 07, 10	150		ns
					03, 08	125		
					04	100		
					05, 09	50		
$\overline{SYNC}$ to $\overline{RxC}$ ↑ setup time 11/	$t_{sSY(RXC)}$		9, 10, 11	8	01,02,06, 07, 10	-200		ns
					03, 08	-150		
					04	-125		
					05, 09	-100		
$\overline{SYNC}$ to $\overline{RxC}$ ↑ hold time 11/	$t_{hSY(RXC)}$		9, 10, 11	9	All	5.0 t_{cPC}		ns
$\overline{TxC}$ ↓ to PCLK ↑ setup time 12/ 14/	$t_{sTXC(PC)}$		9, 10, 11	10	All	0		ns
$\overline{TxC}$ ↓ to TxD 14/ delay (X1 mode)	$t_{dTXCf(TXD)}$		9, 10, 11	11	01		230	ns
					02, 06		200	
					10		190	
					03,07,08		150	
					04		130	
					05, 09		80	
$\overline{TxC}$ ↑ to TxD delay (X1 mode) 13/ 14/	$t_{dTXCr(TXD)}$		9, 10, 11	12	01		230	ns
					02, 06		200	
					10		190	
					03,07,08		150	
					04		130	
					05, 09		80	
TxD to $\overline{TRxC}$ delay (send clock echo)	$t_{dTXD(TRX)}$		9, 10, 11	13	01,02,06, 07, 10		200	ns
					03, 08		140	
					04		120	
					05, 09		80	
$\overline{RTxC}$ high width 15/	t_{wRTxh}		9, 10, 11	14	01	180		ns
					02,06,07	150		
					10	130		
					03, 08	120		
					04	100		
					05, 09	80		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V ±10% unless otherwise specified	Group A subgroups	Ref no.	Device type	Limits		Unit
						Min	Max	
$\overline{\text{RTxC}}$ low width 15/	t_{wRTxl}	See figure 3, general timings. C_L = 50 pF ±10% V_{CC} = 4.5 V	9, 10, 11	15	01	180		ns
					02,06,07	150		
					10	130		
					03, 08	120		
					04	100		
					05, 09	80		
$\overline{\text{RTxC}}$ cycle time (RxD, TxD) 15/ 16/	t_{cRTX}		9, 10, 11	16	01	640		ns
					02, 06	500		
					10	472		
					03,07,08	400		
					04	320		
					05, 09	244		
Crystal oscillator period 4/ 17/	t_{cRTXX}		9, 10, 11	17	01	165	1000	ns
					02,06,10	125	1000	
					03,07,08	100	1000	
					04	80	1000	
					05, 09	62	1000	
$\overline{\text{TRxC}}$ high width 15/	t_{wTRXh}		9, 10, 11	18	01	180		ns
					02,06,07	150		
					10	130		
					03, 08	120		
					04	100		
					05, 09	80		
$\overline{\text{TRxC}}$ low width 15/	t_{wTRXl}		9, 10, 11	19	01	180		ns
					02,06,07	150		
					10	130		
					03, 08	120		
					04	100		
					05, 09	80		
$\overline{\text{TRxC}}$ cycle time 15/ 16/	t_{cTRX}		9, 10, 11	20	01	640		ns
					02, 06	500		
					10	472		
					03,07,08	400		
					04	320		
					05, 09	244		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V ±10% unless otherwise specified	Group A subgroups	Ref no.	Device type	Limits		Unit
						Min	Max	
$\overline{DCD}$ to $\overline{CTS}$ pulse width	t_{wEXT}	See figure 3, general timings. C_L = 50 pF ±10% V_{CC} = 4.5 V	9, 10, 11	21	01,02,06, 07, 10	200		ns
					03, 08	120		
					04	100		
					05, 09	70		
$\overline{SYNC}$ pulse width	t_{wSY}		9, 10, 11	22	01,02,06, 07,10	200		ns
					03, 08	120		
					04	100		
					05, 09	70		
$\overline{RxC}$ ↑ to W/$\overline{REQ}$ valid delay 2/ 11/ 18/	$t_{dRXC(REQ)}$	See figure 3, system timings. C_L = 50 pF ±10% V_{CC} = 4.5 V	9, 10, 11	1	08,09,10	13	17	t_{cPC}
					01,02,03, 04,05,06, 07	8	12	
$\overline{RxC}$ ↑ to wait inactive delay 2/ 7/ 11/ 18/	$t_{dRXC(W)}$		9, 10, 11	2	08,09,10	13	17	t_{cPC}
					01,02,03, 04,05,06, 07	8	14	
$\overline{RxC}$ ↑ to $\overline{SYNC}$ valid delay	$t_{dRXC(SY)}$		9, 10, 11	3	08,09,10	9	12	t_{cPC}
					01,02,03, 04,05,06, 07	4	7	
$\overline{RxC}$ ↑ to $\overline{INT}$ valid delay 2/ 7/ 11/ 18/	$t_{dRXC(INT)}$		9, 10, 11	4	08,09,10	15	21	t_{cPC}
					01,02,03, 04,05,06, 07	10	16	
$\overline{TxC}$ ↑ to W/$\overline{REQ}$ valid delay 2/ 14/ 18/	$t_{dTXC(REQ)}$		9, 10, 11	5	08,09,10	8	11	t_{cPC}
					01,02,03, 04,05,06, 07	5	8	
$\overline{TxC}$ ↓ to wait inactive delay 2/ 7/ 14/ 18/	$t_{dTXC(W)}$		9, 10, 11	6	08,09,10	8	14	t_{cPC}
					01,02,03, 04,05,06, 07	5	11	
$\overline{TxC}$ ↓ to $\overline{DTR/REQ}$ valid delay 2/ 14/ 18/	$t_{dTXC(DRQ)}$		9, 10, 11	7	08,09,10	7	10	t_{cPC}
					01,02,03, 04,05,06, 07	4	7	
$\overline{TxC}$ ↓ to $\overline{DTR/REQ}$ valid delay 2/ 8/ 14/ 18/	$t_{dTXC(EDRQ)}$		9, 10, 11	7a	08,09,10	9	12	t_{cPC}
					03,04,05, 06	5	8	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{CC} = 5.0\ V \pm 10\%$ unless otherwise specified	Group A subgroups	Ref no.	Device type	Limits		Unit
						Min	Max	
$\overline{TxC} \downarrow$ to $\overline{INT}$ valid delay 2/ 7/ 14/ 18/	$t_{dTXC(INT)}$	See figure 3, system timings. $C_L = 50\ pF \pm 10\%$ $V_{CC} = 4.5\ V$	9, 10, 11	8	08,09,10	9	13	t_{cPC}
					01,02,03, 04,05,06, 07	6	10	
$\overline{SYNC}$ transition to INT valid delay 2/ 7/ 18/	$t_{dSY(INT)}$		9, 10, 11	9	All	2	6	t_{cPC}
$\overline{DCD}$ or $\overline{CTS}$ transition to INT valid delay 2/ 7/ 18/	$t_{dEXT(INT)}$		9, 10, 11	10	10	3	8	t_{cPC}
					01,02,03, 04,05,06, 07,08,09	2	6	

1/ All tests must be performed under the worst case conditions.

2/ Guaranteed to the limit specified herein if not tested.

3/ For device types 03, 04, 05, and 06, clock rise and fall times are controlled at approximately 5 ns by the tester.

4/ Tested in interrupt acknowledge cycle only.

5/ Parameter does not apply to interrupt acknowledge transactions.

6/ Float delay is defined as the time required for a ±0.5 V change in the output with a maximum dc load and minimum ac load.

7/ Open-drain output, measured with open-drain test load.

8/ Applies to versions with SDLC enhancements only.

9/ Parameter is system dependent. For any SCC in the daisy chain, $t_{dIAi(RD)}$ must be greater than the sum of $t_{dPC(IEO)}$ for the highest priority device in the daisy chain, $t_{sIEI(RDA)}$ for the SCC, and $t_{dIEIf(IEO)}$ for each device seperating them in the daisy chain.

10/ Parameter applies only between transactions involving the SCC.

11/ $\overline{RxC}$ is $\overline{RTxC}$ or $\overline{TRxC}$, whichever is supplying the receive clock.

12/ Parameter applies only if the data rate is one-fourth the PCLK rate. In all other cases, no phase relationship between $\overline{RxC}$ and PCLK or $\overline{TxC}$ and PCLK is required.

13/ Parameter applies only to FM encoding/decoding.

14/ $\overline{TxC}$ is $\overline{TRxC}$ or $\overline{RTxC}$, whichever is supplying the transmit clock.

15/ Parameter applies only for transmitter and receiver; DPLL and baud rate generator timing requirements are identical to chip PCLK requirements.

16/ The maximum receive or transmit data is one-fourth PCLK.

17/ Both $\overline{RTxC}$ and $\overline{SYNC}$ have 30 pF capacitors to ground connected to them.

18/ The value of this parameter is dependent on PCLK cycle time.

Device type	All		
Case outline	Q		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	D_1	21	$\overline{DCDB}$
2	D_3	22	$\overline{CTSB}$
3	D_5	23	$\overline{RTSB}$
4	$\overline{D_7}$	24	DTR/REQB
5	$\overline{INT}$	25	$\overline{TxDB}$
6	IEO	26	TRxCB
7	$\overline{IEI}$	27	$\overline{RxDB}$
8	INTACK	28	$\overline{RTxCB}$
9	V_{CC}	29	$\overline{SYNCB}$
10	W/REQA	30	W/REQB
11	$\overline{SYNC}$A	31	G$\overline{ND}$
12	RTxCA	32	$\overline{D/C}$
13	$\overline{RxDA}$	33	C$\overline{E}$
14	TRxCA	34	$\overline{A/B}$
15	$\overline{TxDA}$	35	$\overline{WR}$
16	D$\overline{TR}$/R$\overline{E}$QA	36	RD
17	$\overline{RTSA}$	37	D_6
18	$\overline{CTSA}$	38	D_4
19	DCDA	39	D_2
20	PCLK	40	D_0

Device type	All		
Case outlines	Y and X 1/		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	D_0	23	$\overline{PCLK}$
2	D_1	24	$\overline{DCDB}$
3	D_3	25	$\overline{CTSB}$
4	D_5	26	$\overline{RTSB}$
5	$\overline{D_7}$	27	DTR/REQB
6	INT	28	NC
7	IEO	29	$\overline{TxDB}$
8	$\overline{IEI}$	30	TRxCB
9	INTACK	31	$\overline{RxDB}$
10	V_{CC}	32	$\overline{RTxCB}$
11	W/REQA	33	$\overline{SYNCB}$
12	$\overline{SYNC}$A	34	W/REQB
13	RTxCA	35	GND
14	$\overline{RxDA}$	36	$\overline{NC}$
15	TRxCA	37	$\overline{D/C}$
16	TxDA	38	$\overline{CE}$
17	NC	39	$\overline{A/B}$
18	$\overline{NC}$	40	$\overline{WR}$
19	DTR/REQA	41	RD
20	$\overline{RTSA}$	42	D_6
21	$\overline{CTSA}$	43	D_4
22	DCDA	44	D_2

1/ Case X is applicable to device type 07 only.
NC = No connection.

FIGURE 1. Terminal connections.

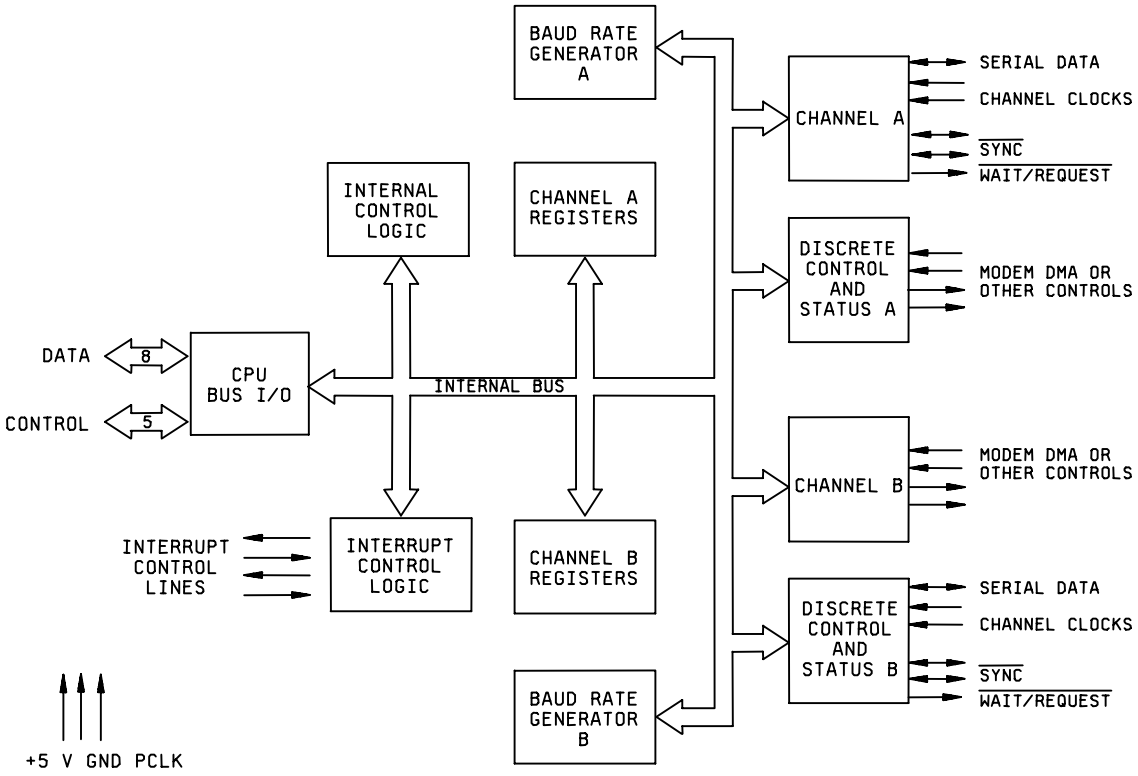


FIGURE 2. Block diagram.

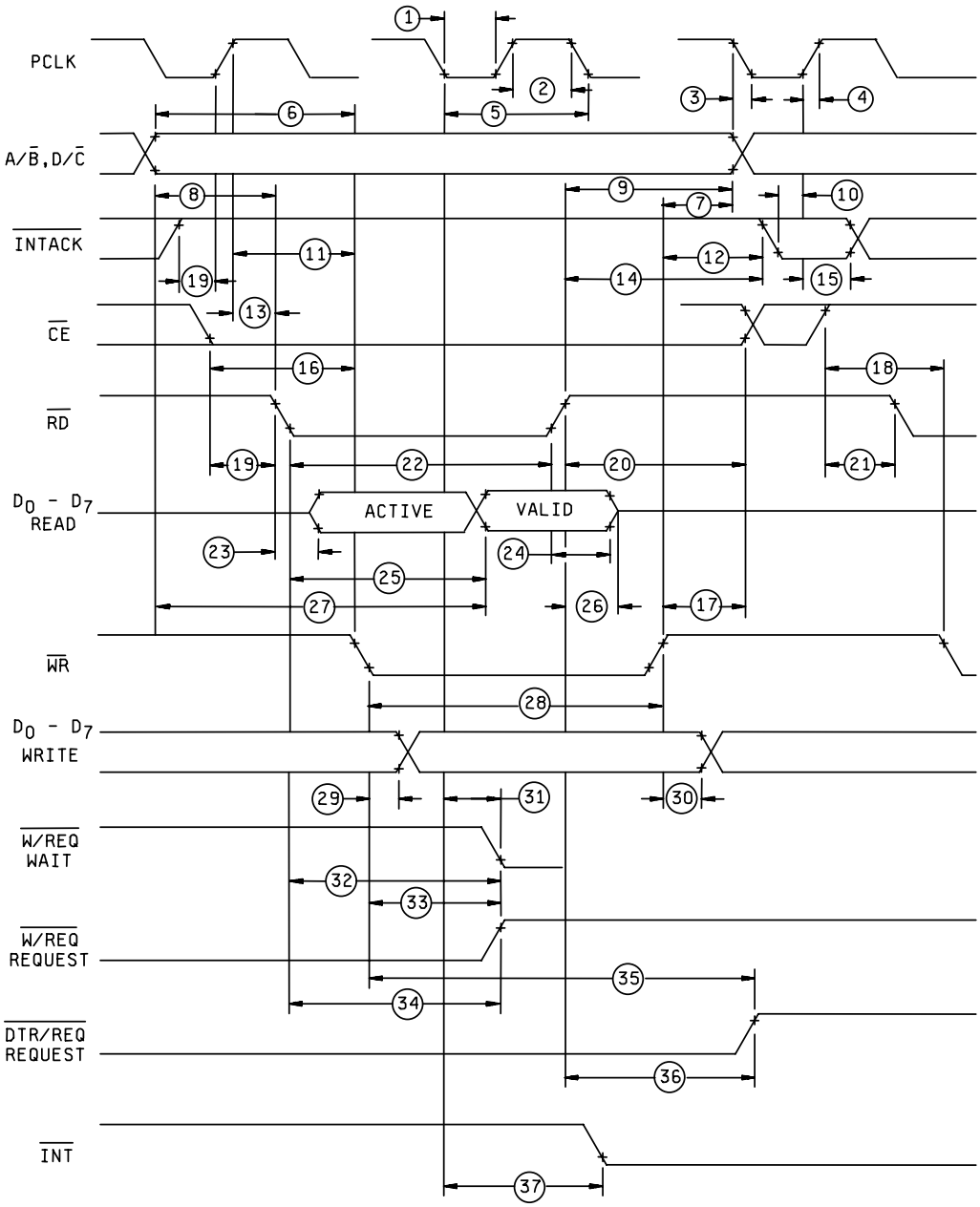
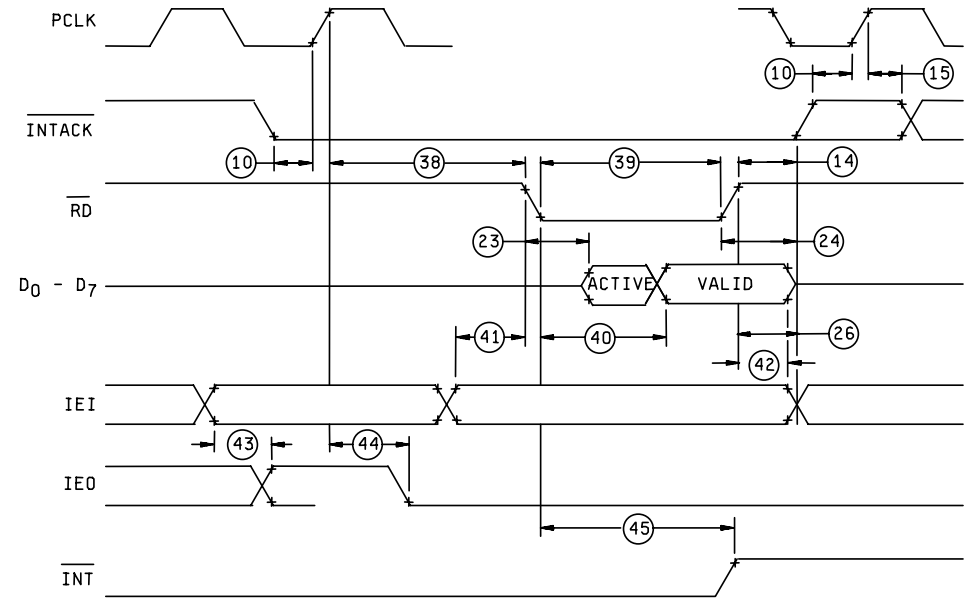
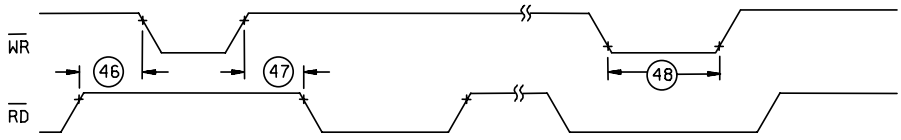


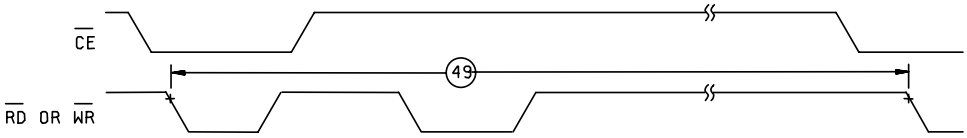
FIGURE 3. Timing waveforms and test circuits.



INTERRUPT ACKNOWLEDGE TIMING

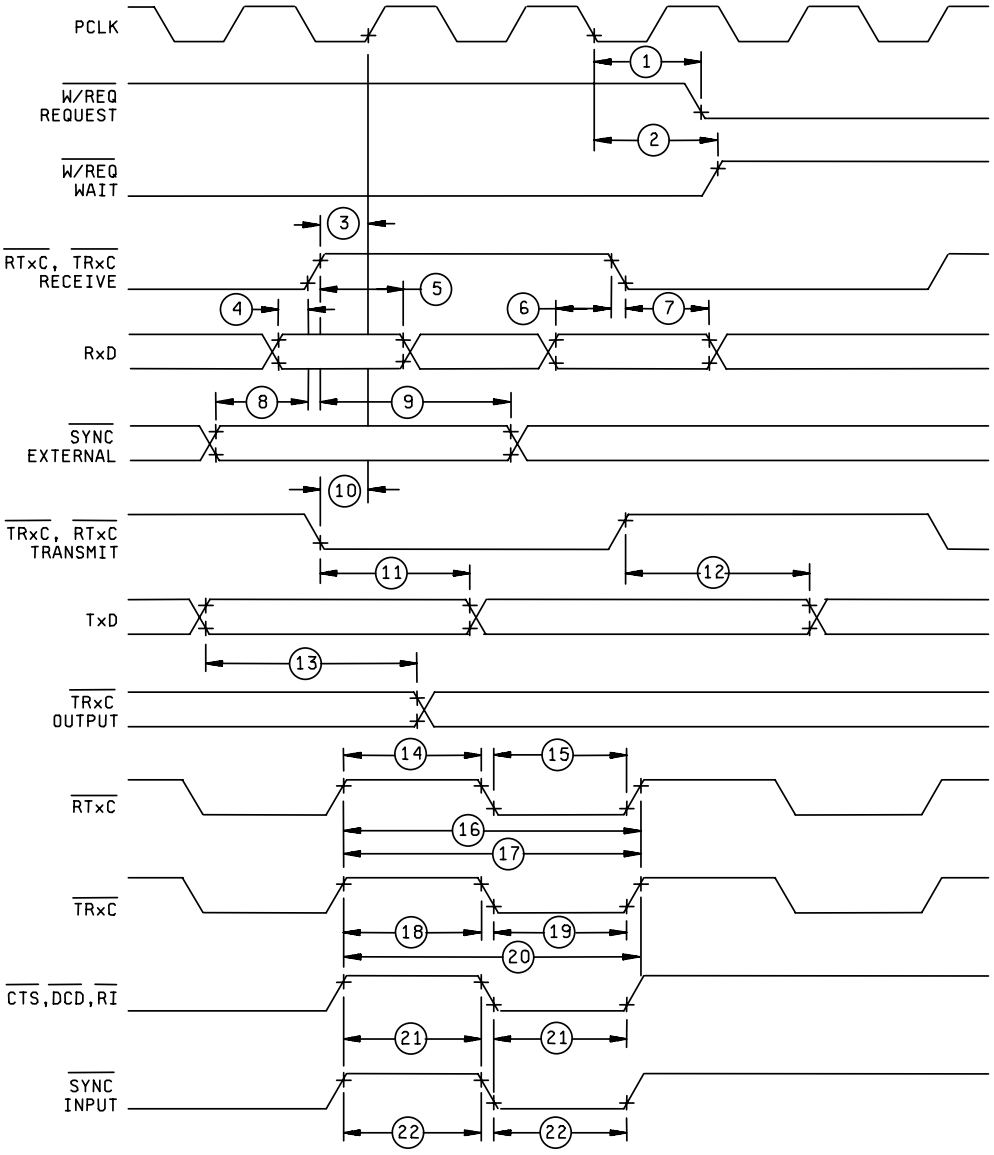


RESET TIMING



CYCLE TIMING

FIGURE 3. Timing waveforms and test circuits – Continued.



GENERAL TIMING

FIGURE 3. Timing waveforms and test circuits – Continued.

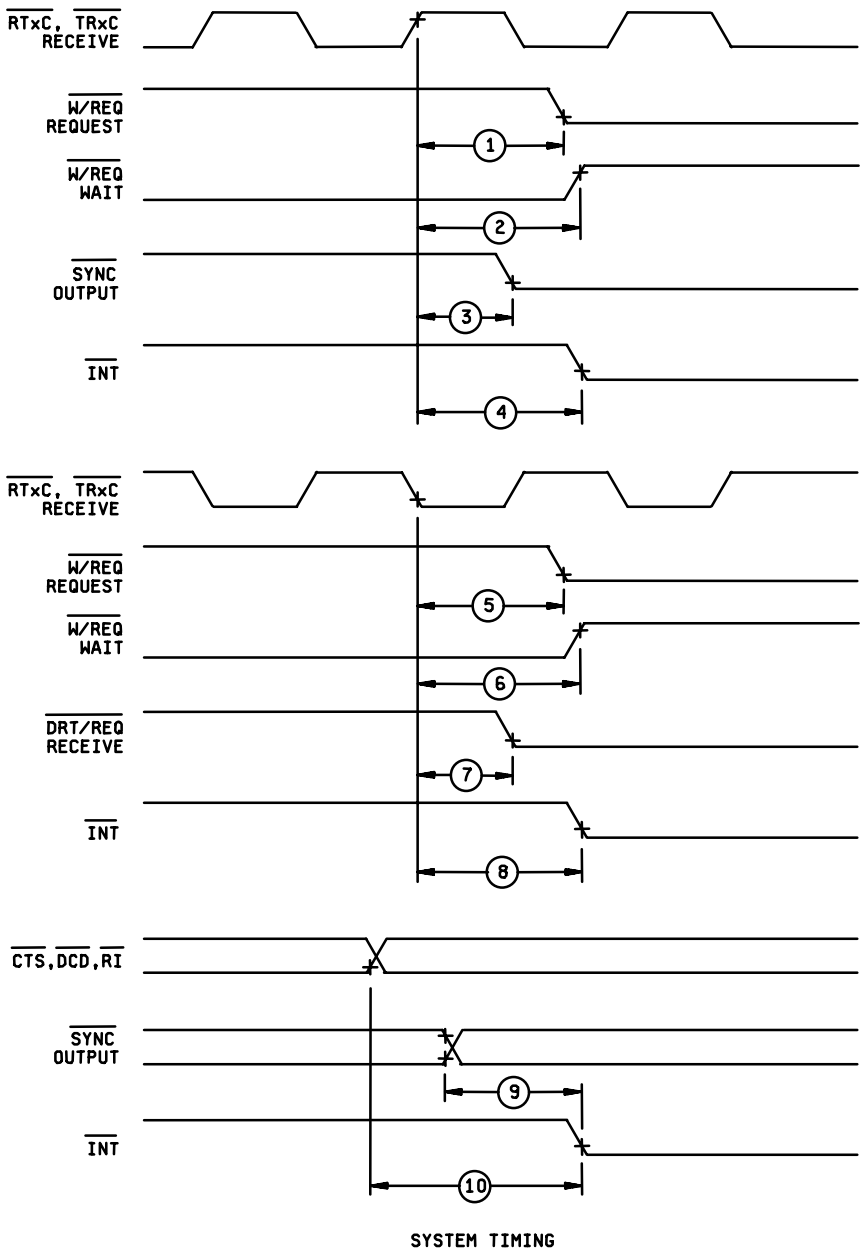
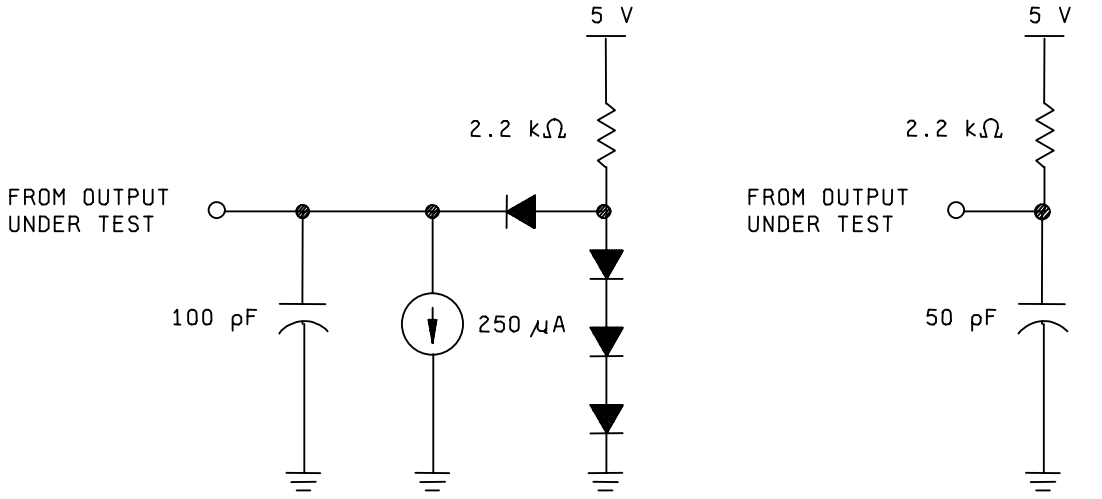
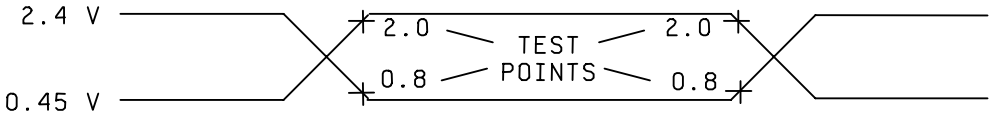


FIGURE 3. Timing waveforms and test circuits – Continued.

Device types 01, 02, 07, 08, 09, 10

Switching test circuits





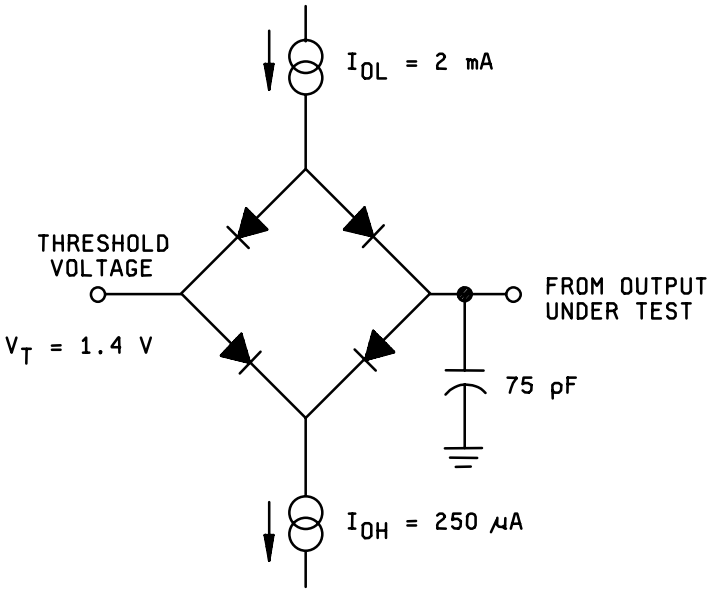
SWITCHING TEST INPUT/OUTPUT WAVEFORM

AC testing: Inputs are driven at 2.4 V for a logic “1” and 0.45 for a logic “0”. Timing measurements are made at 2.0 V for a logic “1” and 0.8 V for a logic “0”.

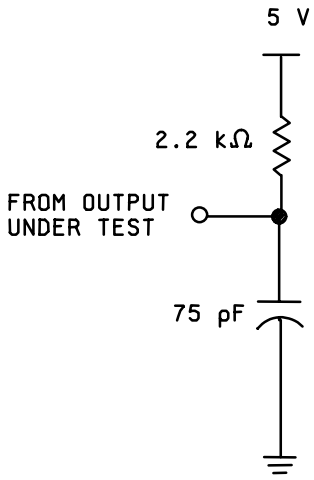
FIGURE 3. Timing waveforms and test circuits – Continued.

Device types 03, 04, 05, 06

Switching test circuits



STANDARD TEST LOAD



OPEN DRAIN TEST LOAD

SWITCHING TEST INPUT/OUTPUT WAVEFORM

AC testing: Inputs are driven at 2.4 V for a logic “1” and 0.45 for a logic “0”. Timing measurements are made at 2.0 V for a logic “1” and 0.8 V for a logic “0”.

FIGURE 3. Timing waveforms and test circuits – Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	----
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN}, C_{OUT}, and $C_{I/O}$ measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of five devices with zero rejects is required.

d. Subgroups 7 and 8 shall verify the functionality of the device.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.6 Pin descriptions.

$A/\overline{B}$	Channel A/channel B select (input). This signal selects the channel in which the read or write operation occurs.
$\overline{CE}$	Chip enable (input, active low). This signal selects the SCC for a read or write operation.
$\overline{CTSA}$, $\overline{CTSB}$	Clear to send (inputs, active low). If these pins are programmed as auto enables, a low on the inputs enables the respective transmitters. If not programmed as auto enables, they may be used as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow rise time inputs. The SCC detects pulses on these inputs and can interrupt the CPU on both logic level transitions.

6.6 Pin descriptions – Continued.

$D/\overline{C}$	Data/control select (input). This signal defines the type of information transferred to or from the SCC. A high means data is transferred, a low indicates a command.
$\overline{DCDA}$, $\overline{DCDB}$	Data carrier detect (inputs, active low). These pins function as receiver enables if they are programmed for auto enables; otherwise they may be used as general-purpose input pins. Both pins are Schmitt-trigger buffered to accommodate slow rise time signals. The SCC detects pulses on these pins and can interrupt the CPU on both logic level transitions.
D_0-D_7	Data bus (bidirectional, three-state). These lines carry data and commands to and from the SCC.
$\overline{DTR/REQA}$, $\overline{DTR/REQB}$	Data terminal ready/request (outputs, active low). These outputs follow the state programmed into the DTR bit. They can also be used as general purpose outputs or as request lines for a DMA controller.
IEI	Interrupt enable in (input, active high). IEI is used with IEO to form an interrupt daisy chain when there is more than one interrupt driven device. A high IEI indicates that no other higher priority device has an interrupt under service or is requesting an interrupt.
IEO	Interrupt enable out (output, active high). IEO is high only if IEI is high and the CPU is not servicing an SCC interrupt or the SCC is not requesting an interrupt (interrupt acknowledge cycle only). IEO is connected to the next lower priority device's IEI input and thus inhibits interrupts from lower priority devices.
$\overline{INT}$	Interrupt request (output, open-drain, active low). This signal is activated when the SCC requests an interrupt.
$\overline{INTACK}$	Interrupt acknowledge (input, active low). This signal indicates an active interrupt acknowledge cycle. During this cycle, the SCC interrupt daisy chain settles. When $\overline{RD}$ becomes active, the SCC places an interrupt vector on the data bus (if IEI is high). $\overline{INTACK}$ is latched by the rising edge of PCLK.
PCLK	Clock (input). This is the master SCC clock used to synchronize internal signals. PCLK is a TTL level signal. PCLK is not required to have any phase relationship with the master system clock.
$\overline{RD}$	Read (input, active low). This signal indicates a read operation and when the SCC is selected, enables the SCC's bus drivers. During the interrupt acknowledge cycle, this signal gates the interrupt vector onto the bus if the SCC is the highest priority device requesting an interrupt.
RxDA, RxDB	Receive data (inputs, active high). These input signals receive serial data at standard TTL levels.
$\overline{RTxCA}$, $\overline{RTxCB}$	Receive/transmit clocks (inputs, active low). These pins can be programmed in several different modes of operation. In each channel, RTxC may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock for the digital phase-locked loop. These pins can also be programmed for use with the respective $\overline{SYNC}$ pins as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous modes.

6.6 Pin descriptions – Continued.

$\overline{\text{RTSA}}$, $\overline{\text{RTSB}}$	Request to send (outputs, active low). When the request to send (RTS) bit in write register 5 is set, the $\overline{\text{RTS}}$ signal goes low. When the RTS bit is reset in the asynchronous mode and auto enable is on, the signal goes high after the transmitter is empty. In synchronous mode or in asynchronous mode with auto enable off, the $\overline{\text{RTS}}$ pin strictly follows the state of the RTS bit. Both pins can be used as general purpose outputs.
$\overline{\text{SYNCA}}$, $\overline{\text{SYNCB}}$	Synchronization (inputs or outputs, active low). These pins can act either as inputs, outputs, or part of the crystal oscillator circuit. In the asynchronous receive mode (crystal oscillator option not selected), these pins are inputs similar to $\overline{\text{CTS}}$ and $\overline{\text{DCD}}$. In this mode, transitions on these lines affect the state of the synchronous/hunt status bits in read register 0 but have no other function. In external synchronization mode with the crystal oscillator not selected, these lines also act as inputs. In this mode, $\overline{\text{SYNC}}$ must be driven low two receive clock cycles after the last bit in the synchronous character is received. Character assembly begins on the rising edge of the receive clock immediately preceding the activation of $\overline{\text{SYNC}}$. In the internal synchronization mode (monosync and bisync) with the crystal oscillator not selected, these pins act as outputs and are active only during the part of the receive clock cycle in which synchronous characters are recognized. The synchronous condition is not latched, so these outputs are active each time a synchronization pattern is recognized (regardless of character boundaries). In SDLC mode, these pins act as outputs and are valid on receipt of a flag.
TxDA, TxDB	Transmit data (outputs, active high). These output signals transmit serial data at standard TTL levels.
$\overline{\text{TRxCA}}$, $\overline{\text{TRxCB}}$	Transmit/receive clocks (inputs or outputs, active low). These pins can be programmed in several different modes of operation. $\overline{\text{TRxC}}$ may supply the receive clock or the transmit clock in the input mode or supply the output of the digital phase-locked loop, the crystal oscillator, the baud rate generator, or the transmit clock in the output mode.
$\overline{\text{WR}}$	Write (input, active low). When the SCC is selected, this signal indicates a write operation. The coincidence of $\overline{\text{RD}}$ and $\overline{\text{WR}}$ is interpreted as a reset.
W/$\overline{\text{REQA}}$, W/$\overline{\text{REQB}}$	Wait/request (outputs, open-drain when programmed for a wait function, driven high or low when programmed for a request function). These dual-purpose outputs may be programmed as request lines for a DMA controller or as wait lines to synchronize the CPU to the SCC data rate. The reset state is wait.

6.7 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 02-12-18

Approved sources of supply for SMD 5962-88689 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8868901QA 5962-8868901YA	0C7V7 0C7V7	Z85C3006CMB Z85C3006LMB
5962-8868902QA 5962-8868902YA	0C7V7 0C7V7	Z85C3008CMB Z85C3008LMB
5962-8868903QX 5962-8868903YX	3/ 3/	AM85C30-10/BQA AM85C30-10/BUA
5962-8868904QX 5962-8868904YX	3/ 3/	AM85C30-12/BQA AM85C30-12/BUA
5962-8868905QX 5962-8868905YX	3/ 3/	AM85C30-16/BQA AM85C30-16/BUA
5962-8868906QX 5962-8868906YX	3/ 3/	AM85C30-8/BQA AM85C30-8/BUA
5962-8868907QA 5962-8868907XA 5962-8868907YA	0C7V7 0C7V7 0C7V7	Z85C3010CMB Z85C3010NMB Z85C3010LMB
5962-8868908QA 5962-8868908YA	0C7V7 0C7V7	Z8523010CMB Z8523010LMB
5962-8868909QA 5962-8868909YA	0C7V7 0C7V7	Z8523016CMB Z8523016LMB
5962-88689010QA 5962-88689010YA	0C7V7 0C7V7	Z8523008CMB Z8523008LMB

See footnotes on next page.

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
0C7V7	Qualified Parts Laboratory, Inc. 3605 Kifer Road Santa Clara, CA 95051