

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Table I, correct symbols for supply under-voltage threshold and minimum supply to enable power OK output. Change maximum test limit to minimum for I _O and correct test condition for CMRR. Update format.	89-10-31	M. A.FRYE
B	Add case outline 2. Editorial changes throughout.	90-07-23	M. A. FRYE
C	Changes in accordance with N.O.R 5962-R265-94.	94-08-31	M. A. FRYE
D	Drawing updated to reflect current requirements. -ro	01-05-22	R. MONNIN
E	Update drawing as part of 5 year review. -rrp	07-07-31	ROBERT M. HEBER

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

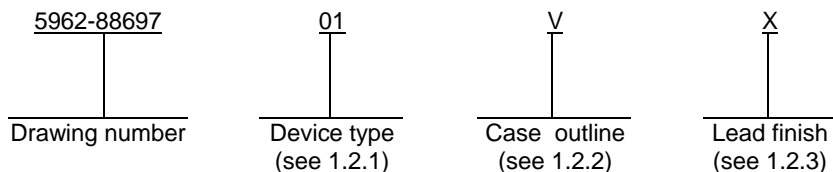
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REV STATUS	REV	E	E	E	E	E	E	E	E	E	E	E	E							
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10									

PMIC N/A	PREPARED BY JOSEPH A. KERBY	<p align="center">DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990 http://www.dscc.dla.mil</p>							
<p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY D. R. COOL								
	APPROVED BY MICHAEL A. FRYE	<p align="center">MICROCIRCUIT, LINEAR, QUAD SUPPLY AND LINE MONITOR, MONOLITHIC SILICON</p>							
	DRAWING APPROVAL DATE 88-10-20								
	REVISION LEVEL E	SIZE A	CAGE CODE 67268	5962-88697					
		SHEET	1 OF 10						

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	UC1903	Quad supply and line monitor

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
V	GDIP1-T18 or CDIP2-T18	18	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/

- Supply voltage (+V_{IN}) +40 V dc
- Open-collector output voltage +40 V dc
- Open-collector output current +50 mA
- SENSE 1- 4 input voltage -0.3 V dc to +20 V dc
- LINE / SWITCHER SENSE input voltage -0.3 V dc to +40 V dc
- Op-amp and inverter input voltages -0.3 V dc to +40 V dc
- Op-amp and inverter output currents -40 mA
- WINDOW ADJUST voltage 0.0 V dc to +10 V dc
- Delay pin voltages 0.0 V dc to +5.0 V dc
- Reference output current -40 mA
- Power dissipation (P_D) :
- At T_A = +25°C 1.0 W 2/
- At T_C = +25°C 3.0 W 3/
- Storage temperature range -65°C to +150°C
- Lead temperature (soldering, 10 seconds) +300°C
- Junction temperature (T_J) +150°C
- Thermal resistance, junction-to-case (θ_{JC}) See MIL-STD-1835

1/ All voltages referenced to ground. Currents are positive into, and negative out of the specified terminals.

2/ For case V, derate at +10mW/°C above T_A = +25°C. For case 2, derate at 9 mW/°C above T_A = +40°C.

3/ For case V, derate at +36mW/°C above T_C = +25°C. For case 2, derate at 50 mW/°C above T_C = +90°C.

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1.4 Recommended operating conditions.

Ambient operating temperature range (T_A) -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

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3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) $T_A = +125^\circ\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
SUPPLY section							
Input supply current	+I _{IN1}	No faults	1,2,3	01		9.0	mA
	+I _{IN2}	Under-voltage, over-voltage and line faults				15	
Supply under-voltage threshold	V _{SUV}	Fault outputs enabled	1,2,3	01	6.0	7.5	V
Minimum supply to enable power OK output	V _{MIN}		1,2,3	01		4.0	V
REFERENCE section							
Output voltage	V _{REF}		1	01	2.485	2.515	V
			2,3		2.465	2.535	
Load regulation	V _{RLD}	0 mA ≤ I _L ≤ -10 mA	1,2,3	01		±10	mV
Line regulation	V _{RLN}	8.0 V ≤ +V _{IN} ≤ 40 V	1,2,3	01		±4.0	mV
FAULT THRESHOLDS section							
Over-voltage threshold adjust	V _{ADJ} (OV)	Input = low to high, 2/ 0.5 V ≤ WINDOW ADJUST ≤ 2.5 V	1,2,3	01	0.230	0.270	V/V
Under-voltage threshold adjust	V _{ADJ} (UV)	Input = high to low, 2/ 0.5 V ≤ WINDOW ADJUST ≤ 2.5 V	1,2,3	01	-0.270	-0.230	V/V
Over-voltage and under-voltage threshold hysteresis	V _{TH} (HYS)	0.5 V ≤ WINDOW ADJUST ≤ 2.5 V	1,2,3	01	10	30	mV/V
Over-voltage and under-voltage threshold supply sensitivity	ΔV _{TH}	8.0 V ≤ +V _{IN} ≤ 40 V	1,2,3	01		±0.01	%V
	Δ+V _{IN}						
Adjust pin input bias current	I _{IB1}	0.5 V ≤ WINDOW ADJUST ≤ 2.5 V	1,2,3	01		±10	μA/V
Line sense threshold	V _{LST}	Input = high to low	1,2,3	01	1.94	2.06	V
Line sense threshold hysteresis	V _{LST} (HYS)		1,2,3	01	125	225	mV

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
SENSE INPUTS 1 through 4 section							
Sense 1 – 4 input bias current	I _{IB2}	Input = 2.8 V <u>3/</u>	1,2,3	01		3.0	μA
		Input = 2.2 V <u>3/</u>				-3.0	
Line sense input bias current	I _{IB3}	Input = 2.3 V <u>3/</u>	1,2,3	01		3.0	μA
OVER-VOLTAGE AND UNDER-VOLTAGE FAULT DELAY							
Delay time	t _D	<u>4/</u>	4,5,6	01	20	50	ms/μF
FAULT OUTPUTS (<u>OV</u> , <u>UV</u> , and POWER OK) section							
Maximum current	I _{MAX}	V _{OUT} = 2.0 V	1,2,3	01	30		mA
Saturation voltage	V _{SAT}	I _{OUT} = 12 mA	1,2,3	01		0.4	V
Leakage current	I _L	V _{OUT} = 40 V	1,2,3	01		25	μA
SENSE 4 INVERTER section							
Input offset voltage	V _{IO1}		1,2,3	01		±8.0	mV
Input bias current	I _{IB4}		1,2,3	01		-2.0	μA
Open loop gain	A _{OL1}		4,5,6	01	65		dB
Power supply rejection ratio	PSRR1	8.0 V ≤ +V _{IN} ≤ 40 V	4,5,6	01	65		dB
Inverting input saturation current tolerance	I _{SAT1} (TOL)	V _{NONINVERT} = GND, <u>5/</u> V _{OUT} ≥ 5.0 V	1,2,3	01		-1.4	mA
GENERAL PURPOSE OPERATIONAL AMPLIFIER section							
Input offset voltage	V _{IO2}		1,2,3	01		±5.0	mV
Input bias current	I _{IB5}		1,2,3	01		-2.0	μA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions ^{1/} -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
GENERAL PURPOSE OPERATIONAL AMPLIFIER section – continued							
Input offset current	I _{IO}		1,2,3	01		-0.5	μA
Open loop gain	A _{OL2}		4,5,6	01	65		dB
Common-mode rejection ratio	CMRR	0 V ≤ V _{CM} ≤ +V _{IN} - 2.0 V	4,5,6	01	65		dB
Power supply rejection ratio	PSRR2	8.0 V ≤ +V _{IN} ≤ 40 V	4,5,6	01	65		dB
Inverting input saturation current tolerance	I _{SAT2} (TOL)	V _{NONINVERT} = GND, ^{5/} V _{OUT} ≥ 5.0 V	1,2,3	01		-1.4	mA

^{1/} Unless otherwise specified, +V_{IN} = 15 V, sense inputs 1, 2, 3, and 4 = 2.5 V, and WINDOW ADJUST = 1.0 V.

^{2/} Offset from V_{REF} as a function of WINDOW ADJUST.

^{3/} These conditions inherently result in maximum input bias currents, which therefore represent the maximum currents required as the sense inputs cross appropriate threshold.

^{4/} Ratio of threshold voltage to charging current.

^{5/} When the non inverting input is driven to less than -0.3 V (as may be the case when sensing a negative supply voltage), the PNP input transistor will saturate and the substrate diode will become forward biased. The input current must be limited to a magnitude of 1.4 mA or less. If not, the resultant parasitic transistor action may cause the output to invert. This parameter is 100 percent tested by ramping the current on the inverting input while verifying that the output voltage remains high.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 7, 8, 9, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
 - (2) T_A = +125°C, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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Device type	01	
Case outlines	V	2
Terminal number	Terminal symbol	
1	+V _{IN}	+V _{IN}
2	V _{REF} (2.5 V)	V _{REF} (2.5 V)
3	GROUND	GROUND
4	WINDOW ADJUST	GROUND SENSE
5	SENSE 4 INVERTING INPUT	WINDOW ADJUST
6	SENSE 4	NC
7	SENSE 3	SENSE 4 INVERTING INPUT
8	SENSE 2	SENSE 4
9	SENSE 1	SENSE 3
10	0 V DELAY	SENSE 2
11	$\overline{0\text{ V FAULT}}$	SENSE 1
12	$\overline{U\text{ V FAULT}}$	0 V DELAY
13	U V DELAY	$\overline{0\text{ V FAULT}}$
14	POWER OK	$\overline{U\text{ V FAULT}}$
15	LINE / SWITCHER SENSE	U V DELAY
16	OPERATIONAL AMPLIFIER OUTPUT	POWER OK
17	OPERATIONAL AMPLIFIER NONINVERTING INPUT	LINE / SWITCHER SENSE
18	OPERATIONAL AMPLIFIER INVERTING INPUT	OPERATIONAL AMPLIFIER OUTPUT
19	---	OPERATIONAL AMPLIFIER NONINVERTING INPUT
20	---	OPERATIONAL AMPLIFIER INVERTING INPUT

NC = No connection

FIGURE 1. Terminal connections.

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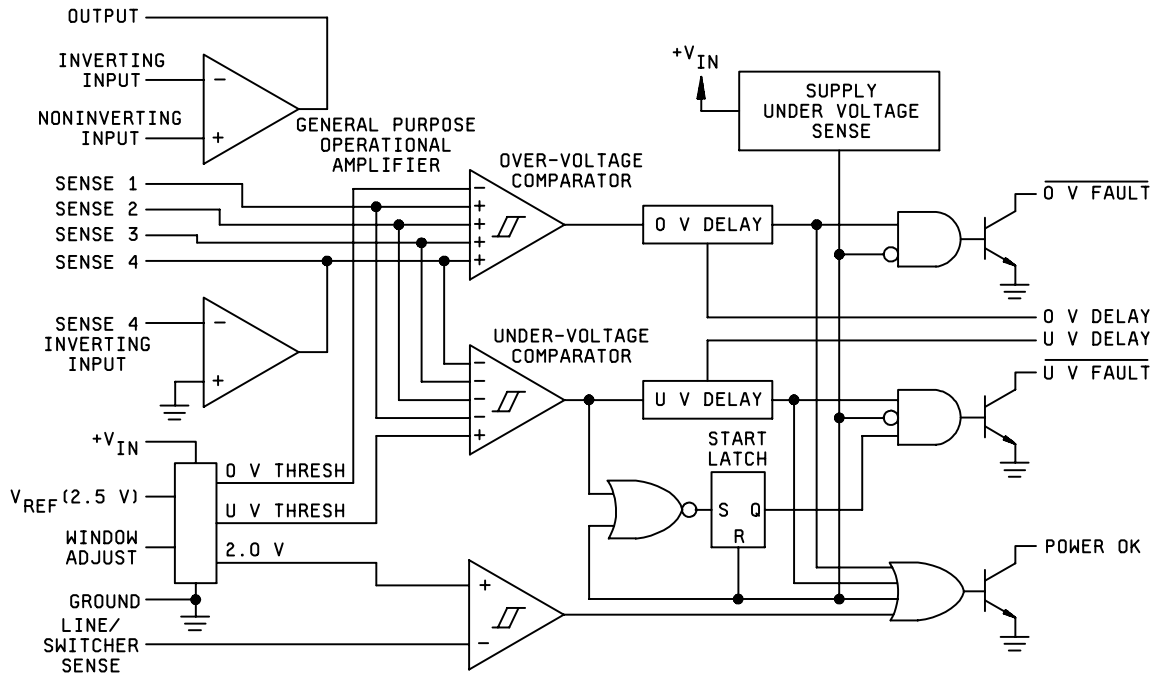


FIGURE 2. Block diagram.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 4, 5, 6
Group A test requirements (method 5005)	1, 2, 3, 4, 5, 6
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 07-07-31

Approved sources of supply for SMD 5962-88697 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at <http://www.dscclia.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-8869701VA	01295	UC1903J/883B
5962-88697012A	01295	UC1903L/883B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

01295

Vendor name
and address

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Lane
P.O. Box 660199
Dallas, TX 75243
Point of contact: U.S. Highway 75 South
P.O. Box 84, M/S 853
Sherman, TX 75090-9493

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