REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Added two device types with access times of 25 ns and 20 ns for vendor CAGE 1FN41. Added low power version. Added F-16 package. Editorial changes throughout.	92-04-21	M. A. Frye
B	Source for 01, 02, and 06 devices no longer available. Added devices 08-12. Added 28 J leaded chip carrier package. Updated boilerplate, editorial changes throughout.	94-10-21	M. A. Frye
C	Updated to new boilerplate format. Added new footnote to ICC1 in table I, renumbered the rest of footnotes. Added additional conditions to ICC1 conditions block. Changed the max limit for devices 11 and 12 for ICC2 from 5 mA to 15 mA.	00-02-22	Raymond Monnin
D	Made changes to table I for device type 08; t_{SS}, f_{MAXS}, and t_{SFS}. Updated boilerplate, editorial changes throughout. ksr	02-09-06	Raymond Monnin
E	Boilerplate update, part of 5 year review. ksr	07-06-22	Robert M. Heber

REV																				
SHEET																				
REV	E	E	E	E	E	E	E	E												
SHEET	15	16	17	18	19	20	21	22												

REV STATUS	REV	E	E	E	E	E	E	E	E	E	E	E	E	E	E
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Kenneth Rice

CHECKED BY
Ray Monnin

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
88 – 09 - 16

REVISION LEVEL
E

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, ULTRAVIOLET ERASABLE, PROGRAMMABLE LOGIC ARRAY, MONOLITHIC SILICON

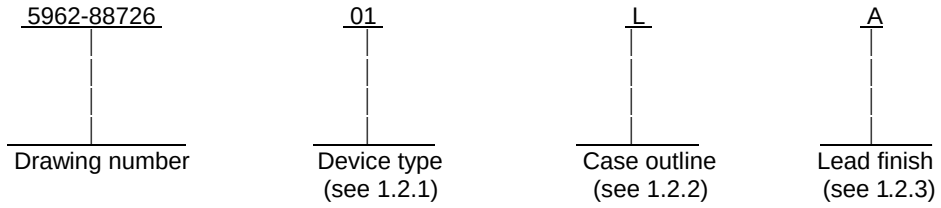
SIZE	CAGE CODE	
A	**67268**	**5962-88726**

SHEET 1 OF 22

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Address access time
01	V750	22-input 10-output and-or-logic array	40 ns
02	V750	22-input 10-output and-or-logic array	35 ns
03	V750	22-input 10-output and-or-logic array	25 ns
04	V750	22-input 10-output and-or-logic array	20 ns
06	V750L	22-input 10-output and-or-logic array	35 ns
07	V750L	22-input 10-output and-or-logic array	25 ns
08	V750B	22-input 10-output and-or-logic array	10 ns
09	V750B	22-input 10-output and-or-logic array	15 ns
10	V750B	22-input 10-output and-or-logic array	25 ns
11	V750BL	22-input 10-output and-or-logic array	15 ns
12	V750BL	22-input 10-output and-or-logic array	25 ns

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
L	GDIP3-T24	24	dual-in-line package 1/
3	CQCC1-N28	28	square chip carrier 1/
X	GDFP1-F24	24	flat pack package 1/
Y	CQCC1-J28	28	J leaded chip carrier 1/

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1/ Lid shall be transparent to permit ultraviolet light erasure.

1.3 Absolute maximum ratings. 2/

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-2.0 V dc to +7.0 V dc 3/
Output voltage applied	-0.5 V dc to +7.0 V dc 3/
Output sink current	16 mA
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Maximum power dissipation (P_D) 4/	1.2 W
Maximum junction temperature	+175°C
Lead temperature (soldering, 10 seconds maximum)	+300°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc to 5.5 V dc
High level input voltage (V_{IH})	2.0 V dc minimum
Low level input voltage (V_{IL})	0.8 V dc maximum

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

2/ All voltages referenced to V_{SS}.

3/ Minimum voltage is -0.6 V dc which may undershoot to -2.0 V dc for pulses of less than 20 ns.
Maximum output pin voltage is V_{CC} +0.75 V dc which may overshoot to +7.0 V dc for pulses of less than 20 ns.

4/ Must withstand the added P_D due to short circuit test, e.g., I_{OS}.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 2.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in group A, B, or C inspections (see 4.3), the device shall be programmed by the manufacturer prior to test with a minimum of 50 percent of the total number of gates programmed or to any altered item drawing pattern which includes at least 25 percent of the total number of gates programmed.

3.2.3.2 Programmed devices. The requirements for supplying programmed devices are not part of this drawing.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Processing EPLDS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.6.1 Erasure of EPLDS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.

3.6.2 Programmability of EPLDS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5 and table III.

3.6.3 Verification of erasure of programmability of EPLDS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.9 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.10 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics

Test	Symbol	Conditions 1/ 4.5 V ≤ V_{CC} ≤ 5.5 V -55°C ≤ T_C ≤ +125°C Unless otherwise specified	Group A Subgroups	Device types	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	I_O = - 4.0 mA	1,2,3	All	2.4		V
Low level output voltage	V_{OL}	I_O = 8.0 mA	1,2,3	01-04, 06, 07		0.5	V
		I_O = 12 mA		08-12			
High impedance 2/ output leakage current	I_{OZ}	V_{CC} = 5.5 V, V_O = 5.5 V, V_O = GND	1,2,3	All	-10	10	uA
High level input current	I_{IH}	V_{IH} = 5.5 V	1,2,3	All		10	uA
		V_{IH} = 2.4 V	1,2,3	All		10	
Low level input current	I_{IL}	V_{IH} = 0.4 V	1,2,3	All		-10	uA
		V_{IH} = GND	1,2,3	All		-10	
Operating supply current	I_{CC1}	V_{CC} = 5.5 V, f = 1MHz, Outputs open, V_{IN} = V_{CC} or GND 3/	1,2,3	01-04, 06, 07		140	mA
				08-12		190	
Standby supply current	I_{CC2}	V_{CC} = 5.5 V, V_{IN} = GND, outputs open	1,2,3	01-04		140	mA
				08-10		190	
				06, 07		15	
				11,12		15	
Output short 4/ circuit current	I_{OS}	V_{CC} = 5.5 V	1,2,3	All	-30	120	mA
Input capacitance	C_I 5/ 6/	V_I = 0 V, V_{CC} = 5.0 V, T_A = 25°C, f = 1 Mhz (see 4.3.1c)	4	All		8	pF
Output capacitance	C_O 5/ 6/	V_O = 0 V, V_{CC} = 5.0 V, T_A = 25°C, f = 1 Mhz (see 4.3.1c)	4	All		8	pF
Functional tests		see note 4 of table II	7, 8A, 8B				

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $4.5\ V \le V_{CC} \le 5.5\ V$ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device	Limits		Unit
					Min	Max	
Input or feedback to nonregistered output	t_{PD}	V_{CC} = 4.5 V, C_L = 50 pF, see figures 4 and 5	9, 10, 11	01		40	ns
				02		35	
				06		30	
				03, 07, 10, 12		25	
				04		20	
				08		10	
				09, 11		15	
Clock to output	t_{CO}	V_{CC} = 4.5 V , C_L = 50 pF, see figures 4 and 5	9, 10, 11	01		35	ns
				02,06		30	
				03,07 10,12		22	
				04		20	
				09,11		14	
				08		10	
Input to output enable	t_{EA}	V_{CC} = 4.5 V , C_L = 5 pF, see figures 4 and 5	9, 10, 11	01		40	ns
				02,06		35	
				03,07, 10,12		25	
				04		20	
				09,11		15	
				08		10	
Input to output disable	t_{ER}		9, 10, 11	01		40	ns
				02,06		35	
				03,07, 10,12		25	
				04		20	
				09,11		15	
				08		10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $4.5\ V \le V_{CC} \le 5.5\ V$ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Clock period	t_P	V_{CC} = 4.5 V , C_L = 5 pF, see figures 4 and 5	9, 10, 11	01	35		ns
				02,06	30		
				03,07	22		
				04	18		
				10,12	17		
				09,11	14		
				08	11		
Clock pulse width 5/ 6/	t_{CL}	V_{CC} = 4.5 V , C_L = 50 pF, see figures 4 and 5	9, 10, 11	01	17		ns
				02,06	15		
				03,07	10		
				10,12	8.5		
				04	8		
				09,11	7		
				08	5.5		
Clock to feedback	t_{CF}		9, 10, 11	01	15		ns
				02,06	12		
				03, 04,07, 10,12	10		
				09,11	9		
				08	7.5		
Input setup time 5/ 6/	t_S	V_{CC} = 4.5 V , C_L = 50 pF, see figures 4 and 5	9, 10, 11	01	20		ns
				02,06	18		
				03,07, 10,12	12		
				04,11	10		
				09	8		
				08	4		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 4.5 V ≤ V_{CC} ≤ 5.5 V -55°C ≤ T_C ≤+125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Hold time 5/ 6/	t_H	V_{CC} = 4.5 V , C_L = 50 pF, see figures 4 and 5	9, 10, 11	01	15		ns
				02,06	10		
				03,07, 09,10	5		
				11,12	7		
				08	2		
Maximum clock frequency 5/ 6/	f_{MAX}		9, 10, 11	01	28		MHz
				02,06	33		
				11	41		
				03,07,09	45		
				04	55		
				10,12	29		
				08	71		
Asynchronous reset pulse width	t_{AW}		9, 10, 11	01	40		ns
				02,06	35		
				03,07, 10,12	20		
				04,09,11	15		
				08	10		
Asynchronous reset recovery time	t_{AR}		9, 10, 11	01	40		ns
				02,06	35		
				03,07, 10,12	20		
				04,09,11	15		
				08	10		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $4.5\ V \le V_{CC} \le 5.5\ V$ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Feedback setup time	t_{SF}	V_{CC} = 4.5 V , C_L = 50 pF, see figures 4 and 5	9, 10, 11	01,02	18		ns
				06	15		
				03,07 09,10, 11,12	7		
				04	5		
				08	4		
Asynchronous reset to registered output reset	t_{AP}		9, 10, 11	01		40	ns
				02,06		35	
				03,07, 10,12		25	
				04		20	
				09,11		15	
				08		12	
Clock period, input pin clock	t_{PS}		9, 10, 11	08	10		ns
				09,11	12		
				10,12	16		
Clock pulse width, input pin clock	f_{WS}		9, 10, 11	08	5		ns
				09,11	6		
				10,12	8		
Clock to feedback, input pin clock	t_{CFS}		9, 10, 11	08		5	ns
				09,11		5.5	
				10,12		7	
Input setup time, input pin clock	t_{SS}		9, 10, 11	08	6.5		ns
				09	8		
				10	9		
				11	10		
				12	12		

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $4.5\ V \le V_{CC} \le 5.5\ V$ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Hold time, input pin clock	t_{HS}	V_{CC} = 4.5 V , C_L = 50 pF, see figures 4 and 5	9, 10, 11	08-12	0		ns
Maximum clock frequency, input pin clock	f_{MAXS}		9, 10, 11	08		74	MHz
				09		58	
				10		41	
				11		52	
				12		37	
Asynchronous reset recovery time, input pin clock	t_{ARS}		9, 10, 11	08	10		ns
				09,11	15		
				10,12	25		
Clock to output, input pin clock	t_{COS}		9, 10, 11	08	0	7	ns
				09,11	0	9	
				10,12	0	15	
Setup time, synchronous preset product term clock	t_{SP}		9, 10, 11	04	12		ns
				01,02	18		
				08	7		
				09,11	8		
				03,06, 07,10,12	15		
Feedback setup time, input pin clock	t_{SFS}		9, 10, 11	08	6.5		ns
				09,11	7		
				10,12	9		
Setup time, synchronous preset, input pin clock	t_{SPS}		9, 10, 11	08	5		ns
				09,11	11		
				10,12	15		

1/ All voltages are referenced to ground.
2/ I/O terminal leakage is the worst case of I_{IX} or I_{OZ}.
3/ Icc for typical functional pattern 3mA/MHz for devices 06&07, 5mA/MHz for devices 10-12, worst case based on initial characterization.
4/ Only one output shorted at a time.
5/ Tested only initially and after any design changes.
6/ Test applies only to register outputs.

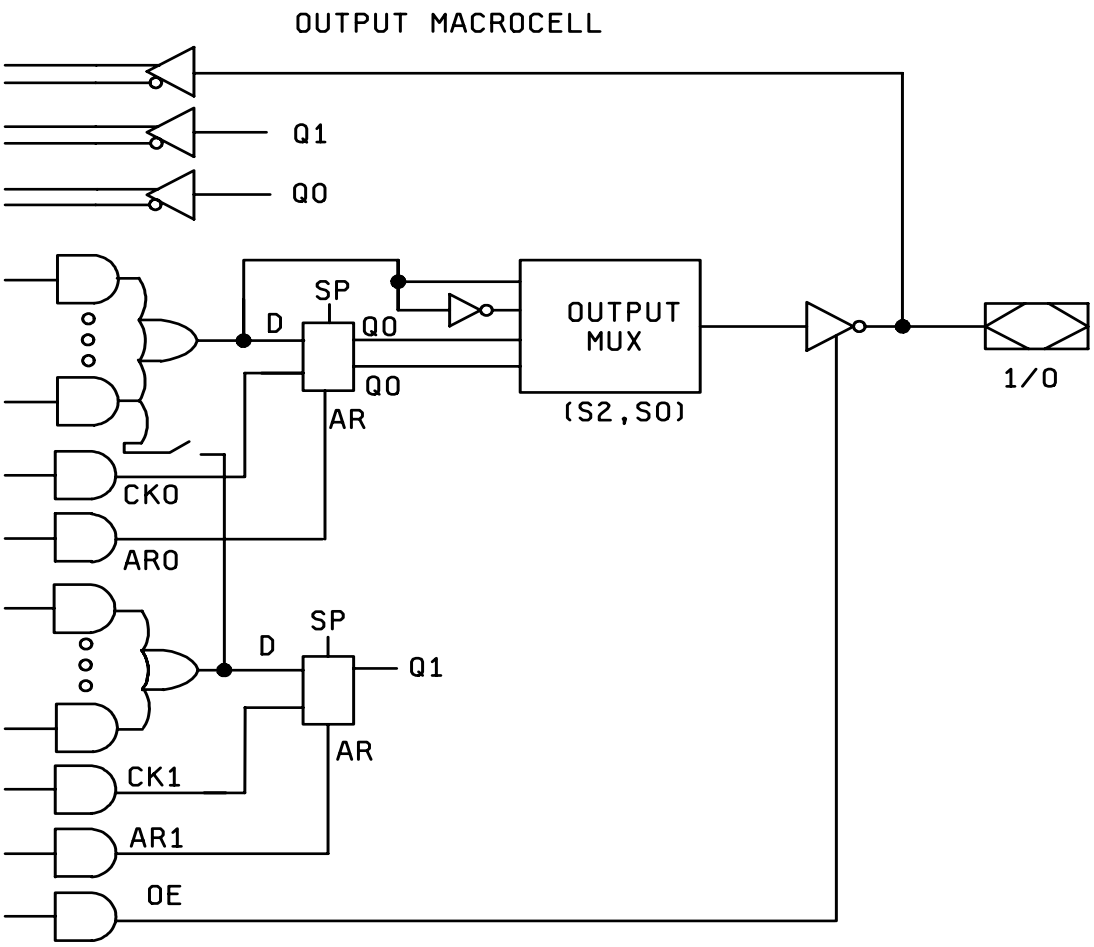
Device types	01-04, 06-12	
Case outlines	L, X	3, Y
Terminal number	Terminal symbol	
1	CK/I	NC
2	I	CK/I
3	I	I
4	I	I
5	I	I
6	I	I
7	I	I
8	I	NC
9	I	I
10	I	I
11	I	I
12	GND	I
13	I	I
14	I/O	GND
15	I/O	NC
16	I/O	I
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O
21	I/O	I/O
22	I/O	NC
23	I/O	I/O
24	V_{CC}	I/O
25	- - -	I/O
26	- - -	I/O
27	- - -	I/O
28	- - -	V_{CC}

FIGURE 1. Terminal connections.

Truth table																					
Input pins												Output pins									
I	I	I	I	I	I	I	I	I	I	I	I	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
X	X	X	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

NOTES:
1. Z = three-state.
2. X = don't care.

FIGURE 2. Truth table. (Unprogrammed)



S2	S1	S0	Output configuration
0	0	0	Active low, combined terms, registered
0	0	1	Active low, combined terms, combinatorial
0	1	0	Active low, separate terms, registered
0	1	1	Active low, separate terms, combinatorial
1	0	0	Active high, combined terms, registered
1	0	1	Active high, combined terms, combinatorial
1	1	0	Active high, separate terms, registered
1	1	1	Active high, separate terms, combinatorial

FIGURE 3. Logic diagram (unprogrammed) - for devices 01 - 04 and 06, 0 7.

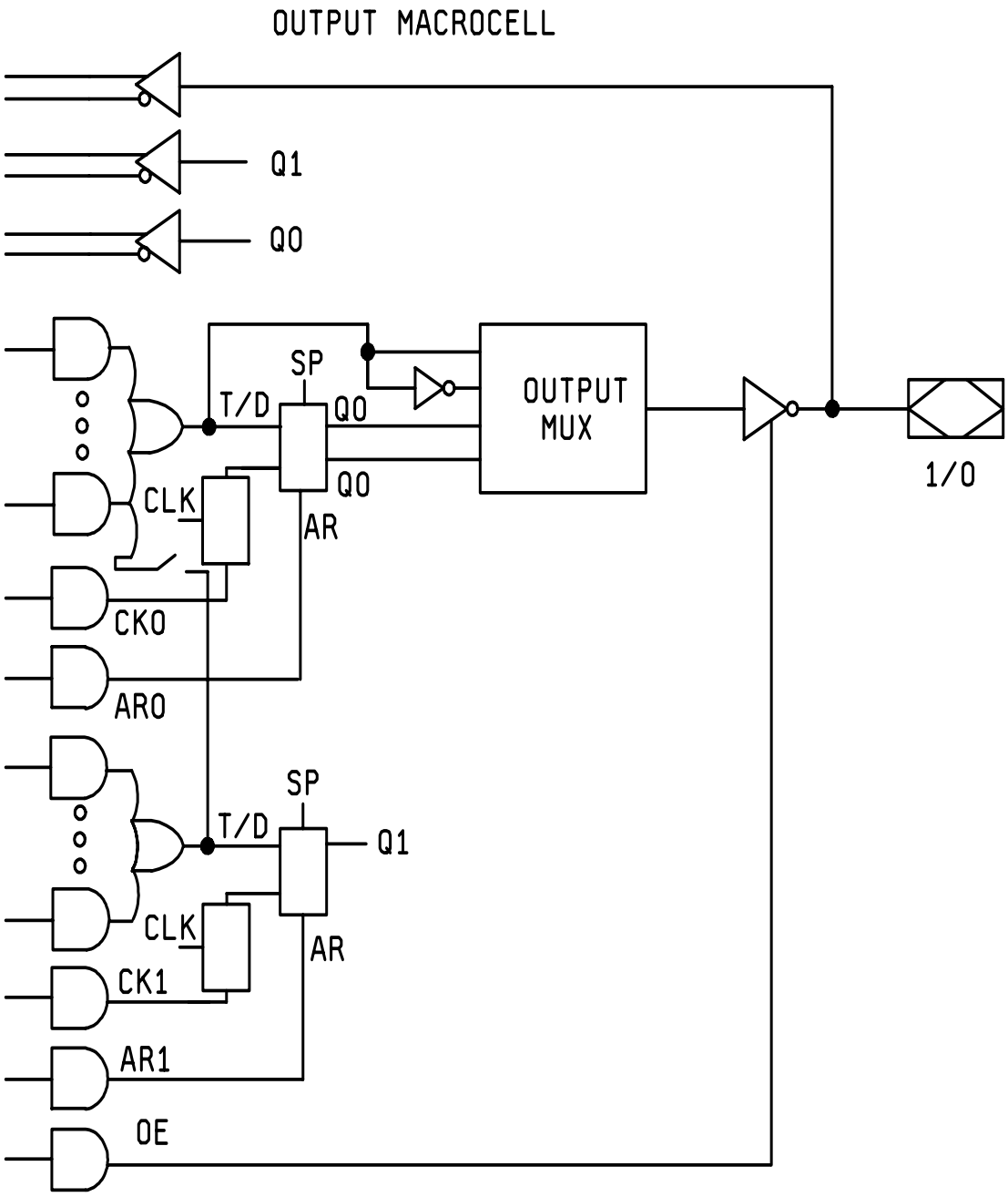
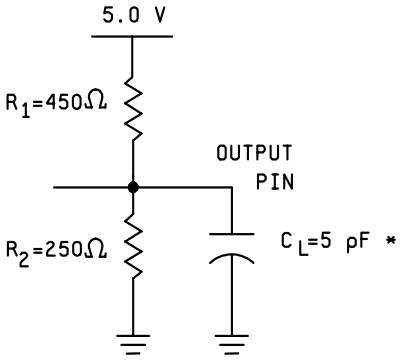


FIGURE 3. Logic diagram (unprogrammed) - for devices 08 - 12

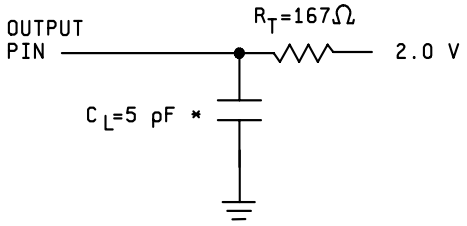
FOR DEVICES 01 – 07

OUTPUT TEST LOAD

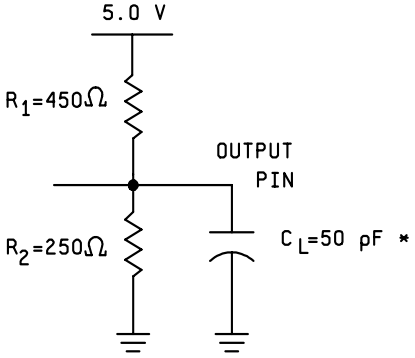


CIRCUIT A OR EQUIVALENT

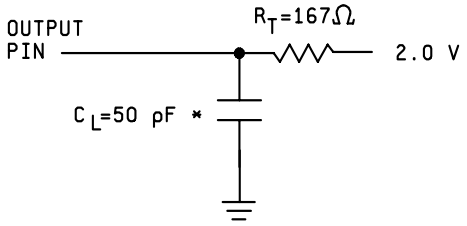
FOR DEVICES 08 – 12



OUTPUT TEST LOAD

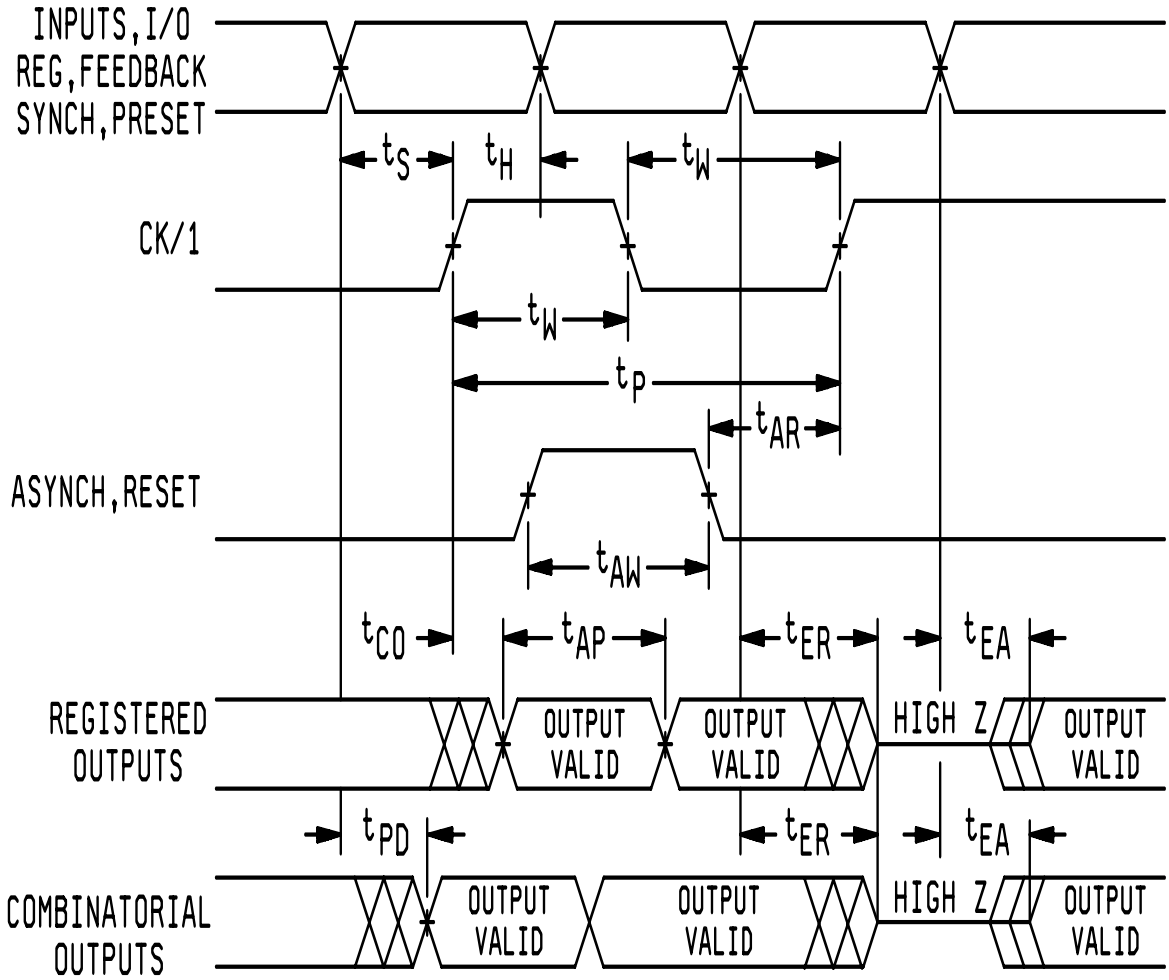


CIRCUIT B OR EQUIVALENT



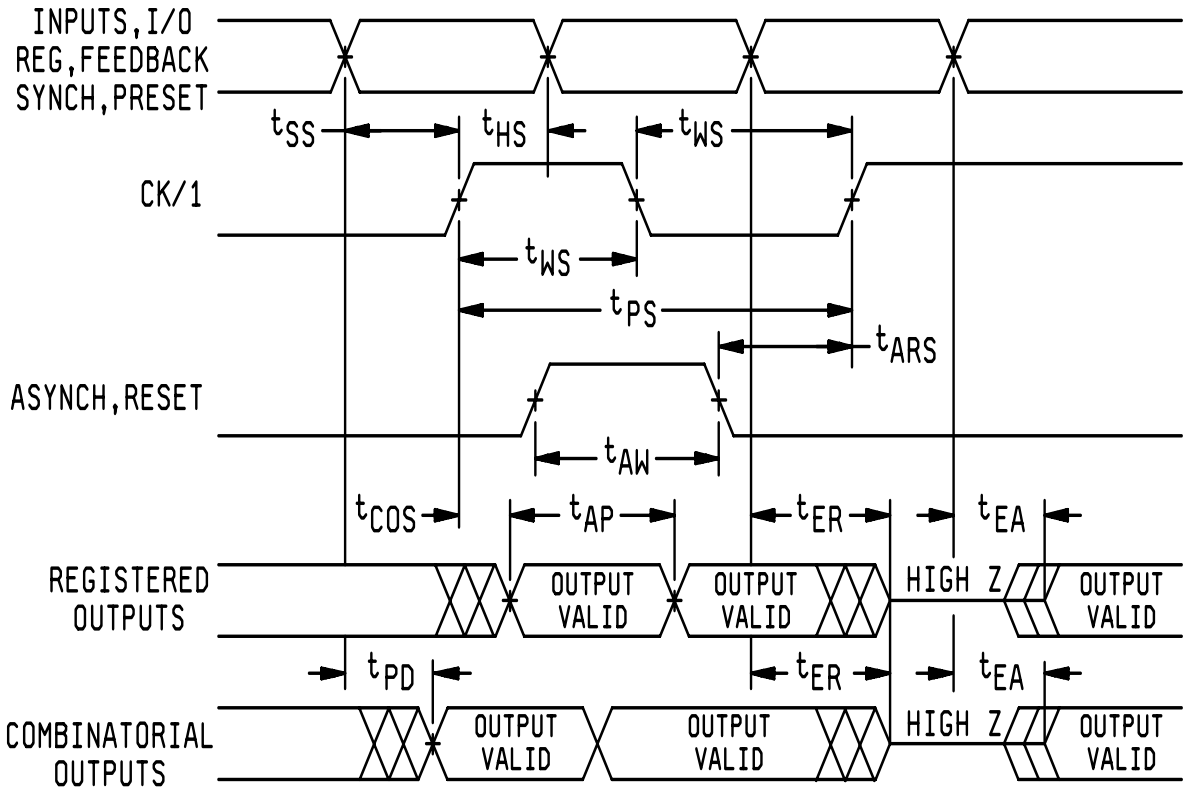
*Including jig and scope
(minimum value)

FIGURE 4. Output test circuit.



NOTE: Timing measurement reference is 1.5 V. Input ac driving levels are 0.0 V and 3.0 V, unless otherwise specified.

FIGURE 5. Switching waveforms. (All device types)



NOTE: Timing measurement reference is 1.5 V. Input ac driving levels are 0.0 V and 3.0 V, unless otherwise specified.

FIGURE 5. Switching waveforms Continued. (Device types 08 - 12)

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps:

Margin test method A.

(1) Program greater than 95 percent of the bit locations, including the slowest programming cell (see 3.5.2). The remaining cells shall provide a worst case speed pattern.

(2) Bake, unbiased, for 72 hours at +140°C to screen for data retention lifetime.

(3) Perform a margin test using V_m = +5.8 V at 25°C using loose timing (i.e., t_{ACC} = 1 μs).

(4) Perform dynamic burn-in (see 4.2a).

(5) Margin at V_m = +5.8 V.

(6) Perform electrical tests (see 4.2).

(7) Erase (see 3.5.1), except devices submitted for groups A, B, C, and D testing.

(8) Verify erasure (see 3.5.3).

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_I and C_O measurement) shall be measured only for the initial test and after process or design changes which may affect input or output capacitance.

TABLE II. Electrical test requirements. 1/ 2/ 3/ 4/

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004) (pre burn-in)	1
Final electrical test parameters (method 5004) for programmed devices	1*, 2, 3, 7*, 8A, 8B
Final electrical test parameters (method 5004) for unprogrammed devices	1*, 2, 3, 7*, 8A, 8B, 9
Group A test requirements (method 5005)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
Group C and D end-point electrical parameters (method 5005)	2, 3, 7, 8A, 8B

1/ * indicates PDA applies to subgroups 1 and 7.
2/ ** see 4.3.1c.
3/ Any or all subgroups may be combined when using high-speed testers.
4/ Subgroups 7 and 8 functional tests shall verify that no fuses are blown for unprogrammed devices or that the altered item drawing pattern exists for programmed devices.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4 Erasing procedures. The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 angstroms (Å). The integrated dose (i.e., ultraviolet intensity x exposure time) for erasure should be a minimum of fifteen (15) Ws/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 1200 $\mu W/cm^2$ power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 Ws/cm^2 (1 week at 12,000 $\mu W/cm^2$). Exposure of the device to high intensity ultraviolet light for long periods may cause permanent damage.

4.5 Programming procedures for method A. The programming characteristics in table III and the following procedures shall be used for programming the device.

a. Connect the device in the electrical configuration for programming the waveforms of figure 6 and programming characteristics of table III shall apply.

b. Initially and after each erasure all bits are in the "1" state. A programmed "0" can be changed to a "1" by ultraviolet light erasure (see 4.4).

c. Programming occurs when the V_{pp} is at 12.5 V and PGM pulse is at 12.5 V.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

TABLE III. Programming characteristics for method A.

Test	Symbol	Conditions 1/ T_A = +25°C ± 5°C, V_{CC} = 6.0 V ±0.25 V V_{PP} = 12.5 V ±0.5 V	Device types	Limits		Unit
				Min	Max	
Input current (all inputs)	I_{LI}	$V_{IN} = V_{IL}$ or V_{IH}	All		10	uA
Input low level (all inputs)	V_{IL}		All	-0.6	0.8	V
Input high level	V_{IH}		All	2.0	V_{CC}+ .75	V
Output low voltage during verify	V_{OL}	I_{OL} = 16 mA	All		0.5	V
Output high voltage during verify	V_{OH}	I_{OH} = -4.0 mA	All	2.4		V
V_{CC} supply current	I_{CC2}		01-04, 06,07		140	mA
			08-12		190	
V_{PP} supply current (program)	I_{PP2}	V_{pp} pin = V_{PP}	All		30	mA
Address setup time	t_{AS}		All	2		us
OE setup time	t_{OES}		All	2		us
Data setup time	t_{DS}		All	2		us
Address hold time	t_{AH}		All	0		us
Data hold time	t_{DH}		All	2		us
Output enable to output float delay	t_{DFP} 2/		All	0	130	ns
V_{CC} = setup time	t_{VCS}		All	2		us
PGM initial program pulse width	t_{PW} 3/		01-04, 06,07	0.95	1.05	ms
			08-12	.095	.105	
PGM overprogram pulse width	4/ t_{OPW}		01-04, 06,07	18	225	ms
			08-12	.475	65.63	
Data valid from OE	t_{DV}		All		70	ns

1/ V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2/ This parameter is only sampled and is not 100 percent tested. Output float is defined as the point where data is no longer driven, see timing diagram.
3/ Initial program pulse width tolerance is 1 ms ±5 percent.
4/ The length of the overprogram pulse may vary from 18 ms to 225 ms as a function of the iteration counter value X.

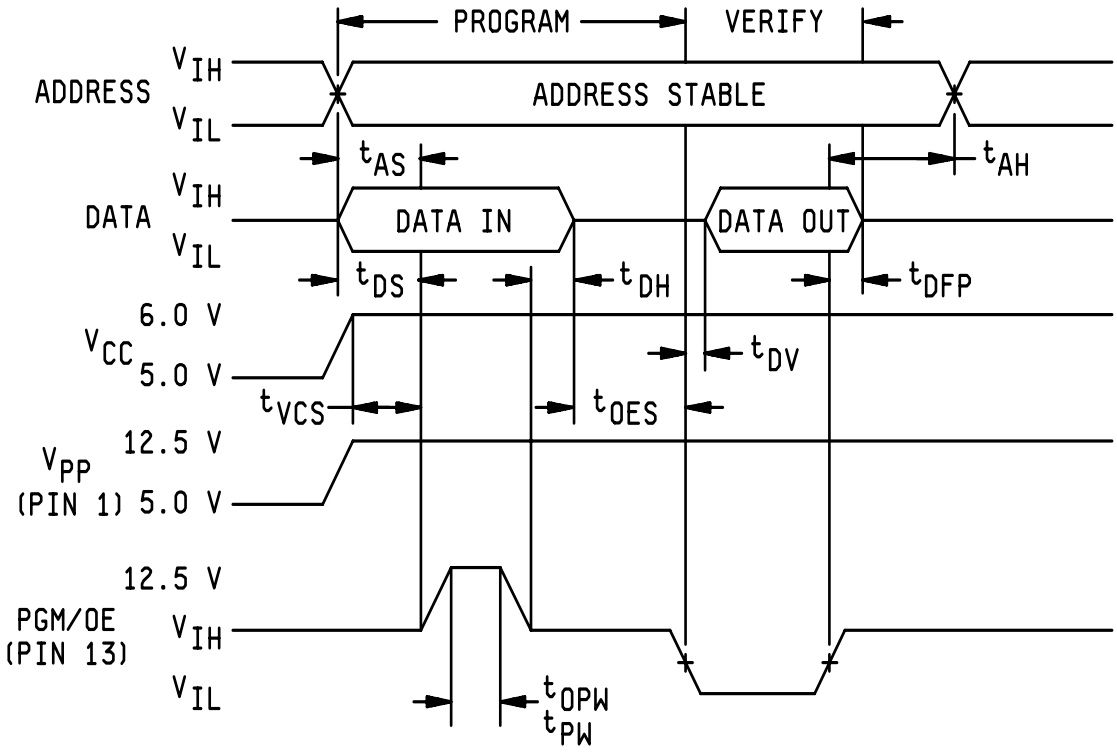


FIGURE 6. Programming waveforms.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 07-06-22

Approved sources of supply for SMD 5962-88726 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standardized military drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 3/
5962-8872601LA	2/	ATV750-40DM/883
5962-88726013A	2/	ATV750-40LM/883
5962-8872601XA	2/	ATV750-40YM/883
5962-8872602LA	2/	ATV750-35DM/883
5962-88726023A	2/	ATV750-35LM/883
5962-8872602XA	2/	ATV750-35YM/883
5962-8872602YA	2/	ATV750-35KM/883
5962-8872603LA	2/	ATV750-25DM/883
5962-88726033A	2/	ATV750-25LM/883
5962-8872603XA	2/	ATV750-25YM/883
5962-8872603YA	2/	ATV750-25KM/883
5962-8872604LA	2/	ATV750-20DM/883
5962-88726043A	2/	ATV750-20LM/883
5962-8872604XA	2/	ATV750-20YM/883
5962-8872604YA	2/	ATV750-20KM/883
5962-8872606LA	2/	ATV750L-25DM/883
5962-88726063A	2/	ATV750L-25LM/883
5962-8872606XA	2/	ATV750L-30YM/883

See footnotes at end of list.

Standardized military drawing PIN 1/	Vendor CAGE number	Vendor Similar PIN 3/
5962-8872607LA	2/	ATV750L-25DM/883
5962-88726073A	2/	ATV750L-25LM/883
5962-8872607XA	2/	ATV750L-25YM/883
5962-8872607YA	2/	ATV750L-25KM/883
5962-8872608LA	1FN41 4/	ATV750B-10DM/883
5962-88726083A	1FN41 4/	ATV750B-10LM/883
5962-8872608YA	2/	ATV750B-10KM/883
5962-8872609LA	1FN41 4/	ATV750B-15DM/883
5962-88726093A	1FN41 4/	ATV750B-15LM/883
5962-8872609YA	2/	ATV750B-15KM/883
5962-8872610LA	2/	ATV750B-25DM/883
5962-88726103A	2/	ATV750B-25LM/883
5962-8872610YA	2/	ATV750B-25KM/883
5962-8872611LA	1FN41 4/	ATV750BL-15DM/883
5962-88726113A	1FN41 4/	ATV750BL-15LM/883
5962-8872611YA	2/	ATV750BL-15KM/883
5962-8872612LA	2/	ATV750BL-25DM/883
5962-88726123A	2/	ATV750BL-25LM/883
5962-8872612YA	2/	ATV750BL-25KM/883

1/ The lead finish shown for each PIN representing hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Not available from an approved source.
3/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
4 The vendor has given an end of life date of 10 December 2007 for ordering and a 31 December 2008 as final ship date.

Vendor CAGE number	Vendor name and address	Margin test method	Programming method
1FN41	ATMEL Corporation 2325 Orchard Parkway San Jose, CA 95131-1034	A	A