REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Technical changes in table I. Editorial changes throughout.	90-11-07	W. K. Heckman
B	Corrections on figure 2. Corrections on table I prop delays. Editorial changes throughout.	92-02-05	Monica L. Poelking
C	Changes in accordance with NOR 5962-R316-92.	92-09-11	Monica L. Poelking
D	Update to current requirements. Editorial changes throughout. - gap	06-06-05	Raymond Monnin

The original first page of this drawing has been replaced.

REV																				
SHEET																				
REV																				
SHEET																				
REV STATUS				REV			D	D	D	D	D	D	D	D	D	D	D	D	D	
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	

PMIC N/A

PREPARED BY
Larry T. Gauder

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Tim H. Noh

APPROVED BY
William K. Heckman

DRAWING APPROVAL DATE
89-04-14

REVISION LEVEL
D

MICROCIRCUIT, DIGITAL, BIPOLAR, ADVANCED SCHOTTKY, 8-BIT UNIVERSAL REGISTER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-89573**

SHEET 1 OF 13

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-89573	01	R	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54F299	8-bit universal shift/storage registers with three-state outputs

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	dual-in-line
S	GDFP2-F20 or CDFP3-F20	20	flat
2	CQCC1-N20	20	square chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC})	-0.5 V dc minimum to +7.0 V dc maximum
Input voltage range	-1.2 V dc at -18 mA to +7.0 V dc
Input current range	-30 mA to +5.0 mA
Voltage applied to any output in the disabled or power-off state	-0.5 V dc to +5.5 V dc
Voltage applied to any output in the high state	-0.5 V dc to V_{CC}
Current into any output in the low state	+40 mA
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J)	+175°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Power dissipation (P_D) 1/	+523 mW

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc minimum to +5.5 V dc maximum
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ Power dissipation is defined as V_{CC} x I_{CC}, and must withstand the added P_D due to short-circuit output test; e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil;quicksearch/ or www.dodssp.daps.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Test circuit and switching waveforms. The test circuit and switching waveforms shall be specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified			Group A subgroups	Limits		Unit
						Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V, V_{IL} = 0.8 V, V_{IH} = 2.0 V	I_{OH} = -1.0 mA	$Q_{A'}$ or $Q_{H'}$	1, 2, 3	2.5		V
			I_{OH} = -1.0 mA	A/Q_A to H/Q_H		2.5		
			I_{OH} = -3.0 mA			2.4		
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, V_{IL} = 0.8 V, V_{IH} = 2.0 V, I_{OL} = 20 mA		$Q_{A'}$ or $Q_{H'}$	1, 2, 3		0.5	V
				A/Q_A to H/Q_H			0.5	
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_{IN} = -18 mA			1, 2, 3		-1.2	V
High level input current	I_{IH1}	V_{CC} = 5.5 V	V_{IN} = 5.5 V	A/Q_A to H/Q_H	1, 2, 3		1.0	mA
			V_{IN} = 7.0 V 1/	All other			1.0	
	I_{IH2}	V_{CC} = 5.5 V, V_{IN} = 2.7 V 2/		A/Q_A to H/Q_H	1, 2, 3		70	µA
				All other			20	
Low level input current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = 0.5 V 2/		A/Q_A to H/Q_H	1, 2, 3		-0.65	mA
				S0 or S1			-1.2	
				All other			-0.6	
Off-state output current	I_{OZH}	V_{CC} = 5.5 V, $\overline{G}1 = \overline{G}2$ = 5.5 V, V_{OUT} = 2.7 V, high level voltage applied			1, 2, 3		70	µA
	I_{OZL}	V_{CC} = 5.5 V, $\overline{G}1 = \overline{G}2$ = 5.5 V, V_{OUT} = 0.5 V, low level voltage applied					-0.65	mA
Short-circuit output current	I_{OS}	V_{OUT} = 0.0 V, V_{CC} = 5.5 V 3/			1, 2, 3	-60	-150	mA
Supply current	I_{CC}	V_{CC} = 5.5 V 4/			1, 2, 3		95	mA
Functional tests		See 4.3.1c, V_{CC} = 4.5 V, 5.5 V 5/			7, 8			
Maximum clock frequency	f_{MAX}	6/ 7/			9, 10, 11	70		MHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
Setup time, before CLK going high	t_{s1}	V_{CC} = 4.5 V and 5.5 V, C_L = 50 pF, R_L = 500Ω, See figure 4 5/	S0 or S1 high	9, 10, 11	9.5		ns
			S0 or S1 low		7.5		
	t_{s2}		A/Q_A to H/Q_H, SR or SL high or low		4.5		ns
	t_{s3}		$\overline{CLR}$ high, inactive-state		12.5		ns
Hold time, after CLK going high	t_{h1}		S0 or S1 high or low	9, 10, 11	0		ns
	t_{h2}		A/Q_A to H/Q_H, SR or SL high or low		2.0		ns
Pulse duration	t_{w1}		CLK high or low	9, 10, 11	7.0		ns
	t_{w2}		$\overline{CLR}$ low		7.0		ns
Propagation delay time, from CLK to $Q_{A'}$, $Q_{H'}$	t_{PLH1}	C_L = 50 pF, R_L = 500Ω, See figure 4 5/	V_{CC} = 5.0 V	9	3.5	7.0	ns
			V_{CC} = 4.5 V and 5.5 V	10, 11	3.5	9.0	
	t_{PHL1}		V_{CC} = 5.0 V	9	4.5	9.0	
			V_{CC} = 4.5 V and 5.5 V	10, 11	4.5	9.5	
Propagation delay time, from CLK to A/Q_A to H/Q_H	t_{PLH2}		V_{CC} = 5.0 V	9	4.0	9.0	ns
			V_{CC} = 4.5 V and 5.5 V	10, 11	4.0	11.0	
	t_{PHL2}		V_{CC} = 5.0 V	9	5.0	9.0	
			V_{CC} = 4.5 V and 5.5 V	10, 11	5.0	11.5	
Propagation delay time, from $\overline{CLR}$ to $Q_{A'}$ or $Q_{H'}$	t_{PHL3}		V_{CC} = 5.0 V	9	5.5	9.5	ns
			V_{CC} = 4.5 V and 5.5 V	10, 11	5.5	11.5	
Propagation delay time, from $\overline{CLR}$ to A/Q_A to H/Q_H	t_{PHL4}		V_{CC} = 5.0 V	9	5.5	10.0	
			V_{CC} = 4.5 V and 5.5 V	10, 11	5.5	11.5	
Output enable time, from $\overline{G}1$, $\overline{G}2$ to A/Q_A to H/Q_H	t_{PZH}		V_{CC} = 5.0 V	9	3.5	8.0	ns
			V_{CC} = 4.5 V and 5.5 V	10, 11	2.7	10.5	
	t_{PZL}		V_{CC} = 5.0 V	9	4.0	10.0	
			V_{CC} = 4.5 V and 5.5 V	10, 11	4.0	12.0	
Output disable time, from $\overline{G}1$, $\overline{G}2$ to A/Q_A to H/Q_H	t_{PHZ}		V_{CC} = 5.0 V	9	2.5	7.0	ns
			V_{CC} = 4.5 V and 5.5 V	10, 11	1.7	9.0	
	t_{PLZ}		V_{CC} = 5.0 V	9	1.5	5.5	
			V_{CC} = 4.5 V and 5.5 V	10, 11	1.5	7.5	

See footnotes on next page.

TABLE I. Electrical performance characteristics - Continued.

1/ For device types with npn output transistor configuration, V_{CC} = 0.0 V.

2/ For I/O ports (A/Q_A to H/Q_H), the parameters I_{IH2} and I_{IL} include the off-state output current.

3/ Not more than one output will be shorted at one time and the duration of the short-circuit condition shall not exceed one second.

4/ I_{CC} is measured with $\overline{G}1$, $\overline{G}2$, and CLK at 4.5 V.

5/ Functional tests shall be conducted at input test conditions of GND ≤ V_{IL} ≤ V_{OL} and V_{IH} ≤ V_{CC}.

6/ Subgroup 9 testing is performed at V_{CC} = 5.0 V. Subgroups 10 and 11 testing is performed at V_{CC} = 4.5 V and repeated at V_{CC} = 5.5 V.

7/ For subgroups 10 and 11, f_{MAX}, if not tested, shall be guaranteed to the specified limit.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

Case outlines	R, S, and 2
Terminal number	Terminal symbols
1	S0
2	$\overline{G}1$
3	$\overline{G}2$
4	G/Q_G
5	E/Q_E
6	C/Q_C
7	A/Q_A
8	$Q_{A'}$
9	$\overline{CLR}$
10	GND
11	SR
12	CLK
13	B/Q_B
14	D/Q_D
15	F/Q_F
16	H/Q_H
17	$Q_{H'}$
18	SL
19	S1
20	V_{CC}

FIGURE 1. Terminal connections.

Mode	Inputs								I/O ports								Outputs	
				Output control														
	$\overline{CLR}$	S1	S0	$\overline{G}1$*	$\overline{G}2$*	CLK	SL	SR	A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	$Q_{A'}$	$Q_{H'}$
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

* When one or both output controls are high, the eight input/output terminals are disabled to the high impedance state; however, sequential operation or clearing of the register is not affected.

a...h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

↑ = Clock transition from low to high
H = High voltage level
L = Low voltage level
X = Irrelevant

FIGURE 2. Truth table.

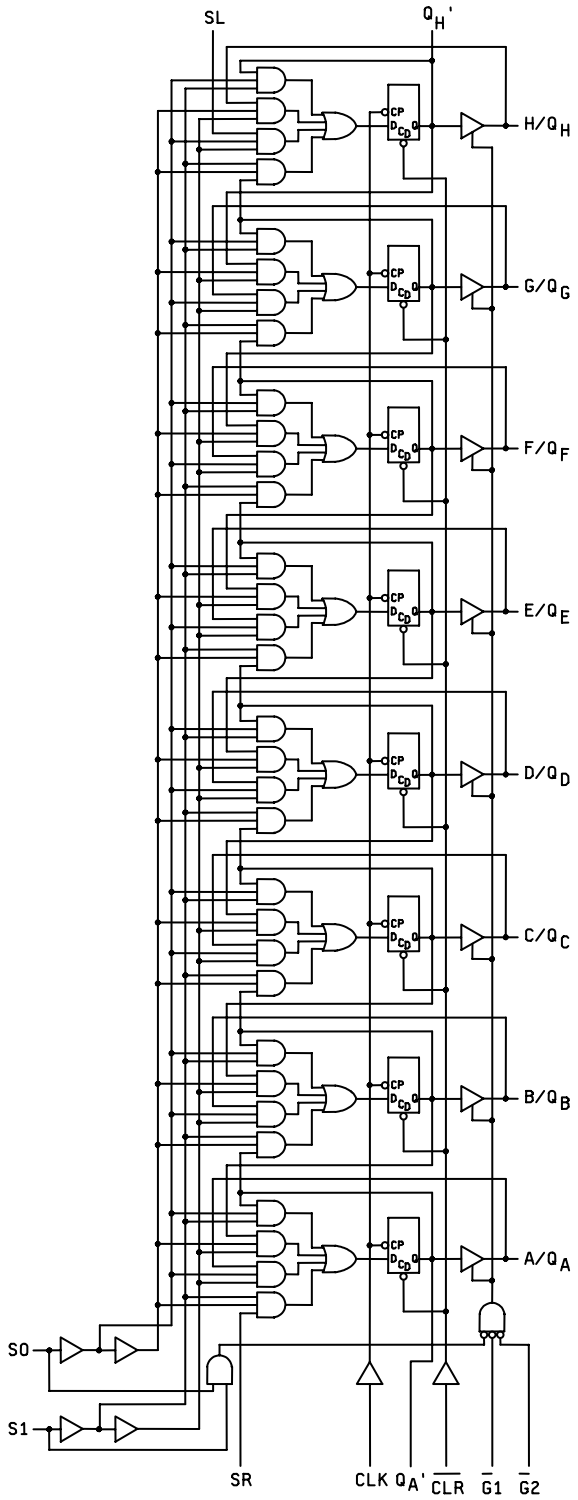


FIGURE 3. Logic diagram.

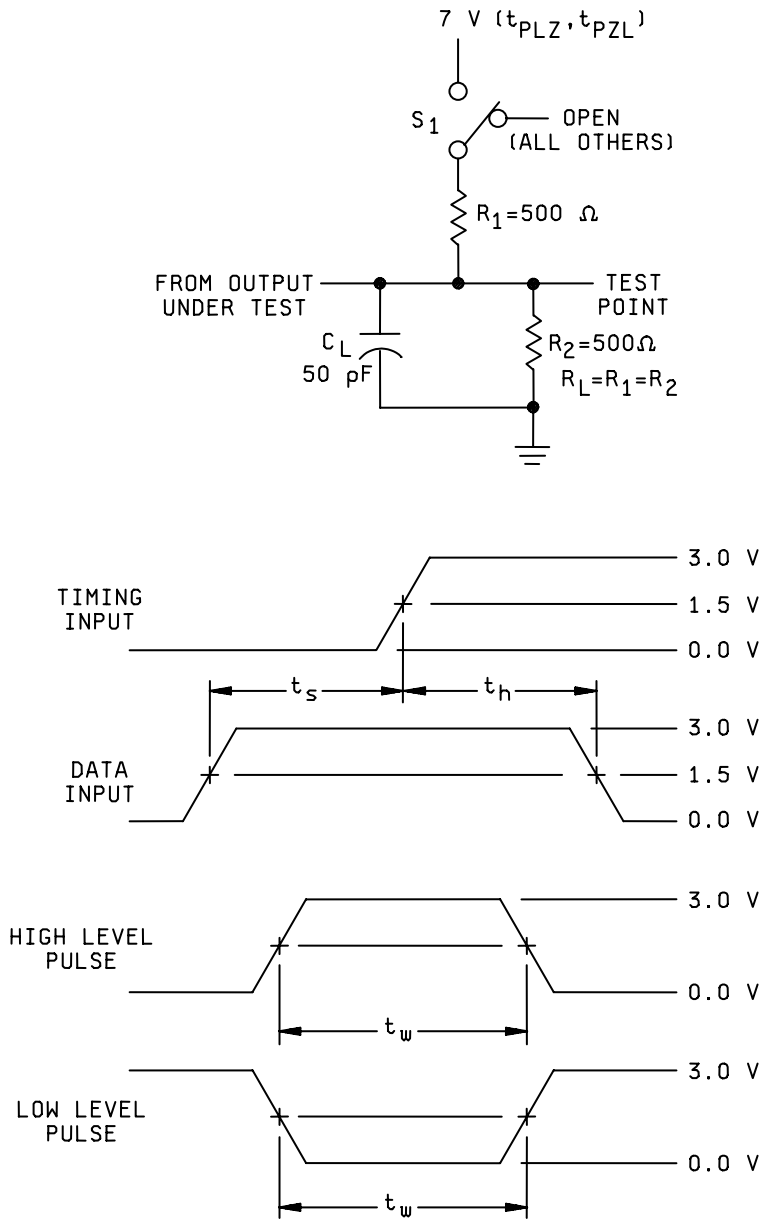
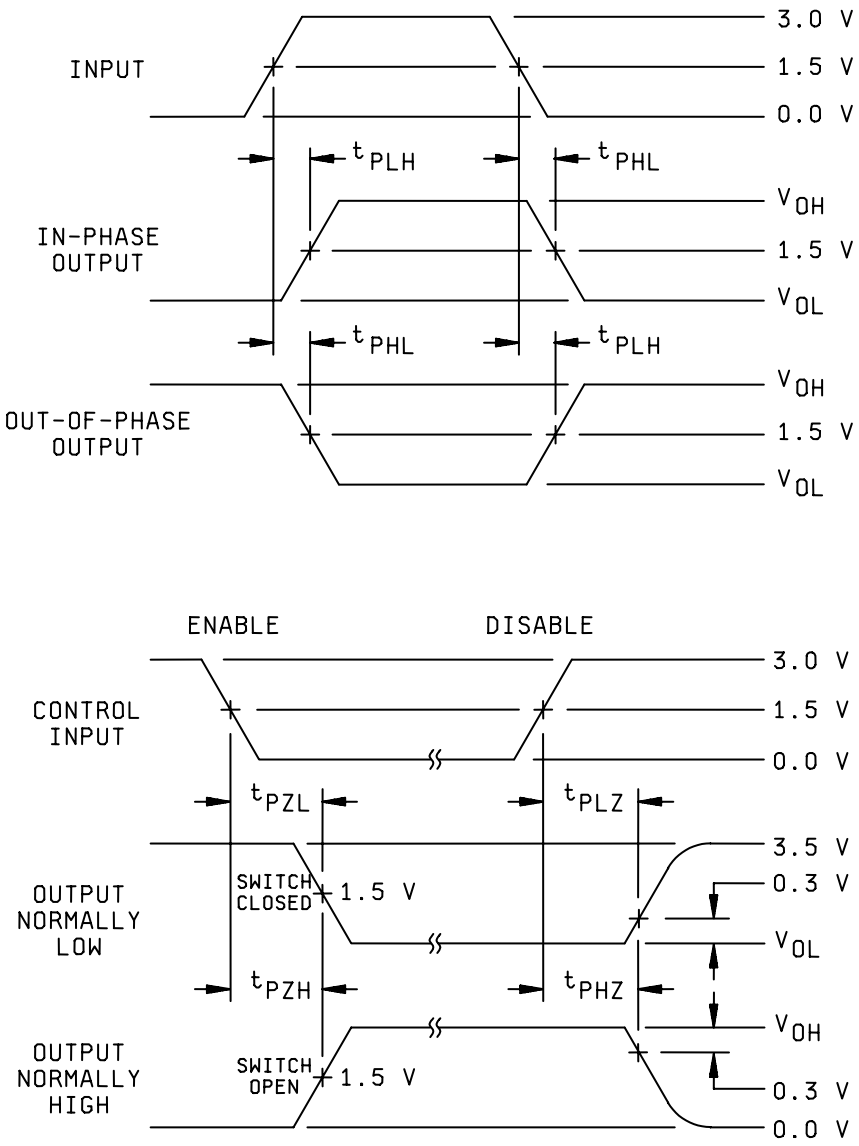


FIGURE 4. Test circuit and switching waveforms.



NOTES:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses have the following characteristics: PRR = 1 MHz, $t_r = t_f = 2.5$ ns, duty cycle = 50 percent.
4. When measuring propagation delay times of three-state outputs, switch 1 is open.
5. When measuring pulse widths, $t_r = t_f \leq 1$ ns.
6. The outputs are measured one at a time with one input transition per measurement.

FIGURE 4. Test circuit and switching waveforms - Continued.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-06-05

Approved sources of supply for SMD 5962-89573 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8957301RA	3V146	54F299/BRA
	0C7V7	54F299DMQB
	3/	SNJ54F299J
5962-8957301SA	3V146	54F299/BSA
	0C7V7	54F299FMQB
	3/	SNJ54F299W
5962-89573012A	3V146	54F299/B2A
	0C7V7	54F299LMQB
	3/	SNJ54F299FK

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051
3V146	Rochester Electronics Inc. 17 Malcolm Hoyt Drive Newburyport, MA 01950

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.