REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Updated boilerplate. Moved endurance and data retention testing requirements from Section 4 of drawing to Section 3 of drawing. Editorial changes throughout.	94-05-31	M. A. Frye
B	Updated boilerplate as part of 5-year review. - glg	10-07-30	Charles Saffle

REV																				
SHEET																				
REV	B	B																		
SHEET	15	16																		

REV STATUS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

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DRAWING APPROVAL DATE
90-09-27

REVISION LEVEL
B

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUITS, MEMORY, DIGITAL, CMOS, 512 X 8 BIT SERIAL EEPROM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-89590**

SHEET 1 OF 16

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-89590	01	P	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Endurance
01	24C04	512 X 8 serial EEPROM	10,000 cycles

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
P	GDIP1-T8 or CDIP2-T8	8	Dual-in-line

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/

Supply voltage ..... -0.3 V dc to +6.50 V dc
Temperature under bias ..... -65°C to +135°C
Storage temperature range ..... -65°C to +150°C
Voltage on any pin with respect to ground ..... -1.0 V to +6.5 V
DC output current ..... 5 mA
Maximum power dissipation ..... 100 mW
Junction temperature (T_J) ..... +175°C 2/
Thermal resistance, junction to case ..... See MIL-STD-1835
Lead temperature (soldering, 10 seconds) ..... +300°C
Input voltage range ..... -0.3 V to +6.5 V
Endurance (minimum) ..... 10,000 cycles
Data retention (minimum) ..... 10 years

1.4 Recommended operating conditions.

Operating supply voltage ..... +4.5 V dc to +5.5 V dc
Case operating temperature range (T_C) ..... -55°C to +125°C.
High level input voltage (V_{IH}) ..... V_{CC} x 0.7 to V_{CC} + 0.5 V dc
Low level input voltage (V_{IL}) ..... -1.0 V dc to V_{CC} x 0.3

1/ Unless otherwise specified, all voltages are referenced to ground.
2/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Power supply current	I_{CC}	f_{SCL} = 100 kHz	1, 2, 3		3.0	mA
Standby current	I_{SB}	$V_{IN} = V_{CC}$	1, 2, 3		200	µA
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}	1, 2, 3		±10	µA
Output leakage current	I_{LO}	V_{OUT} = GND to V_{CC}	1, 2, 3		±10	µA
Input low voltage	V_{IL} 2/		1, 2, 3	-1.0	V_{CC} X 0.3	V
Input high voltage	V_{IH} 2/		1, 2, 3	V_{CC} X 0.7	V_{CC} + 0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.0 mA,	1, 2, 3		0.4	V
I/O capacitance (SDA)	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1 MHz see 4.3.1c 3/, 4/	4		8	pF
Input capacitance (A_0, A_1, A_2, SCL)	C_{IN}	V_{IN} = 0 V, f = 1 MHz see 4.3.1c 3/, 4/	4		6	pF
Functional tests		See 4.3.1d	7, 8A, 8B			
SCL clock frequency	f_{SCL}		9, 10, 11		100	kHz
Bus free time	t_{DHDL}		9, 10, 11	4.7		µs
Start hold time	t_{DVCL}		9, 10, 11	4.0		µs
Clock low period	t_{CLCH}		9, 10, 11	4.7		µs
Clock high period	t_{CHCL}		9, 10, 11	4.0		µs
Start setup time	t_{CHDL}		9, 10, 11	4.7		µs

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Data in hold time	t_{CLDX}		9, 10, 11	0		µs
Data in setup time	t_{DVCH}		9, 10, 11	250		ns
SDA/SCL rise time	t_R 5/		9, 10, 11		1	µs
SDA/SCL fall time	t_F 5/		9, 10, 11		300	ns
Stop setup time	t_{CHDH}		9,10,11	4.7		µs
SCL low to SDA out	t_{CLQV}		9, 10, 11	0.3	3.5	µs
Data out hold time	t_{CLQX}		9, 10, 11	300		ns
Write cycle time	t_{WR} 6/		9, 10, 11	10		ms

1/ Equivalent ac test conditions:
Output load: CL = 100 pF (see figure 5).
Input pulse levels: V_{CC} x 0.1 to V_{CC} x 0.9. Input and output timing levels: V_{CC} x 0.5.
Input rise and fall times: < 10 ns (see figure 4).
2/ V_{IL} minimum and V_{IH} maximum are for reference only and are not tested.
3/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
4/ All pins not being tested are to be open.
5/ t_R and t_F as measured between the 10 percent and 90 percent points of the input pulse levels are periodically sampled and not 100-percent tested (see figures 4 and 6).
6/ t_{WR} is the maximum time for the device to perform its internal write operation; from the system perspective this is a minimum.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. Defense Supply Center Columbus (DSCC), DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.11 Processing EEPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.11.1 Erasure of EEPROMS. When specified, devices shall be erased in accordance with the manufacturer’s test procedures or optionally all locations may be written to logic “1” in byte or page mode as specified in 4.4 and table I herein.

3.11.2 Programmability of EEPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.4 and table I herein.

3.11.3 Verification of state of EEPROMS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of reading the device in accordance with the procedures and characteristics specified in 4.4.1. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.12 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitors. This reprogrammability test shall be done for initial characterization and after any design or process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but shall guarantee the number of program/erase endurance cycles listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

3.13 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process change, which may affect data retention. The methods and procedures may be vendor specific, but shall guarantee the number of years listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D or F. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Prior to burn-in, devices shall be programmed with a topological alternating bit pattern. The pattern shall be read before and after burn in. Devices having bits not in the proper state after burn in shall constitute a device failure and shall be included in the PDA calculation.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. After the completion of all screening, the device shall be erased and verified prior to delivery.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 ($C_{I/O}$ and C_{IN} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is fifteen devices with no failures and all input and output terminals tested.

d. Subgroups 7 and 8 shall test sufficient to verify the truth table.

e. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified, (except devices submitted for groups B, C, and D testing).

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. All devices requiring end-point electrical testing shall be programmed with a topologically alternating bit pattern.

c. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D or F. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

d. After the completion of all screening, the device shall be erased and verified prior to delivery.

Device type	01
Case Outline	P
Terminal Number	Terminal Symbol
1	A0 (see note 1)
2	A1 (see note 3)
3	A2 (see note 3)
4	V_{SS}
5	SDA (see note 2)
6	SCL (see note 2)
7	TEST (see note 1)
8	V_{CC}

NOTES:
1. Pins marked with this notation symbol are reserved for manufacturer's test modes and should be tied to ground for proper device operation.
2. SDA and SCL require external pull-up resistors.
3. A_1 and A_2 are used to set the least significant two bits of the six bit slave address. These inputs can be used static or driven. If used statically, they must be tied to V_{SS} or V_{CC} as appropriate. If driven, they must be driven by open collector outputs with resistor pull-ups to V_{CC}.

FIGURE 1. Terminal connections.

Precondition R/W bit	SCL	SDA	Operation
N/A	High	¯_	Start condition
N/A	High	_/¯	Stop condition
1	¯_	Data out	Read
0	¯_	Data in	Write

FIGURE 2. Truth table.

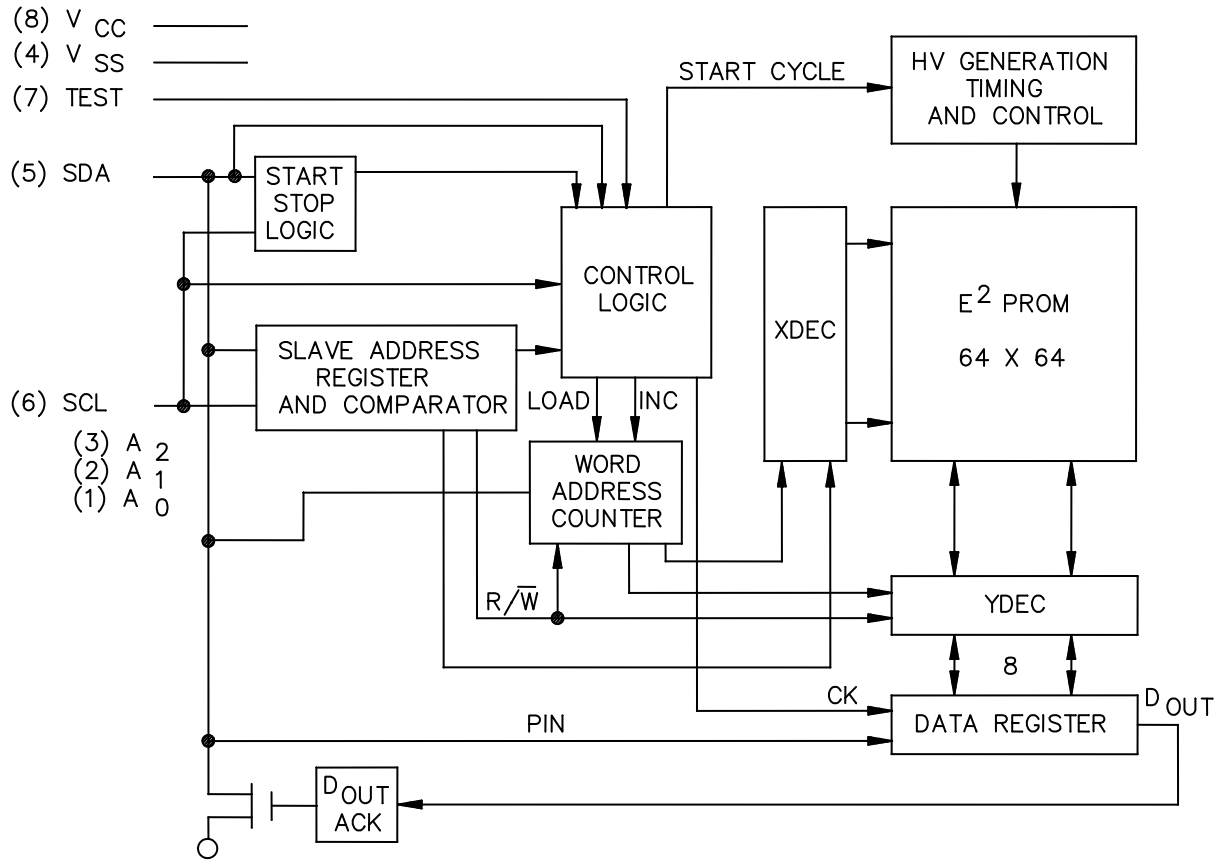
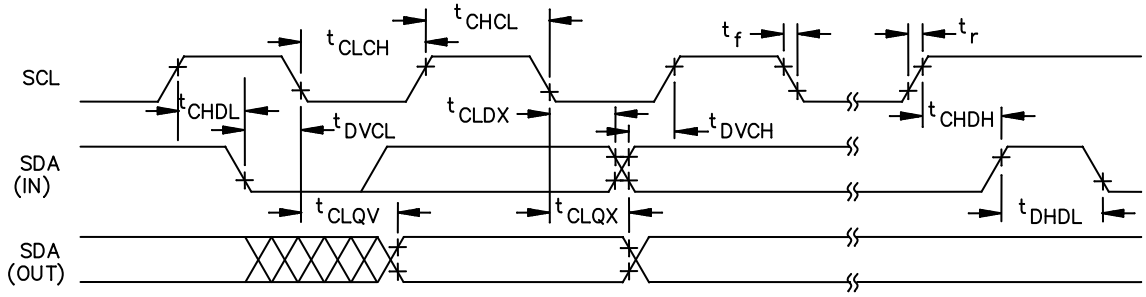
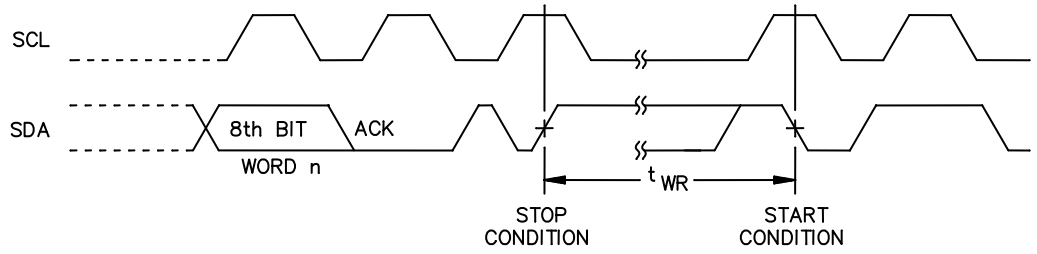


FIGURE 3. Block Diagram.

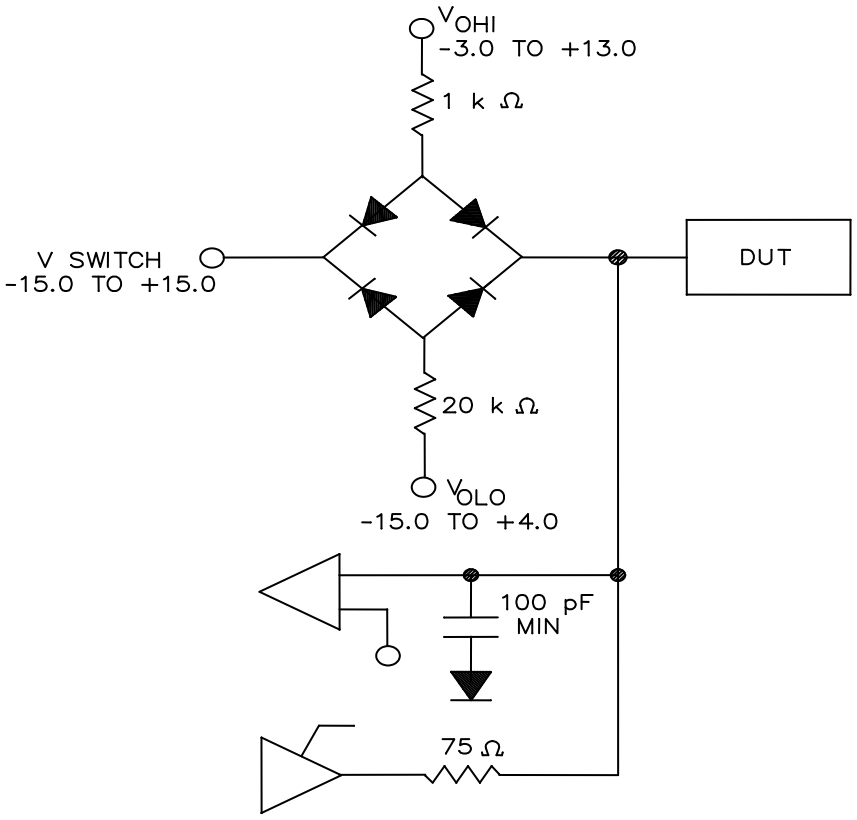
READ CYCLE TIMING





WRITE CYCLE TIMING

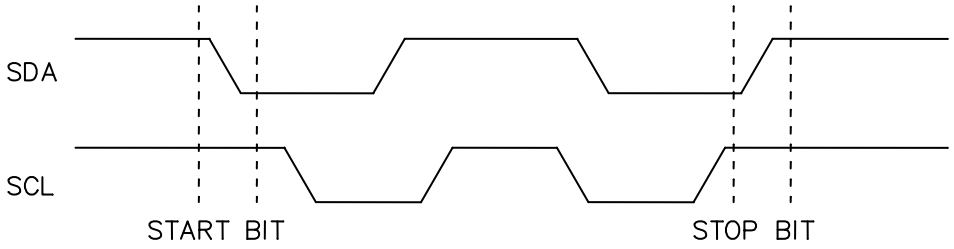
FIGURE 4. Switching waveforms.

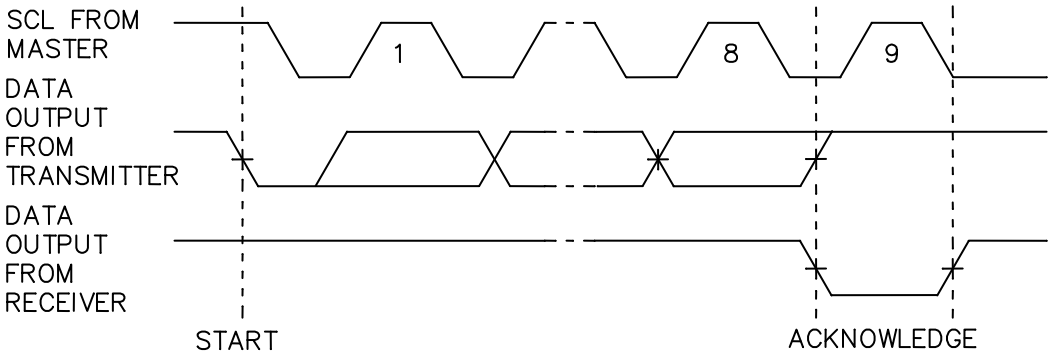


NOTE: V_{OHI} will be adjusted to meet load conditions I_{OL} = 3 mA of table I.

FIGURE 5. Switching load circuit.

START/STOP CONDITION

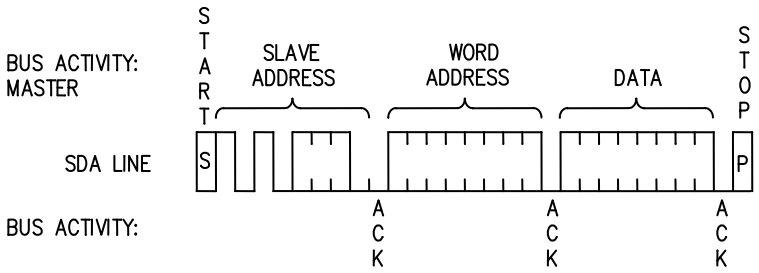


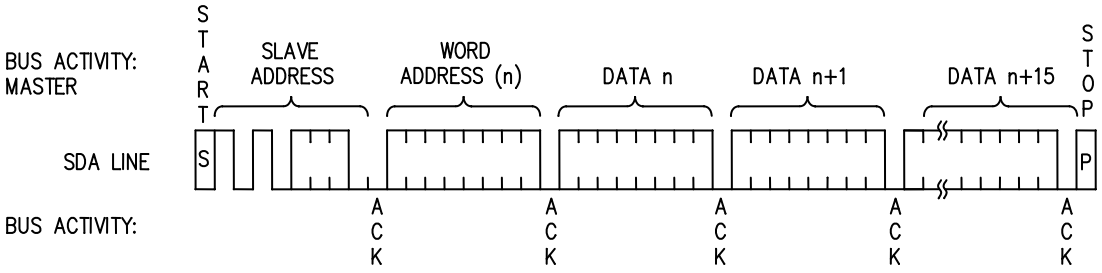


ACKNOWLEDGE RESPONSE

FIGURE 6. Bus sequence diagrams.

BYTE WRITE BUS ACTIVITY

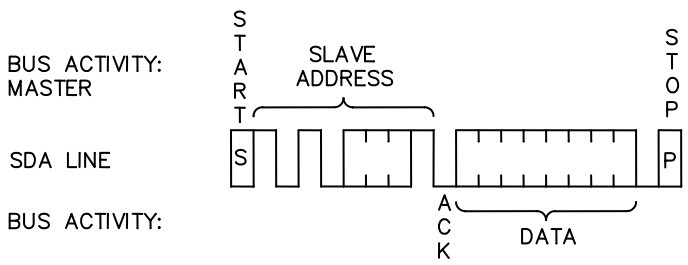


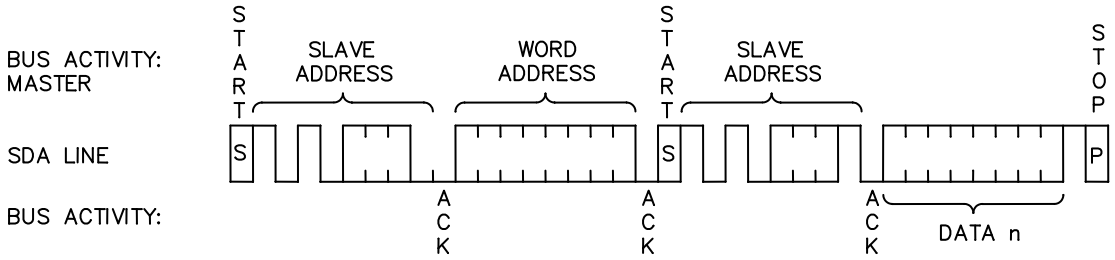


PAGE WRITE BUS ACTIVITY

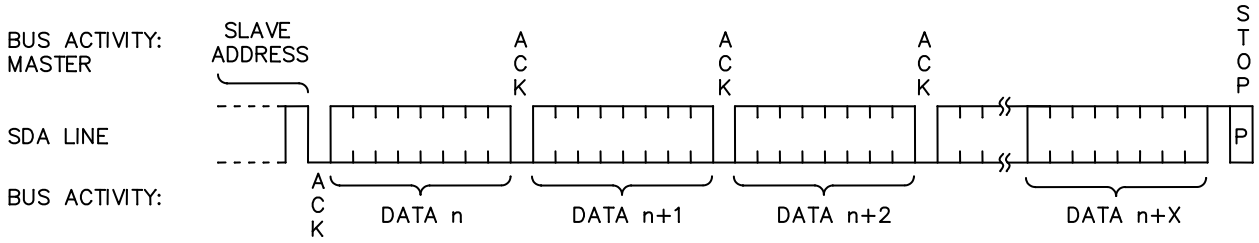
FIGURE 6. Bus sequence diagrams - continued.

CURRENT ADDRESS
READ BUS ACTIVITY





RANDOM READ
BUS ACTIVITY



SEQUENTIAL ADDRESS
READ BUS ACTIVITY

FIGURE 6. Bus sequence diagrams - continued.

TABLE II. Electrical test requirements. 1/ 2/ 3/

MIL-STD-883 test requirements	Subgroups(per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
Group A test requirements (method 5005)	1,2,3,4**,7,8A,8B,9, 10,11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3, 7, 8A, 8B, 9, 10, 11

1/ (*) PDA applies to subgroups 1 and 7 (see 4.2a).

2/ Any subgroups at the same temperature may be combined when using a multifunction tester.

3/ (**) Indicates that subgroup 4 will only be performed during initial qualification or after a design or process change that may affect capacitance.

4.4 Programming procedure. The programming procedures shall be as specified by the device manufacturer. The following procedure shall be followed when programming (write) is performed. The waveforms and timing relationships shown on figure 4 and the sequences of data transfers illustrated on figure 5 and the conditions specified in table I shall be adhered to. Information is introduced in a serial fashion: The sequence is to issue a start condition (SCL HIGH with a HIGH to LOW transition of SDA) followed by first the device address and the R/W bit of the data stream LOW. After receipt of an ACK response from the memory device 8 bits of data (one byte) is clocked into the device. The transfer is terminated and the data written into the E^2 array by issuing a stop condition (SCL HIGH with a LOW to HIGH transition of SDA).

4.4.1 Read mode operation. The following procedure shall be followed when reading data. A start condition will be issued to the device followed by device address and R/W bit set HIGH, the device will respond with an ACK and begin outputting data on subsequent clock pulses. The waveforms and timing relationships shown on figure 4 and the sequences of data transfers illustrated on figure 5 and the conditions specified in table I shall be adhered to.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 10-07-30

Approved sources of supply for SMD 5962-89590 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 3/
5962-8959001PA	2/	X24C04DMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Not available from an approved source. The last known source Is listed below.

3/ Caution: Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
60395	XICOR, Incorporated 851 Buckeye Court Milpitas, CA 95035-7493