REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Drawing updated to reflect current requirements. Invoked dimensional requirements in accordance with CDIP3-T28 and GDIP4-T28 of MIL-STD-1835 for case outline X. Editorial changes throughout. - gap	00-11-16	Raymond Monnin
B	Boilerplate update and part of five year review. tcr	07-02-28	Robert M. Heber
C	Update drawing to meet current MIL-PRF-38535 requirements. – glg	15-09-11	Charles Saffle

THE FRONT PAGE OF THIS DRAWING HAS BEEN REPLACED

REV																				
SHEET																				
REV	C																			
SHEET	15																			

REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Steve L. Duncan

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Charles Reusing

APPROVED BY
William K. Heckman

DRAWING APPROVAL DATE
89-08-22

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, CASCADABLE 64 X 8 FIFO, MONOLITHIC SILICON

REVISION LEVEL
C

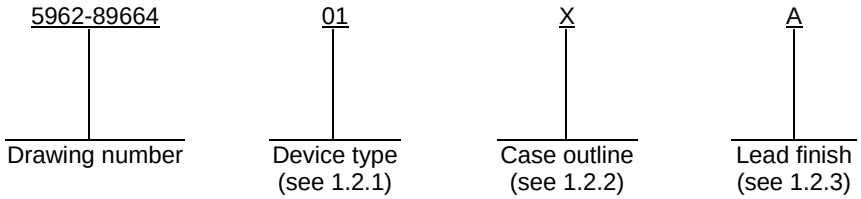
SIZE	CAGE CODE	
A	**67268**	**5962-89664**

SHEET 1 OF 15

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Shift rate
01	7C408A-15	64 X 8 FIFO	15 MHz
02	7C408A-25	64 X 8 FIFO	25 MHz

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDIP3-T28 or GDIP4-T28	28	Dual-in-line package
Y	GDFP2-F28	28	Flat package
3	CQCC1-N28	28	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
DC voltage applied to outputs	-0.5 V dc to +7.0 V dc
DC Input voltage	-3.0 V dc to +7.0 V dc
DC output current	20 mA
Maximum power dissipation	1.0 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases X, Y, and 3	See MIL-STD-1835
Junction temperature (T_J) 1/	+150°C
Storage temperature range	-65°C to +150°C
Temperature under bias	-55°C to +125°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Ground voltage (GND)	0 V dc
Input high voltage (V_{IH})	2.2 V dc minimum
Input low voltage (V_{IL})	0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

1/ Maximum junction temperature may be increased to +175°C during burn-in and steady-state life tests.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.4 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection only. Each coated microcircuit inspection lot (see inspection lot as defined in MIL-PRF-38535) shall be subjected to and pass the internal moisture content test at 5000 ppm (see method 1018 of MIL-STD-883). The frequency of the internal water vapor testing shall not be decreased unless approved by the preparing activity for class M. The TRB will ascertain the requirements as provided by MIL-PRF-38535 for classes Q and V. Samples may be pulled any time after seal.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified 1/	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -4.0 mA $V_{IN} = V_{IH}, V_{IL}$	1, 2, 3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8.0 mA $V_{IN} = V_{IH}, V_{IL}$	1, 2, 3	All		0.4	V
Input high voltage	V_{IH} 2/		1, 2, 3	All	2.2		V
Input low voltage	V_{IL} 2/		1, 2, 3	All		0.8	V
Input leakage current	I_{IX}	V_{IN} = 5.5 V to GND	1, 2, 3	All	-10	10	µA
Output leakage current	I_{OZ}	V_{CC} = 5.5 V, V_{OUT} = 5.5 V and GND	1, 2, 3	All	-10	10	µA
DC supply current	I_{CC1}	V_{CC} = 5.5 V, I_{OUT} = 0 mA V_{IN} = 0 V and 3 V, f = 0	1, 2, 3	All		125	mA
Operating supply current	I_{CC2}	V_{CC} = 5.5 V, I_{OUT} = 0 mA V_{IN} = 0 V and 3 V	1, 2, 3	All		3/	
Input capacitance	C_{IN}	V_{CC} = 5.0 V T_A = +25°C, f = 1 MHz See 4.3.1c	4	All		8	pF
Output capacitance	C_{OUT}	V_{CC} = 5.0 V T_A = +25°C, f = 1 MHz See 4.3.1c	4	All		8	pF
Functional tests		See 4.3.1d	7, 8	All			
Operating frequency	f_O 4/		9, 10, 11	01		15	MHz
				02		25	
SI high time	t_{PHSI} 4/	See figure 4	9, 10, 11	01	23		ns
				02	11		
SI low time	t_{PLSI} 4/		9, 10, 11	01	25		ns
				02	24		
Data setup to SI	t_{SSI} 5/		9, 10, 11	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified 1/	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Data hold from SI	t_{HSI} 5/	See figure 4	9, 10, 11	01	30		ns
				02	20		
Delay, SI high to IR low	t_{DLIR}		9, 10, 11	01		35	ns
				02		21	
Delay, SI low to IR high	t_{DHIR}		9, 10, 11	01		40	ns
				02		23	
SO high time	t_{PHSO} 4/		9, 10, 11	01	23		ns
				02	11		
SO low time	t_{PLSO} 4/		9, 10, 11	01	25		ns
				02	24		
Delay, SO high to OR low	t_{DLOR}		9, 10, 11	01		35	ns
				02		21	
Delay, SO low to OR high	t_{DHOR}		9, 10, 11	01		40	ns
				02		23	
Data Setup to OR high	t_{SOR}		9, 10, 11	All	0		ns
Data hold from SO low	t_{HSO}		9, 10, 11	All	0		ns
Fallthrough, bubbleback time	t_{BT}		9, 10, 11	01	10	65	ns
				02	10	60	
Data setup to IR	t_{SIR} 6/		9, 10, 11	All	5		ns
Data hold from IR	t_{HIR} 6/		9, 10, 11	01	30		ns
				02	20		
Input ready pulse high	t_{PIR} 7/		9, 10, 11	All	6		ns
Output ready pulse high	t_{POR} 8/		9, 10, 11	All	6		ns
$\overline{OE}$ low to low Z	t_{DLZOE} 9/ 10/		9, 10, 11	01		35	ns
				02		30	
$\overline{OE}$ high to high Z	t_{DHZOE} 9/ 10/		9, 10, 11	01		35	ns
				02		30	
SI low to HF high	t_{DHHF}		9, 10, 11	01		65	ns
				02		55	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified 1/	Group A subgroups	Device types	Limits		Unit
					Min	Max	
SO low to HF low	t_{DLHF}	See figure 4	9, 10, 11	01		65	ns
				02		55	
SO or SI low to AFE low	t_{DLAFE}		9, 10, 11	01		65	ns
				02		55	
SO or SI low to AFE high	t_{DHAFE}		9, 10, 11	01		65	ns
				02		55	
$\overline{MR}$ pulse width	t_{PMR}		9, 10, 11	01	55		ns
				02	45		
$\overline{MR}$ high to SI high	t_{DSI}		9, 10, 11	01	25		ns
				02	10		
$\overline{MR}$ low to OR low	t_{DOR}		9, 10, 11	01		55	ns
				02		45	
$\overline{MR}$ low to IR high	t_{DIR}		9, 10, 11	01		55	ns
				02		45	
$\overline{MR}$ low to output low	t_{LZMR} 11/		9, 10, 11	01		55	ns
				02		45	
$\overline{MR}$ low to AFE high	t_{AFE}		9, 10, 11	01		55	ns
				02		45	
$\overline{MR}$ low to HF low	t_{HF}		9, 10, 11	01		55	ns
				02		45	

1/ AC tests are performed with input rise and fall times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output load on figure 3, circuit A.

2/ These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.

3/ Subgroups 1, 2, and 3 tests for I_{CC2} shall be tested to the calculated limit for initial test and after any design or process changes which may affect this parameter. To calculate I_{CC2} at any given operating frequency, use I_{CC1} + (1 mA/MHz) x $(1/f_{osi} + 1/f_{oso})/2$.

4/ $1/f_O \ge (t_{PHSI} + t_{PLSI})$, $1/f_O \ge (t_{PHSO} + t_{PLSO})$.

5/ The parameters t_{SSI} and t_{HSI} apply when memory is not full.

6/ The parameters t_{SIR} and t_{HIR} apply when memory is full, SI is high and minimum bubblethrough (t_{BT}) conditions exist.

7/ At any given operating condition $t_{PIR} \ge (t_{PHSO}$ required).

8/ At any given operating condition $t_{POR} \ge (t_{PHSI}$ required).

9/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.

10/ The parameter t_{DHZOE} transition is measured at steady-state high level -500 mV or steady-state low level +500 mV on the output from the 1.5 V level on the input with the load in figure 3, circuit B. The parameter t_{DLZOE} is measured ±100 mV from steady-state voltage with the load in figure 3, circuit B.

11/ All data outputs will be at low level after reset goes high until data is entered into the FIFO.

Device types	All
Case outlines	X, Y, and 3
Terminal number	Terminal symbol
1	AFE
2	HF
3	IR
4	SI
5	DI_0
6	DI_1
7	GND
8	DI_2
9	DI_3
10	DI_4
11	DI_5
12	DI_6
13	DI_7
14	NC
15	$\overline{OE}$
16	DO_7
17	DO_6
18	DO_5
19	DO_4
20	DO_3
21	DO_2
22	GND
23	DO_1
24	DO_0
25	OR
26	SO
27	$\overline{MR}$
28	V_{CC}

FIGURE 1. Terminal connections.

Mode	Input control				Output control	
	SI	SO	$\overline{MR}$	$\overline{OE}$	IR	OR
Read	X	See note 1	H	L	X	H
Write	See note 2	X	H	X	H	X
Reset	X	X	L	X	X	X
Disable	X	X	X	H	X	X

NOTES:
1. High to low transition.
2. Low to high transition.

FIGURE 2. Truth table .

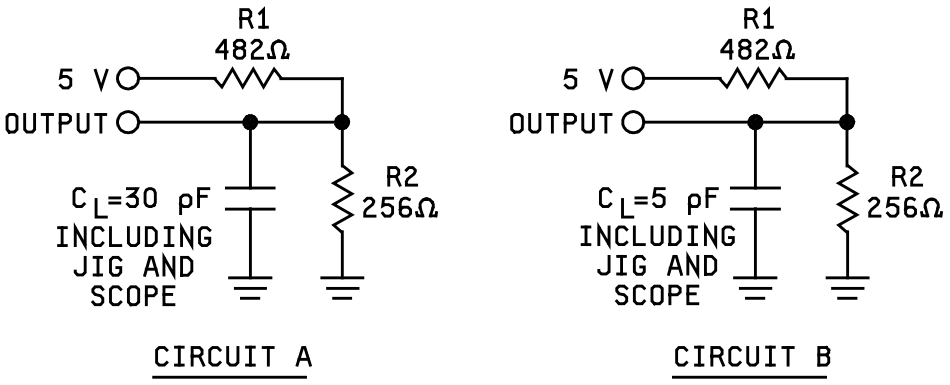
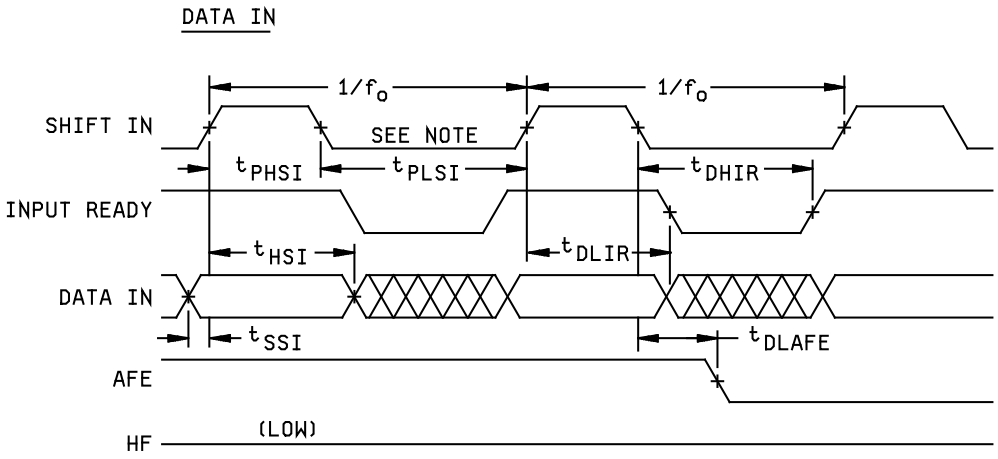
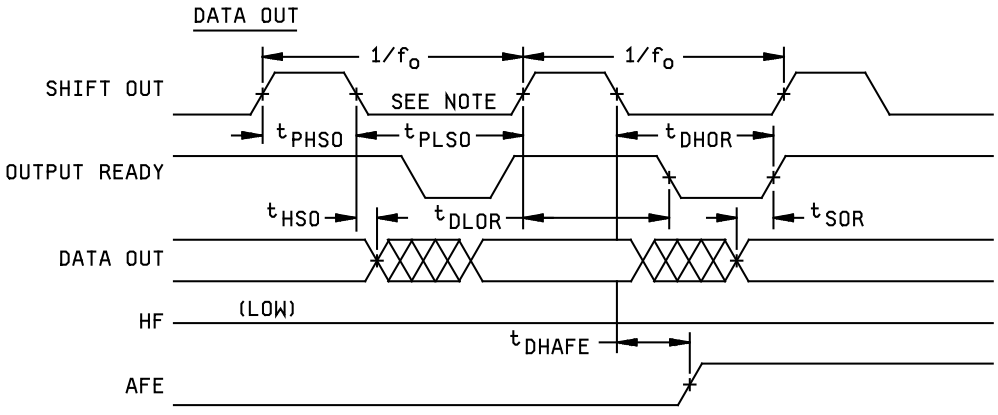


FIGURE 3. Output load circuit.

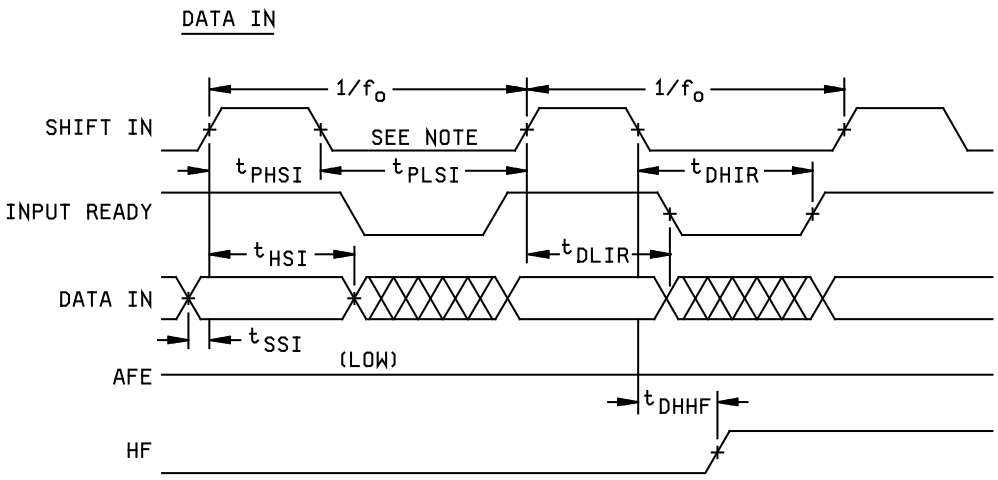


NOTE: FIFO contains 8 words.

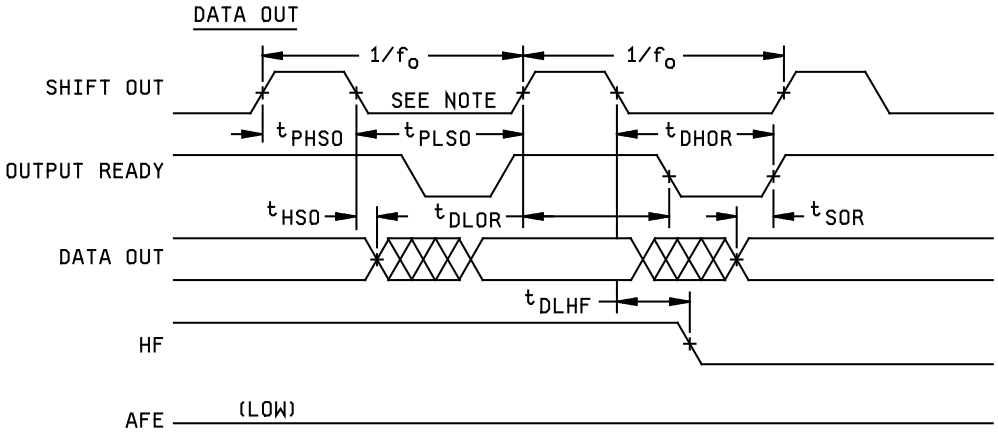


NOTE: FIFO contains 9 words.

FIGURE 4. Timing waveforms.



NOTE: FIFO contains 31 words.



NOTE: FIFO contains 32 words.

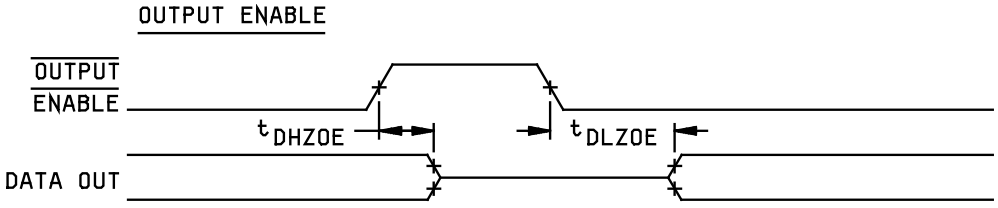
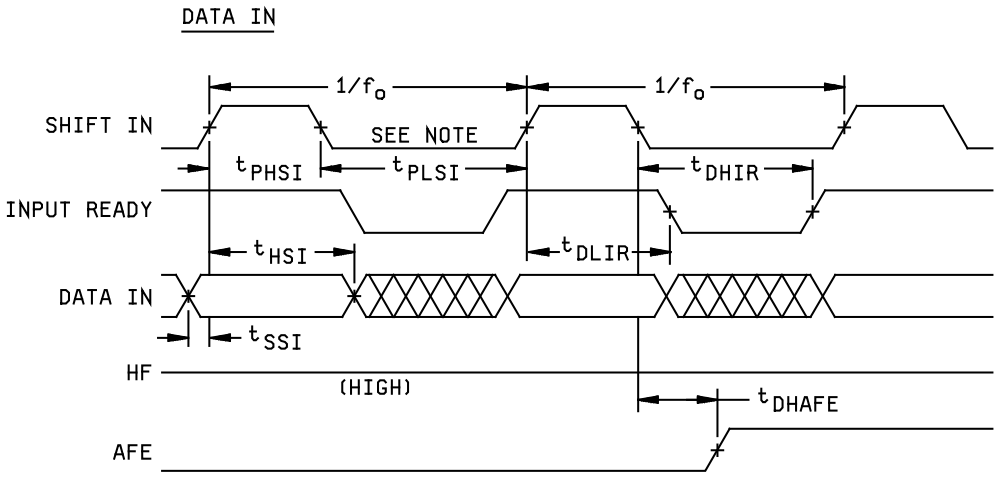
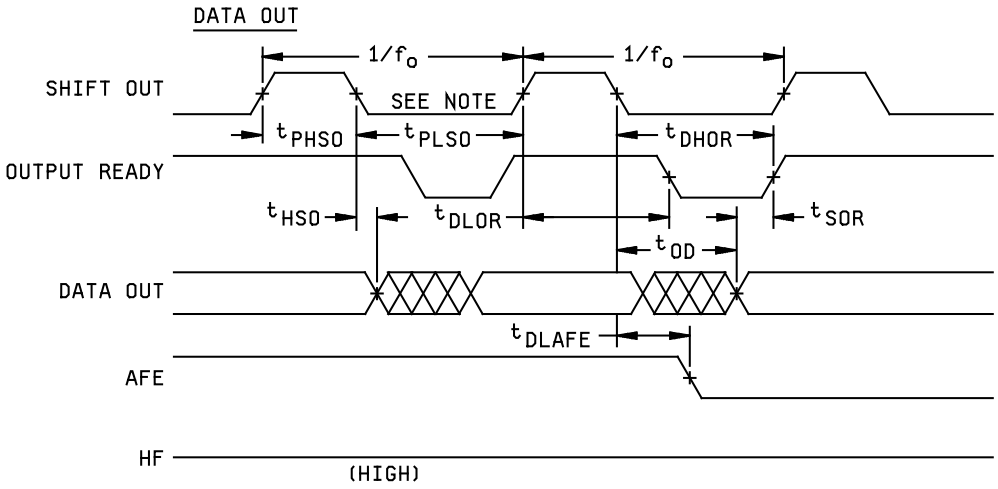


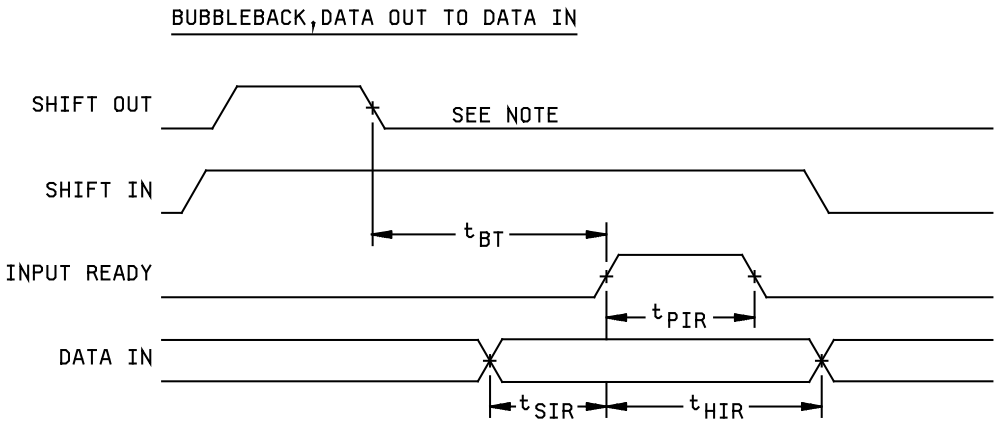
FIGURE 4. Timing waveforms - Continued.



NOTE: FIFO contains 55 words.



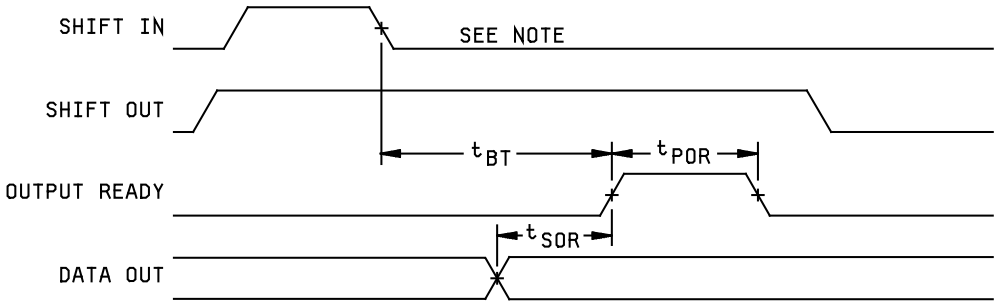
NOTE: FIFO contains 56 words.



NOTE: FIFO contains 64 words.

FIGURE 4. Timing waveforms - Continued.

FALLTHROUGH, DATA IN TO DATA OUT



NOTE: FIFO is empty.

MASTER RESET

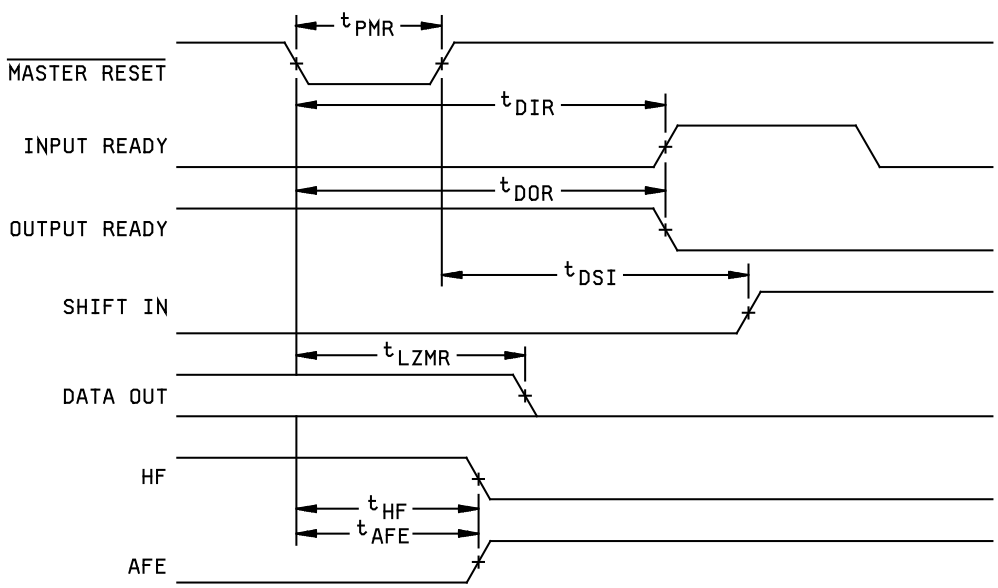


FIGURE 4. Timing waveforms - Continued.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4**, 7***, (8A and 8B)***, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8A, 8B

* PDA applies to subgroup 1 and 7.
** For subgroup 4, see 4.3.1c.
*** For subgroups 7, and 8, see 4.3.1d.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect input or output capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-0540.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-8108.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 15-09-11

Approved sources of supply for SMD 5962-89664 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8966401XA	0C7V7	CY7C408A-15DMB
5962-8966401YA	0C7V7	CY7C408A-15KMB
5962-89664013A	0C7V7	CY7C408A-15LMB
5962-8966402XA	0C7V7	CY7C408A-25DMB
5962-8966402YA	0C7V7	CY7C408A-25KMB
5962-89664023A	0C7V7	CY7C408A-25LMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
0C7V7	e2v, Inc. dba QP Semiconductor Inc. 765 Sycamore Drive Milpitas, CA 95035