REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Updated document. Added three device types 04, 05, and 06. Added S package. Added two vendors. Editorial changes throughout.	91-08-23	M. A. Frye
B	Update boilerplate. Add device type 07 for vendor 66675. Editorial changes throughout.	94-07-12	M. A. Frye
C	Add device types 08 through 10. Update boilerplate. Editorial changes throughout.	95-05-12	M. A. Frye
D	Add device types 11 through 14. Update boilerplate. ksr	98-12-04	Raymond Monnin
E	Lower t_{PD} and t_{CO} minimum value by 1 ns for devices 01, 02, and 03. ksr	99-08-04	Raymond Monnin
F	Boilerplate update, part of 5 year review. ksr	07-04-24	Robert M. Heber

THE ORIGINAL FIRST PAGE HAS BEEN REPLACED

REV																				
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SHEET																				

REV STATUS	REV	F	F	F	F	F	F	F	F	F	F	F	F	F	
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	

PMIC N/A

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DRAWING APPROVAL DATE
89-12-18

REVISION LEVEL
F

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

MICROCIRCUIT, MEMORY, DIGITAL, EE PROGRAMMABLE ARRAY LOGIC, MONOLITHIC SILICON

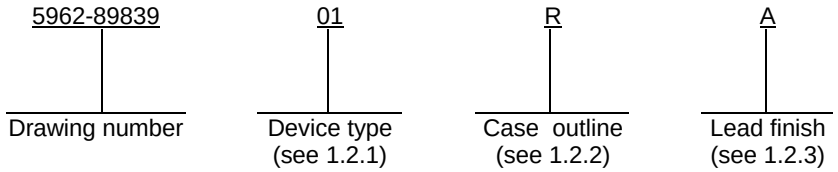
SIZE	CAGE CODE	
A	**67268**	**5962-89839**

SHEET 1 OF 13

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time	current
01	16V8	16-input, 8-output, EECMOS, architecturally generic, programmable AND-OR array	30	130
02	16V8	16-input, 8-output, EECMOS, architecturally generic, programmable AND-OR array	20	130
03	16V8	16-input, 8-output, EECMOS, architecturally generic, programmable AND-OR array	15	130
04, 11	16V8	16-input, 8-output, EECMOS, architecturally generic, programmable AND-OR array	10	130
05	16V8	16-input, 8-output, EECMOS, architecturally generic, programmable AND-OR array	25	65
06	16V8	16-input, 8-output, EECMOS, architecturally generic, programmable AND-OR array	20	65
07	16V8	16-input, 8-output, EECMOS, architecturally generic, programmable AND-OR array	7.5	130
08, 12	16V8	16-input, 8-output, EECMOS, architecturally generic, programmable AND-OR array	25	65
09, 13	16V8	16-input, 8-output, EECMOS, architecturally generic, programmable AND-OR array	15	130
10, 14	16V8	16-input, 8-output, EECMOS, architecturally generic, programmable AND-OR array	15	65

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
S	GDFP2-F20 or CDFP3-F20	20	Flat package
2	CQCC1-N20	20	Square chip carrier package

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range applied	-2.5 V dc to V_{CC} + 1.0 V dc 1/
Off-state output voltage range applied	-2.5 V dc to V_{CC} + 1.0 V dc 1/
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 2/	1.5 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C
Data retention	10 years (minimum)
Endurance	100 erase/write cycles (minimum)

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
High level input voltage range (V_{IH})	2.0 V dc to V_{CC} + 1.0 V dc
Low level input voltage range (V_{IL})	V_{SS} -0.5 V dc to +0.8 V dc
High level output current (I_{OH})	-2.0 mA maximum
Low level output current (I_{OL})	12 mA maximum
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

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1 Minimum input voltage is -0.5 V dc which may undershoot to -2.5 V dc for pulses less than 20 ns.

2/ Must withstand the added P_D due to short circuit test (e.g., I_{SC}).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V, 4.5 V $\le V_{CC} \le 5.5$ V unless otherwise specified	Device type	Group A sub-groups	Limits		Unit
					Min	Max	
Input leakage current	I_{LX}	0.0 V $\le V_{IN} \le V_{CC}$	01-03, 05,06	1,2,3	-10	10	µA
			04, 07-14		-100	10	
Bidirectional pin leakage current	$I_{I/O/Q}$	0.0 V $\le V_{I/O/Q} \le V_{CC}$	01-03, 05,06	1,2,3	-10	10	µA
			04, 07-14		-100	10	
Output low voltage	V_{OL}	$V_{CC} = 4.5$ V, $I_{OL} = 12$ mA, $V_{IN} = V_{IH}$ or V_{IL}	All	1,2,3		0.5	V
Output high voltage	V_{OH}	$V_{CC} = 4.5$ V, $I_{OH} = -2.0$ mA, $V_{IN} = V_{IH}$ or V_{IL}	All	1,2,3	2.4		V
Input low voltage 1/	V_{IL}		All	1,2,3	V_{SS} -0.5	0.8	V
Input high voltage 1/	V_{IH}		All	1,2,3	2.0	V_{CC} +1.0	V
Operating power supply current 2/	I_{CC}	$V_{IL} = 0.5$ V, $V_{IH} = 3.0$ V, $f_{tog} = 25$ MHz	01-04, 07,09, 11,13	1,2,3		130	mA
			05,06, 08,10, 12,14			65	
Output short circuit current 3/	I_{OS}	$V_{CC} = 5.0$ V, $V_{OUT} = 0.5$ V, $T_A = +25°C$, see 4.3.1d	All	1	-30	-150	mA
Input capacitance	C_{IN}	$V_{CC} = 5.0$ V, $V_I = 2.0$ V, f = 1.0 MHz, $T_A = +25°C$, see 4.3.1c	All	4		10	pF
Bidirectional pin capacitance	$C_{I/O/Q}$	$V_{CC} = 5.0$ V, $V_{I/O/Q} = 2.0$ V, f = 1.0 MHz, $T_A = +25°C$, see 4.3.1c	All	4		10	pF
Functional tests		See 4.3.1e	All	7,8A,8B			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{SS} = 0 V, 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Device type	Group A sub-groups	Limits		Unit
					Min	Max	
Input or feedback to nonregistered output	t_{PD}	V_{CC} = 4.5 V, see figures 3 and 4 4/	01	9,10,11	2.0	30	ns
			02		2.0	20	
			06		3.0	20	
			03		2.0	15	
			09,10, 13,14		3.0	15	
			04		2.0	10	
			05,08, 12		3.0	25	
			07		1.0	7.5	
			11		3.0	10.0	
Clock to output delay 5/	t_{CO}		01	9,10,11	1.0	20	ns
			02		1.0	15	
			06		2.0	15	
			03		1.0	12	
			09,10,12		2.0	12	
			04		1.0	7.0	
			13,14		2.0	10.0	
			05,08		2.0	15	
			07		1.0	6	
			11		2.0	7.0	
Input to output enable	t_{EA1}		01	9,10,11		30	ns
			02,06			20	
			03,09, 10,13,14			15	
			04,11			10	
			05,08, 12			25	
			07			9.0	
Input to output register enable 5/	t_{EA2}		01,08	9,10,11		25	ns
			02,06			18	
			03,09, 10,13,14			15	
			04,11			10	
			05,12			20	
			07			7.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{SS} = 0 V, 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Device type	Group A sub-groups	Limits Min	Limits Max	Unit
Input to output disable 6/	t_{ER1}	V_{CC} = 4.5 V, see figures 3 and 4 4/	01	9,10,11		30	ns
			02,06			20	
			03,09, 10,13,14			15	
			04,11			10	
			05,08, 12			25	
			07			7.0	
Input to output register disable 5/ 6/	t_{ER2}		01,08	9,10,11		25	ns
			02,06			18	
			03,09, 10,13,14			15	
			04,11			10	
			05,12			20	
			07			7.0	
Clock frequency without feedback 5/ 7/	f_{CLK1}		01	9,10,11	0.0	33.3	MHz
			12		0.0	37.0	
			02,06		0.0	41.6	
			13,14		0.0	45.5	
			03,09, 10		0.0	50.0	
			04		0.0	62.5	
			11		0.0	58.0	
			05,08		0.0	33.3	
			07		0.0	100.0	
Clock frequency with feedback 5/	f_{CLK2}		01	9,10,11	0.0	22.2	MHz
			02,06		0.0	33.3	
			12		0.0	40.0	
			03,09, 10		0.0	41.6	
			04		0.0	58.5	
			13,14		0.0	50.0	
			05,08		0.0	28.5	
			11		0.0	62.5	
			07		0.0	76.9	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{SS} = 0 V, 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Device type	Group A sub-groups	Limits Min	Limits Max	Unit
Input or feedback setup time, before rising clock 5/	t_S	V_{CC} = 4.5 V, see figures 3 and 4 4/	01	9,10,11	25		ns
			02,06, 12		15		
			03,09, 10,13,14		12		
			04,11		10		
			05,08		20		
			07		7.0		
Input or feedback hold time after rising clock 5/	t_H		01 - 10	9,10,11	0		ns
			11 - 14		0.5		
Clock pulse width, high 5/	t_{PWH}		01	9,10,11	15		ns
			02,06, 12		12		
			03,09, 10		10		
			04,13,14		8.0		
			05,08		15		
			07		5.0		
			11		6.0		
Clock pulse width, low 5/	t_{PWL}		01	9,10,11	15		ns
			02,06, 12		12		
			03,09, 10		10		
			04,13, 14		8.0		
			05,08		15		
			07		5.0		
			11		6.0		

1/ These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.

2/ This parameter may be tested at a frequency other than 25MHz, but shall be guaranteed to the specified limits at 25MHz.

3/ Not more than one output at a time should be shorted. Short circuit test duration should not exceed 1 second (see 4.3.1d).

4/ AC tests are performed with input rise and fall times (10 percent to 90 percent) of 3.0 ns, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and the output load of figure 3. Input pulse levels are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.

5/ Test applies only to registered outputs.

6/ Transition is measured at steady-state high level -500 mV or steady-state low level +500 mV on the output from the 1.5 V level on the input.

7/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.

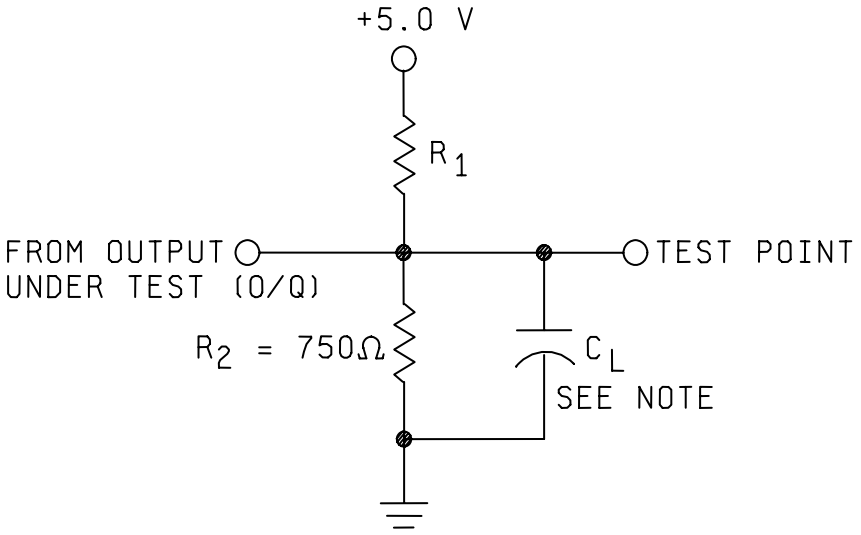
Device types	All
Case outlines	R, S, 2
Terminal number	Terminal symbol
1	I/CLK
2	I
3	I
4	I
5	I
6	I
7	I
8	I
9	I
10	GND
11	I/$\overline{OE}$
12	I/O/Q
13	I/O/Q
14	I/O/Q
15	I/O/Q
16	I/O/Q
17	I/O/Q
18	I/O/Q
19	I/O/Q
20	V_{CC}

FIGURE 1. Terminal connections.

Inputs										Output							
I/CLK	I/$\overline{OE}$	I	I	I	I	I	I	I	I	I/O/Q	I/O/Q	I/O/Q	I/O/Q	I/O/Q	I/O/Q	I/O/Q	I/O/Q
X	X	X	X	X	X	X	X	X	X	H	H	H	H	H	H	H	H

X = Don't care state
H = logic high

FIGURE 2. Truth tables (unprogrammed).



Test	R_1	C_L (minimum)
t_{PD}, t_{CO}, f_{CLK}, f_{CLK2}	390Ω	50 pF
t_{EA1}, t_{EA2}	Active high = infinity Active low = 390Ω	50 pF
t_{ER1}, t_{ER2}	Active high = infinity Active low = 390Ω	5.0 pF

NOTE: C_L = load capacitance and includes jig and probe capacitance.

FIGURE 3. Output load circuit.

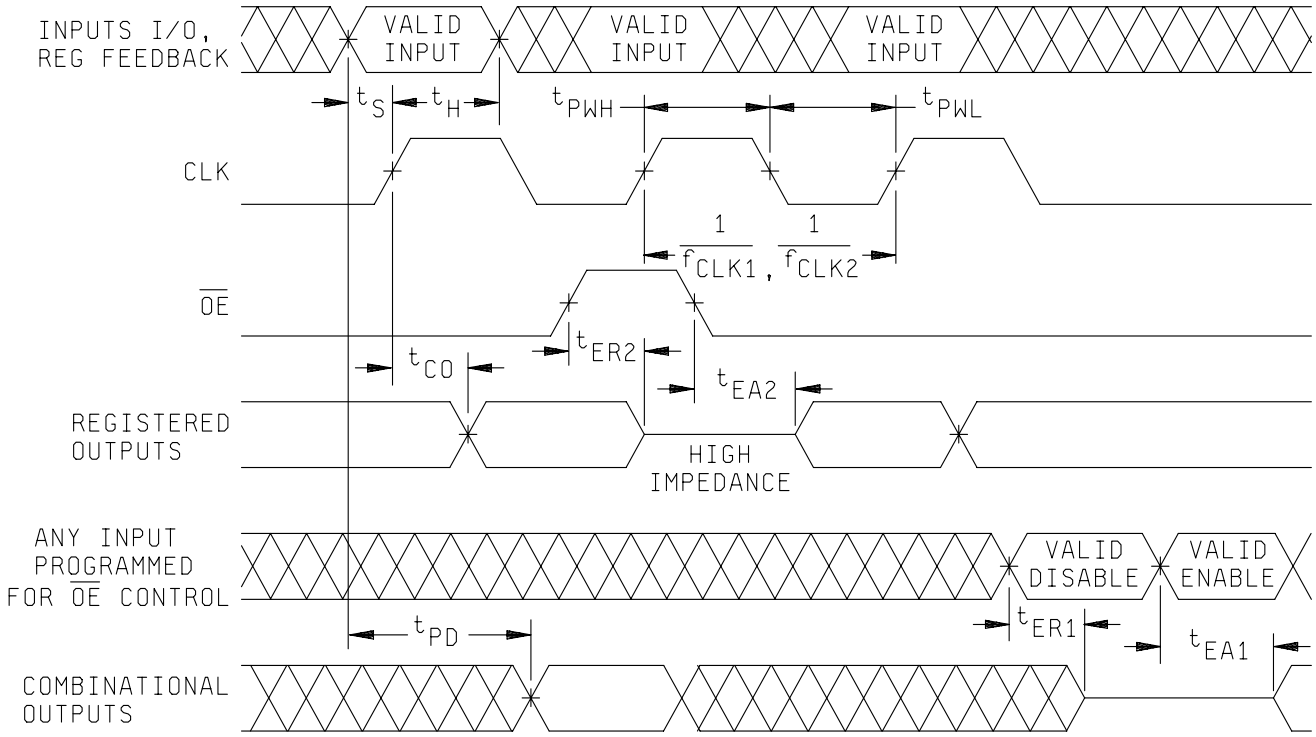


FIGURE 4. Switching waveforms.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8A, 8B 9, 10,11
Group A test requirements (method 5005)	1,2,3,4**,7,8A,8B, 9, 10,11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8A, 8B

* indicates PDA applies to subgroups 1 and 7.

** see 4.3.1c.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table (unprogrammed devices). The truth table for unprogrammed devices shall be as specified on figure 2.

3.2.4 Programmed devices. The requirements for supplying programmed devices are not a part of this drawing.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Endurance A reprogrammability test shall be completed as part of the vendor's reliability process. This reprogrammability test shall be done for initial characterization and after any design or process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but shall guarantee the number of program/erase endurance cycles listed in section 1.3 herein. The vendor's procedure shall be under document control and shall be made available upon request.

3.11 Retention A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process changes which may affect data retention. The methods and procedures may be vendor specific, but shall guarantee the number of years listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with the test data.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Devices shall be burned-in containing a pattern that assures all inputs and I/O's are dynamically switched. This pattern must have all cells programmed in a high or low state (not neutralized).

(4) The burn-in pattern shall be read before and after burn-in. Devices having any logic array bits not in the proper state shall constitute a device failure and shall be added as failures for PDA calculation.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and $C_{I/O/Q}$ measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is fifteen devices with no failures and all input and output terminals tested.

d. I_{OS} measurements in subgroup 1 shall be measured only for the initial test and after process or design changes which may affect I_{OS}. Sample size is 15 devices with no failures, and all output terminals tested.

e. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) TA = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

(4) All devices shall be programmed with a pattern that assures all inputs and I/O's are dynamically switched.

4.4 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available to the user on request.

4.5 Erasing procedures. The erasing procedures shall be as specified by the device manufacturer and shall be made available to the user on request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 07-04-24

Approved sources of supply for SMD 5962-89839 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8983901RA	3/	PALCE16V8H-25E4/BRA
	66675	GAL16V8D-30LD/883C
5962-89839012A	3/	PALCE16V8H-25E4/B2A
	3/	GAL16V8A-30LR/883C
5962-8983902RA	3/	GAL16V8L20J/883
	3/	PALCE16V8H-20E4/BRA
	66675	GAL16V8D-20LD/883C
5962-89839022A	3/	PALCE16V8H-20E4/B2A
	66675	GAL16V8A-20LR/883C
5962-8983902SA	3/	GAL16V8L20W/883
5962-8983903RA	3/	GAL16V8L15J/883
	3/	PALCE16V8H-15E4/BRA
	66675	GAL16V8D-15LD/883C
5962-89839032A	3/	PALCE16V8H-15E4/B2A
	66675	GAL16V8D-15LR/883C
5962-8983903SA	3/	GAL16V8L15W/883
5962-8983904RA	66675	GAL16V8D-10LD/883C
	3/	ATF16V8-10GM/883
	0C7V7	PALCE16V8-10DMB
5962-89839042A	66675	GAL16V8D-10LR/883C
	3/	ATF16V8B-10NM/883
	0C7V7	PALCE16V8-10LMB
5962-8983905RA	3/	GAL16V8A-25QD/883C
5962-89839052A	3/	GAL16V8A-25QR/883C
5962-8983906RA	3/	GAL16V8A-20QD/883C
5962-89839062A	3/	GAL16V8A-20QR/883C
5962-8983907RA	66675	GAL16V8D-7LD/883
5962-89839072A	66675	GAL16V8D-7LR/883
5962-8983908RA	0C7V7	PALCE16V8L-25DMB
5962-89839082A	0C7V7	PALCE16V8L-25LMB
5962-8983909RA	0C7V7	PALCE16V8-15DMB
5962-89839092A	0C7V7	PALCE16V8-15LMB
5962-8983910RA	0C7V7	PALCE16V8L-15DMB
5962-89839102A	0C7V7	PALCE16V8L-15LMB

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8983911RA	0C7V7	PALCE16V8-10DMB
5962-89839112A	0C7V7	PALCE16V8-10LMB
5962-8983912RA	0C7V7	PALCE16V8L-25DMB
5962-89839122A	0C7V7	PALCE16V8L-25LMB
5962-8983913RA	0C7V7	PALCE16V8-15DMB
5962-89839132A	0C7V7	PALCE16V8-15LMB
5962-8983914RA	0C7V7	PALCE16V8L-15DMB
5962-89839142A	0C7V7	PALCE16V8L-15LMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution: Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source.

Vendor CAGE number	Vendor name and address
66675	Lattice Semiconductor Corporation 5555 NE Moore Court Hillsboro, OR 97124-6421
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051