REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R204-95. jb	95-10-30	Michael A. Frye
B	Changes in accordance with NOR 5962-R051-98. ksr	98-03-06	Raymond Monnin
C	Changes in accordance with NOR 5962-R137-98. glg	98-07-20	Raymond Monnin
D	Boilerplate update and part of five year review. tcr	07-05-03	Robert M. Heber

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV	D	D	D	D	D	D														
SHEET	35	36	37	38	39	40														
REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Kenneth Rice

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Kenneth Rice

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
92-03-05

MICROCIRCUIT, MEMORY, DIGITAL,
CMOS 4M X 1 DYNAMIC RANDOM ACCESS MEMORY
(DRAM) MONOLITHIC SILICON

REVISION LEVEL	SIZE	CAGE CODE	
D	A	**67268**	**5962-90622**

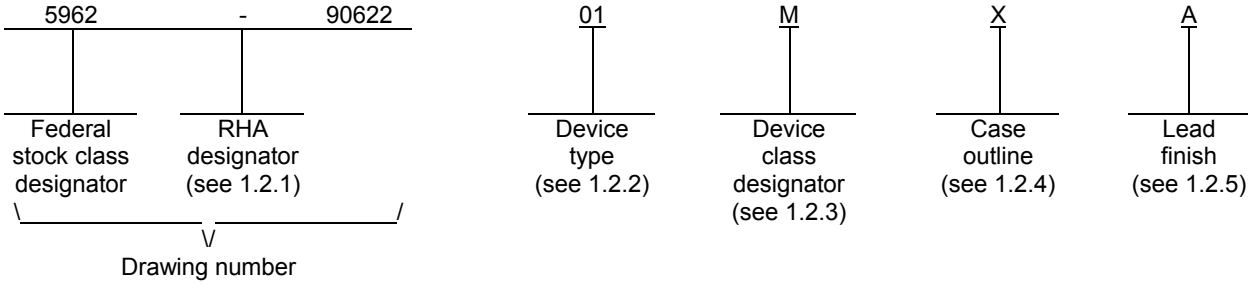
SHEET 1 OF 40

DSCC FORM 2233
APR 97

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01		4M x 1 Dynamic random access memory	120 ns
02		4M x 1 Dynamic random access memory	100 ns
03		4M x 1 Dynamic random access memory	80 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Case outline
X	See figure 1, (20-lead, 0.710" x 0.497" x 0.100"), flat package (top brazed)
Y	See figure 1, (26/20-terminal, .710" x .407" x .092"), rectangular chip carrier package
Z	See figure 1, (26/20-terminal, .685" x .370" x .160"), rectangular chip carrier J-leaded package
U	See figure 1, (26/20-terminal, .685" x .357" x .080"), rectangular chip carrier package
T	See figure 1, (18-lead, .910" x .410" x .140"), dual in-line package
N	See figure 1, (20-lead, 1.050" x .395" x .105"), zig-zag in-line package
V	D-6 (18-lead, .960" x .310" x .200"), dual-in-line package
M	See figure 1, (20-lead, .708" x .415" x .117"), flat package (bottom brazed)

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ Generic numbers are listed on the Standardized Military Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL- HDBK -103 (see 6.6.2 herein).

1.3 Absolute maximum ratings. 2/

Voltage range on any pin	-1.0 V dc to 7.0 V dc
Voltage range on V_{CC}	-1.0 V dc to 7.0 V dc
Short circuit output current	50 mA
Maximum power dissipation (P_D)	1 W
Storage temperature range	-65°C to +150°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case outline V	See MIL-STD-1835
Case outlines X, Y, Z, U, T, N, and M	20°C/W 3/
Junction temperature (T_J) 4/	+175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) 5/	+4.5 V dc to +5.5 V dc
High level input voltage range (V_{IH})	2.4 V dc minimum to 6.5 V dc maximum
Low level input voltage range (V_{IL}) 6/	-1.0 V dc minimum to 0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3/ When a thermal resistance for this case is specified in MIL-STD-1835, that value shall supersede the value indicated herein.

4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

5/ All voltage values in this drawing are with respect to V_{SS}.

6/ The algebraic convention, where the more negative (less positive) limit is designated as a minimum, is used in this drawing for logic voltage levels only.

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) induced by Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to: ASTM International, PO Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959; http://www.astm.org.)

ELECTRONICS INDUSTRIES ALLIANCE (EIA)

JEDEC Standard EIA/JESD 78 - IC Latch-Up Test.

(Applications for copies should be addressed to the Electronics Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201; http://www.jedec.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Functional tests. Various functional tests used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device class M, alternate test patterns shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request. For device classes Q and V alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.2.5 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection only. Each coated microcircuit inspection lot (see inspection lot as defined in MIL-PRF-38535) shall be subjected to and pass the internal moisture content test at 5000 ppm (see method 1018 of MIL-STD-883). The frequency of the internal water vapor testing shall not be decreased unless approved by the preparing activity for class M. The TRB will ascertain the requirements as provided by MIL-PRF-38535 for classes Q and V. Samples may be pulled any time after seal.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 41 (see MIL-PRF-38535, appendix A).

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(1) Dynamic burn-in (method 1015 of MIL-STD-883, test condition D) using the circuit submitted (see 4.2b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard EIA/JESD 78 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply to group C inspection and shall consist of tests specified in table IIB herein.

4.4.2.1 Additional criteria for device class M.

a. Steady-state life test conditions, method 1005 of MIL-STD-883:

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -5 mA, V_{IL} = .8 V, V_{IH} = 2.4 V	1,2,3	All	2.4		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 4.2 mA, V_{IL} = .8 V, V_{IH} = 2.4 V	1,2,3	All		0.4	V
Input leakage current	I_I	V_I = 0 V to 6.5 V, V_{CC} = 5.5 V, All other pins = 0 V to V_{CC}	1,2,3	All		±10	µA
Output leakage current	I_O	V_{CC} = 5.5 V, $\overline{CAS}$ high, V_O = V_{CC} to 0 V	1,2,3	All		±10	µA
Power supply current read or write cycle	I_{CC1}	Minimum cycle, V_{CC} = 5.5 V Measured for a maximum of One address transition while $\overline{RAS}$ = V_{IL}	1,2,3	01		70	mA
				02		80	
				03		85	
Power supply current standby	I_{CC2}	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V	1,2,3	All		4	mA
Power supply current average refresh ($\overline{RAS}$ –only or CBR)	I_{CC3}	V_{CC} = 5.5 V, minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ – only) $\overline{RAS}$ low after $\overline{CAS}$ low (CBR) Measured for a maximum of one address transition while $\overline{RAS}$ = V_{IL}	1,2,3	01		65	mA
				02		75	
				03		85	
Power supply current average page	I_{CC4}	$\overline{RAS}$ low, $\overline{CAS}$ cycling, t_{PC} = minimum, V_{CC} = 5.5 V Measured for a maximum of one address transition while $\overline{CAS}$ = V_{IH}	1,2,3	01		40	mA
				02		50	
				03		60	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input capacitance, address inputs	$C_I(A)$	f = 1 MHz See 4.4.1e Bias on pins under test = 0 V V_{CC} = 5.0 V nominal For $C_I(A)$ the Max capacitance for packages U, T, and N which use HYPER die with On-Chip-Routing (OCR) will be 11 pF Max.	4	All		8	pF
Input capacitance, data inputs	$C_I(D)$		4	All		7	pF
Input capacitance, strobe inputs	$C_I(S)$		4	All		10	pF
Input capacitance, Write-enable inputs	$C_I(W)$		4	All		10	pF
Output capacitance	C_O		4	All		10	pF
Access time from column address	t_{AA}	See figures 4 and 5 1/	9,10,11	01		55	ns
				02		50	
				03		40	
Access time from $\overline{CAS}$ low	t_{CAC}		9,10,11	01		30	ns
				02		25	
				03		20	
Access time from column precharge	t_{CPA}		9,10,11	01		55	ns
				02		50	
				03		45	
Access time from $\overline{RAS}$ low	t_{RAC}		9,10,11	01		120	ns
				02		100	
				03		80	
Output disable time after $\overline{CAS}$ high 2/	t_{OFF}		9,10,11	01		30	ns
				02		25	
				03		20	
Cycle time, random read or write 3/	t_{RC}		9,10,11	01	210		ns
				02	180		
				03	150		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Cycle time, read-write	t_{RWC}	See figures 4 and 5 1/	9,10,11	01	255		ns
				02	220		
				03	205		
Cycle time, page-mode read or write 4/	t_{PC}		9,10,11	01	65		ns
				02	60		
				03	50		
Cycle time, page-mode read or write	t_{PRWC}		9,10,11	01	135		ns
				02	115		
				03	100		
Pulse duration, page-mode, $\overline{RAS}$ low 5/	t_{RASP}		9,10,11	01	120		ns
				02	100		
				03	80		
				All		100	µs
Pulse duration, non-page-mode, $\overline{RAS}$ low 5/	t_{RAS}		9,10,11	01	120		ns
				02	100		
				03	80		
				All		10	µs
Pulse duration, $\overline{CAS}$ low 6/	t_{CAS}		9,10,11	01	30		ns
				02	25		
				03	20		
				All		10	µs
Pulse duration, $\overline{CAS}$ high	t_{CP}		9,10,11	01	15		ns
				02	12		
				03	12		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Pulse duration, $\overline{RAS}$ high (precharge)	t_{RP}	See figures 4 and 5 1/	9,10,11	01	80		ns
				02	70		
				03	60		
Pulse duration, write	t_{WP}		9,10,11	01	25		ns
				02	20		
				03	15		
Setup time, column-address before $\overline{CAS}$ low	t_{ASC}		9,10,11	All	0		ns
Setup time, row-address before $\overline{RAS}$ low	t_{ASR}		9,10,11	All	0		ns
Setup time, data 7/	t_{DS}		9,10,11	All	0		ns
Setup time, read before $\overline{CAS}$ low	t_{RCS}		9,10,11	All	0		ns
Setup time, $\overline{W}$ low before $\overline{CAS}$ high	t_{CWL}		9,10,11	01	30		ns
				02	25		
				03	20		
Setup time, $\overline{W}$ low before $\overline{RAS}$ high	t_{RWL}		9,10,11	01	30		ns
				02	25		
				03	20		
Setup time, $\overline{W}$ low before $\overline{CAS}$ low (Early write operation only)	t_{WCS}		9,10,11	All	0		ns
Setup time, $\overline{W}$ high ($\overline{CAS}$ before $\overline{RAS}$ Refresh only)	t_{WSR}		9,10,11	All	10		ns
Hold time, column-address after $\overline{CAS}$ low	t_{CAH}		9,10,11	01	20		ns
				02	20		
				03	15		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Hold time, data 7/	t_{DH}	See figures 4 and 5 1/	9,10,11	01	25		ns
				02	20		
				03	15		
Hold time, data after $\overline{RAS}$ low	t_{DHR}		9,10,11	01	90		ns
				02	75		
				03	60		
Hold time, column address after $\overline{RAS}$ low 8/	t_{AR}		9,10,11	01	90		ns
				02	75		
				03	60		
Hold time, row-address after $\overline{RAS}$ low	t_{RAH}		9,10,11	01	15		ns
				02	15		
				03	10		
Hold time, read after $\overline{CAS}$ high 9/	t_{RCH}		9,10,11	All	0		ns
Hold time, read after $\overline{RAS}$ high 9/	t_{RRH}		9,10,11	All	0		ns
Hold time, write after $\overline{CAS}$ low (Early write operation only)	t_{WCH}		9,10,11	01	25		ns
				02	20		
				03	15		
Hold time, write after $\overline{RAS}$ low 6/	t_{WCR}		9,10,11	01	90		ns
				02	75		
				03	60		
Hold time, $\overline{W}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	t_{WHR}		9,10,11	All	10		ns
Delay time, column address to $\overline{W}$ low (Read – write operation only)	t_{AWD}		9,10,11	01	60		ns
				02	50		
				03	40		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	See figures 4 and 5 1/	9,10,11	01	10		ns
				02,03	5		
Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$ - before- $\overline{RAS}$ refresh only)	t_{CHR}		9,10,11	01	25		ns
				02	20		
				03	20		
Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}		9,10,11	01	120		ns
				02	100		
				03	80		
Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$ - before- $\overline{RAS}$ refresh only)	t_{CSR}		9,10,11	All	10		ns
Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Read-write operation only)	t_{CWD}		9,10,11	01	30		ns
				02	25		
				03	20		
Delay time, $\overline{RAS}$ low to column-address 10/	t_{RAD}		9,10,11	01	20	65	ns
				02	20	50	
				03	15	40	
Delay time, column-address to $\overline{RAS}$ high	t_{RAL}		9,10,11	01	55		ns
				02	50		
				03	40		
Delay time, column-address to $\overline{CAS}$ high	t_{CAL}		9,10,11	01	55		ns
				02	50		
				03	40		
Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low 10/	t_{RCD}		9,10,11	01	25	90	ns
				02	25	75	
				03	20	60	
Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}		9,10,11	01	30		ns
				02	25		
				03	20		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	t_{RPC}	See figures 4 and 5 1/	9,10,11	All	0		ns
Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Read-write operation only)	t_{RWD}		9,10,11	01	120		ns
				02	100		
				03	80		
$\overline{CAS}$ to output in low Z	t_{CLZ}		9,10,11	All		See 11/	ns
Refresh time interval	t_{REF}		9,10,11	All		16	ms

1/ Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ are to be a minimum of 3 ns and a maximum of 50 ns.

2/ t_{OFF} is specified when the output is no longer driven. The output is disabled when $\overline{CAS}$ is brought high.

3/ All cycle times assume $t_T = 5$ ns.

4/ To assure t_{PC} minimum, t_{ASC} should be greater than or equal to t_{CP}.

5/ In a read-write cycle, t_{RWD} and t_{RWL} must be observed.

6/ In a read-write cycle, t_{CWD} and t_{CWL} must be observed.

7/ Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.

8/ The minimum value is measured when t_{RCD} is set to t_{RCD} minimum as a reference.

9/ Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

10/ Maximum value specified only to guarantee access time.

11/ Valid data is presented at the output after all access times are satisfied but may go from three-state to an invalid data state prior to the specified access times as the outputs are driven when $\overline{CAS}$ goes low.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/

Line No.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, method 5005, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1,7,9 or 2,8A,10	1,7,9 or 2,8A,10
2	Static burn-in I and II (method 1015)	Not required	Not required	Required
3	Same as line 1			1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*,7* Δ
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10,11	1*,2,3,7*, 8A,8B,9,10,11	1*,2,3,7*, 8A,8B,9,10,11
7	Group A test requirements	1,2,3,4**,5,6,7, 8A,8B,9,10,11	1,2,3,4**,5,6,7, 8A,8B,9,10,11	1,2,3,4**,5,6,7, 8A,8B,9,10,11
8	Group C end-point electrical parameters	2,3,7, 8A,8B	1,2,3,7, 8A,8B Δ	1,2,3,7, 8A,8B,9,10,11 Δ
9	Group D end-point electrical parameters	2,3,8A,8B	2,3,8A,8B	2,3,8A,8B
10	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

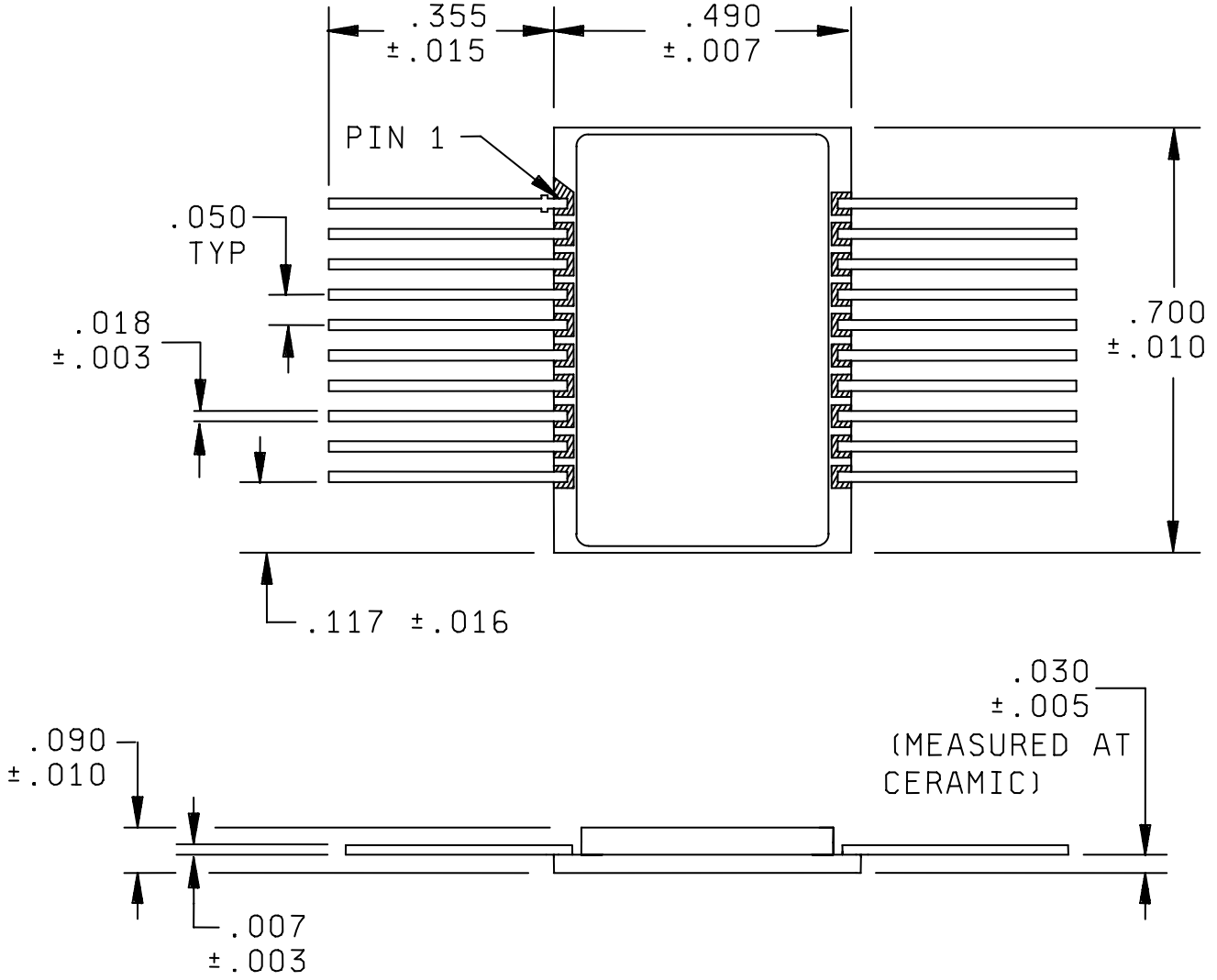
1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous electrical parameters (see table IIB).

TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_{CC2} standby	±10% of specified value in table I
I_I , I_O	±10% of specified value in table I

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

Case X

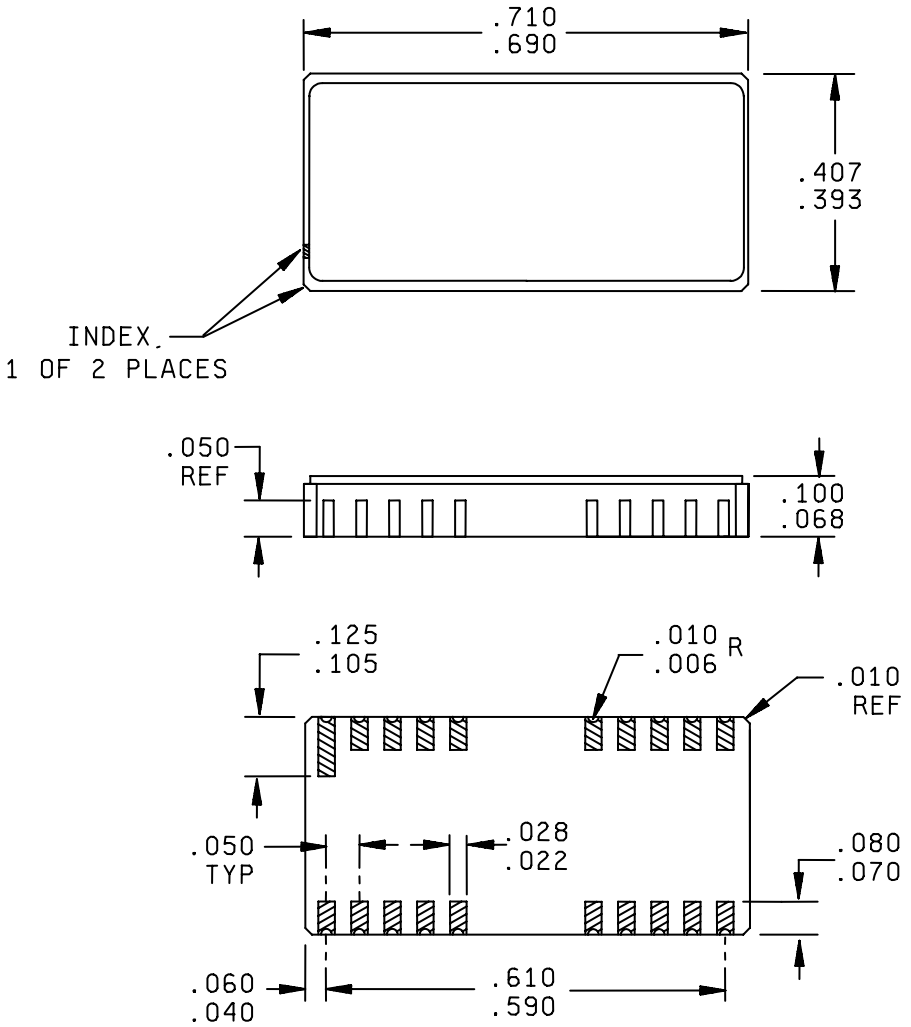


Inches	mm	Inches	mm
.003	.08	.030	0.76
.005	.13	.050	1.27
.007	.18	.090	2.29
.010	.25	.117	2.97
.015	.38	.355	9.02
.016	.41	.490	12.45
.018	.46	.700	17.78

20 Pin flat pack

FIGURE 1. Case outlines.

Case Y

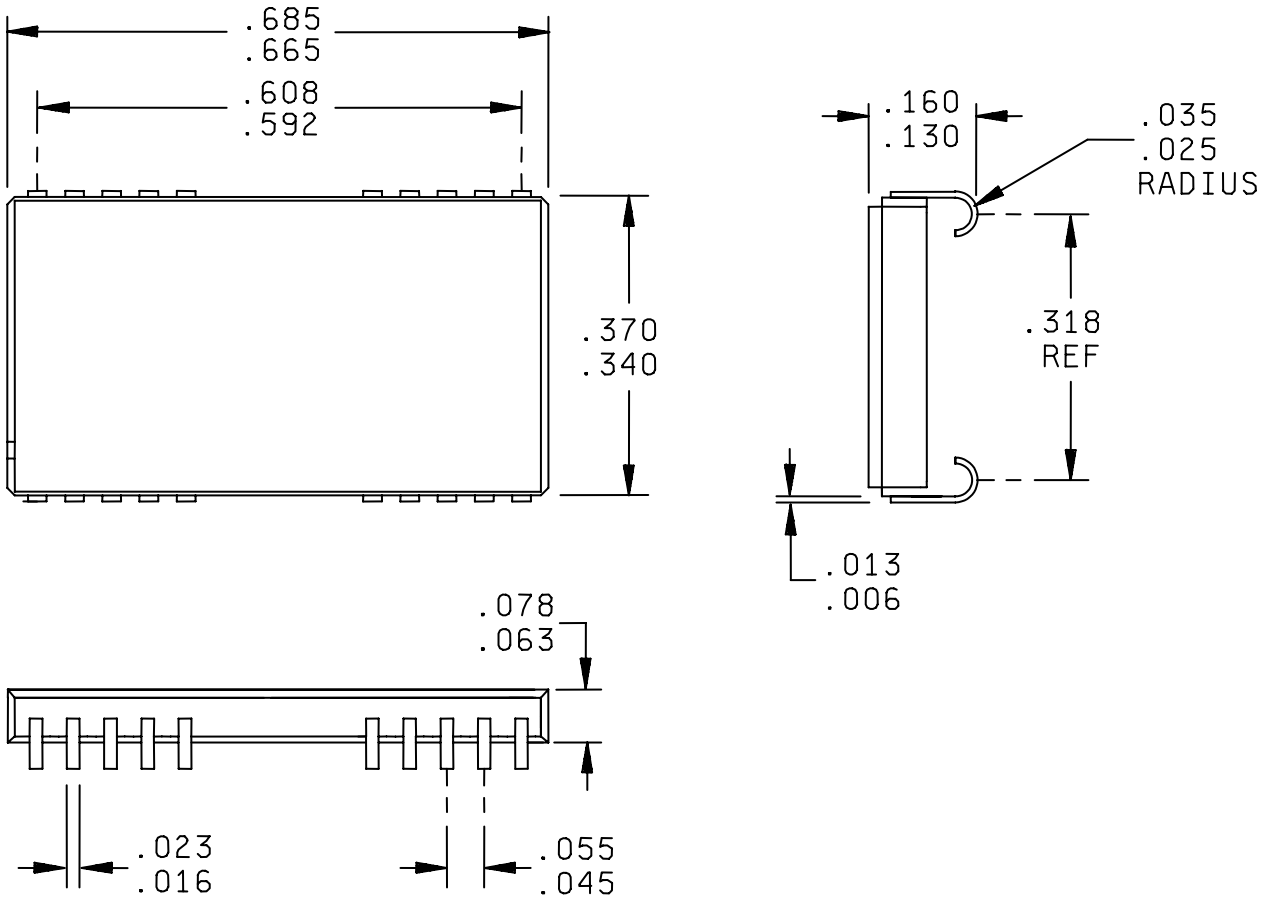


Inches	mm	Inches	mm
.006	0.15	.080	2.03
.010	0.25	.100	2.54
.022	0.56	.105	2.68
.028	0.71	.125	3.18
.040	1.02	.393	9.98
.050	1.27	.407	10.34
.060`	1.52	.590	14.98
.068	1.72	.610	15.49
.070	1.78	.690	17.52
		.710	18.03

20 Pin, small-outline leadless ceramic chip carrier

FIGURE 1. Case outlines – continued.

Case Z

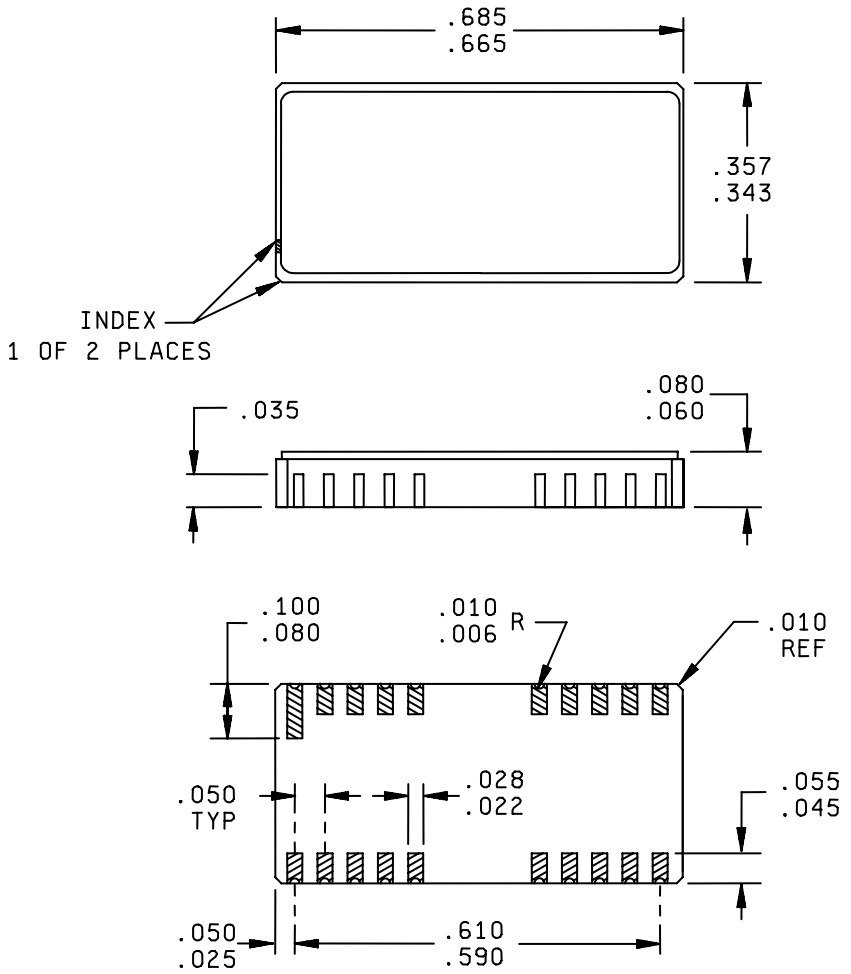


Inches	mm	Inches	mm
.006	0.15	.130	3.30
.013	0.33	.160	4.06
.016	0.41	.318	8.08
.023	0.58	.340	8.64
.025	0.63	.370	9.40
.035	0.89	.592	15.04
.045	1.14	.608	15.44
.055	1.40	.665	16.89
.063	1.60	.685	17.40
.078	1.98		

20/26 Pin, ceramic small-outline, j-leaded chip carrier, 350 mil

FIGURE 1. Case outlines - Continued.

Case U

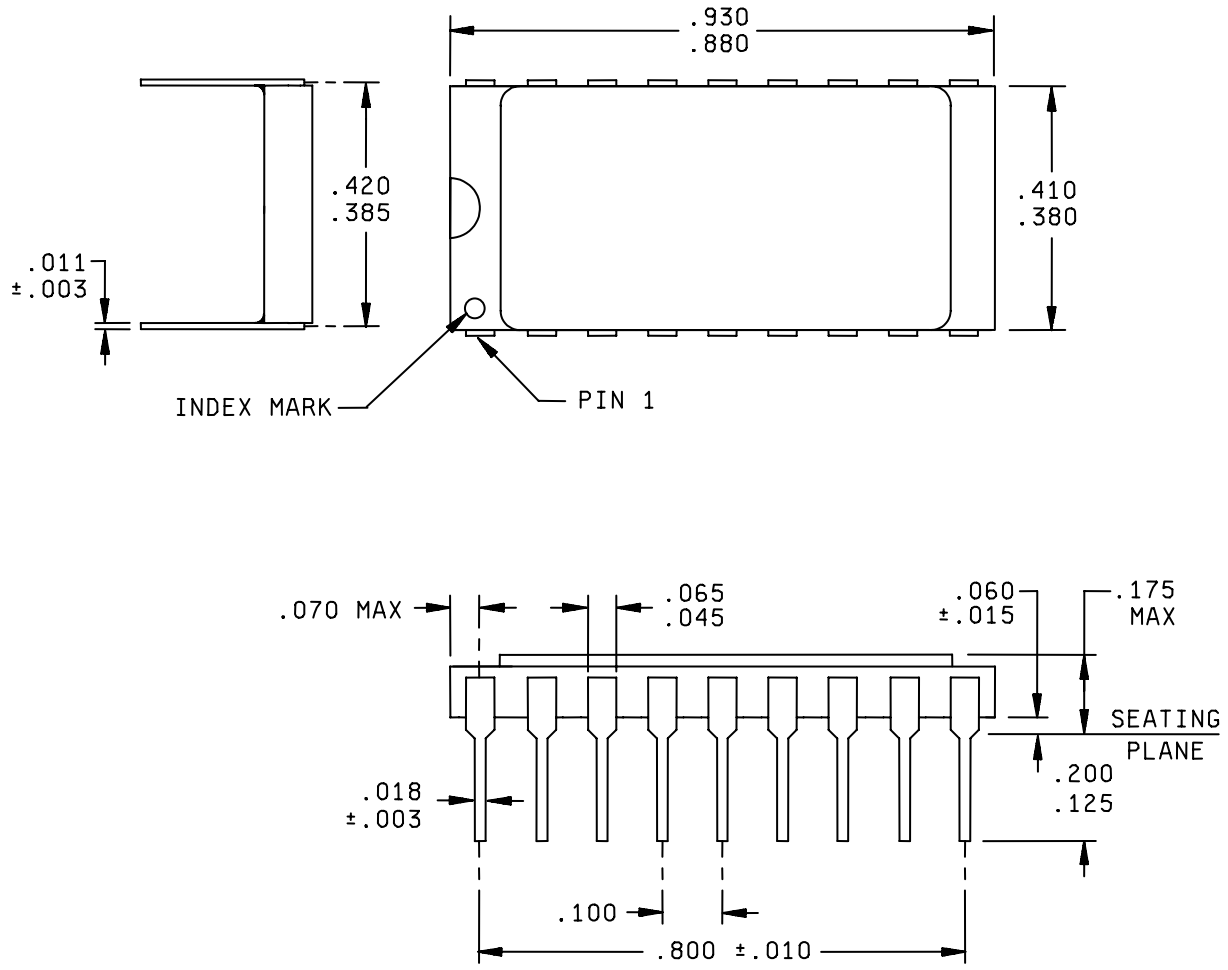


Inches	mm	Inches	mm
.006	0.15	.080	2.03
.010	0.25	.100	2.54
.022	0.56	.343	8.71
.025	0.64	.357	9.06
.028	0.71	.590	14.98
.035	0.89	.610	15.49
.045	1.14	.665	16.89
.050	1.27	.585	17.40
.055	1.40		
.060	1.52		

20-Pin, (350 mil) small-outline, leadless ceramic chip carrier

FIGURE 1. Case outlines - Continued.

Case T

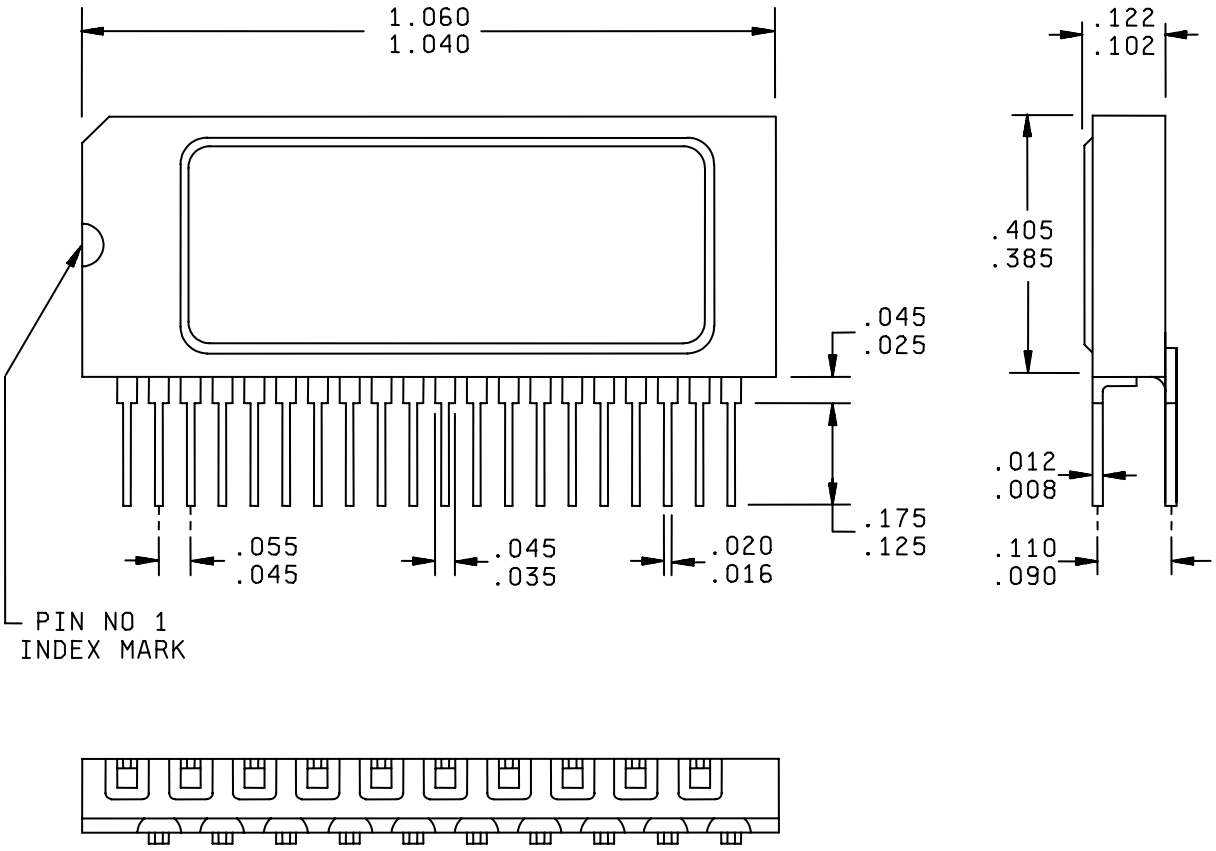


Inches	mm	Inches	mm
.003	0.08	.125	3.18
.010	0.25	.175	4.44
.011	0.28	.200	5.08
.015	0.38	.380	9.65
.018	0.46	.385	9.78
.045	1.14	.410	10.41
.060	1.52	.420	10.68
.065	1.65	.800	20.32
.070	1.78	.880	22.35
.100	2.54	.930	23.62

18-Pin, ceramic side brazed, dual-in-line package

FIGURE 1. Case outlines - Continued.

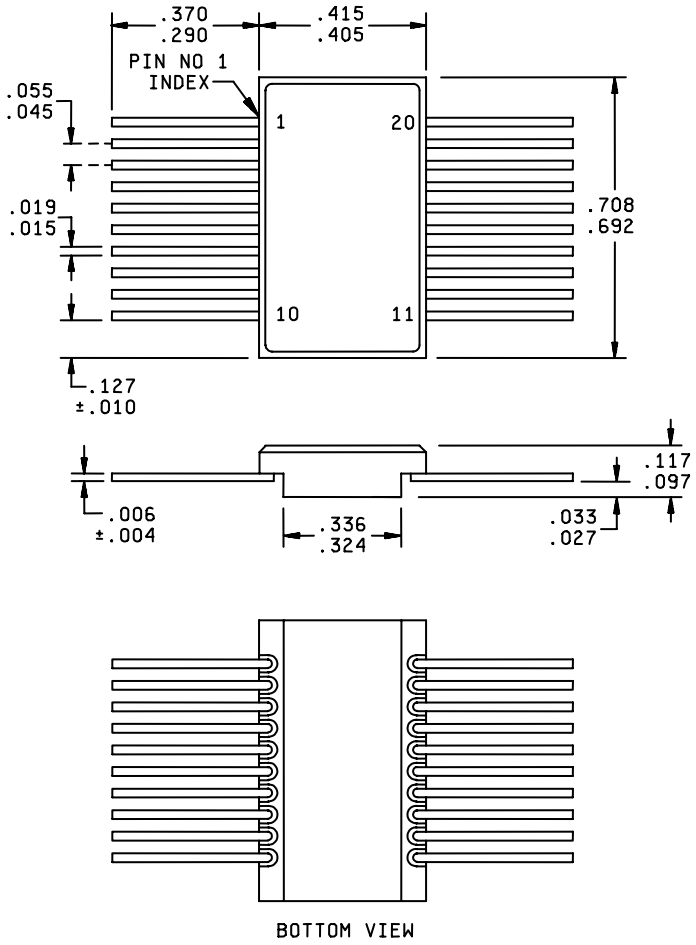
Case N



Inches	mm	Inches	mm
.008	0.20	.102	2.59
.012	0.30	.110	2.79
.016	0.41	.122	3.10
.025	0.64	.125	3.18
.020	0.51	.175	4.45
.035	0.89	.385	9.78
.045	1.14	.405	10.29
.055	1.40	1.040	26.42
.090	2.29	1.060	26.92

FIGURE 1. Case outlines - Continued.

Case M



Inches	mm	Inches	mm
.004	0.10	.127	3.23
.006	0.15	.290	7.37
.010	0.25	.310	7.87
.015	0.38	.324	8.23
.019	0.48	.336	8.53
.027	0.69	.405	10.29
.033	0.84	.415	10.54
.045	1.14	.435	11.05
.055	1.40	.455	11.56
.097	2.46	.692	17.58
.117	2.97	.708	17.98

20 Pin flat pack.

FIGURE 1. Case outlines - Continued.

Device types	01, 02, 03			
Case outlines	T, V	X, M	Y, U, Z	N
Terminal number	Terminal Symbol			
1	D	D	D	A_9
2	$\overline{W}$	$\overline{W}$	$\overline{W}$	$\overline{CAS}$
3	$\overline{RAS}$	$\overline{RAS}$	$\overline{RAS}$	Q
4	A_{10}	NC	NC	V_{SS}
5	A_0	A_{10}	A_{10}	D
6	A_1	A_0	---	$\overline{W}$
7	A_2	A_1	---	$\overline{RAS}$
8	A_3	A_2	---	A_{10}
9	V_{CC}	A_3	A_0	NC
10	A_4	V_{CC}	A_1	NC
11	A_5	A_4	A_2	A_0
12	A_6	A_5	A_3	A_1
13	A_7	A_6	V_{CC}	A_2
14	A_8	A_7	A_4	A_3
15	A_9	A_8	A_5	V_{CC}
16	$\overline{CAS}$	A_9	A_6	A_4
17	Q	NC	A_7	A_5
18	V_{SS}	$\overline{CAS}$	A_8	A_6
19	---	Q	---	A_7
20	---	V_{SS}	---	A_8
21	---	---	---	---
22	---	---	A_9	---
23	---	---	NC	---
24	---	---	$\overline{CAS}$	---
25	---	---	Q	---
26	---	---	V_{SS}	---

Figure 2. Terminal connections.

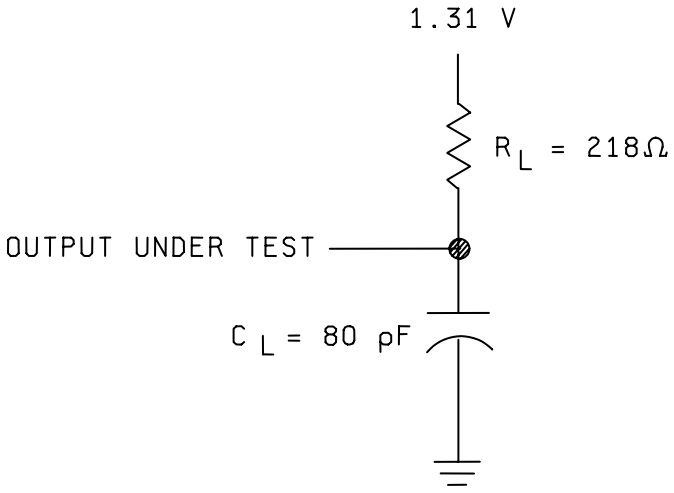
Operation	Inputs					Input	Output
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	Row address	Column address	D	Q
Read	ACT	ACT	NAC	APD	APD	DNC	VLD
Write (early write)	ACT	ACT	ACT	APD	APD	VLD	OPN
Write (late write)	ACT	ACT	ACT	APD	APD	VLD	ILD 1/
Read-modify-write	ACT	ACT	ACT	APD	APD	VLD	VLC
$\overline{RAS}$ – only refresh	ACT	NAC	DNC	APD 2/	DNC	DNC	OPN
Hidden refresh	ACT	ACT	NAC	APD	DNC	DNC	VLD
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	OPN
Standby	NAC	NAC	DNC	DNC	DNC	DNC	OPN

1/ Output may go from high impedance to an invalid data state prior to the specified access time as the output is driven when $\overline{CAS}$ goes low.

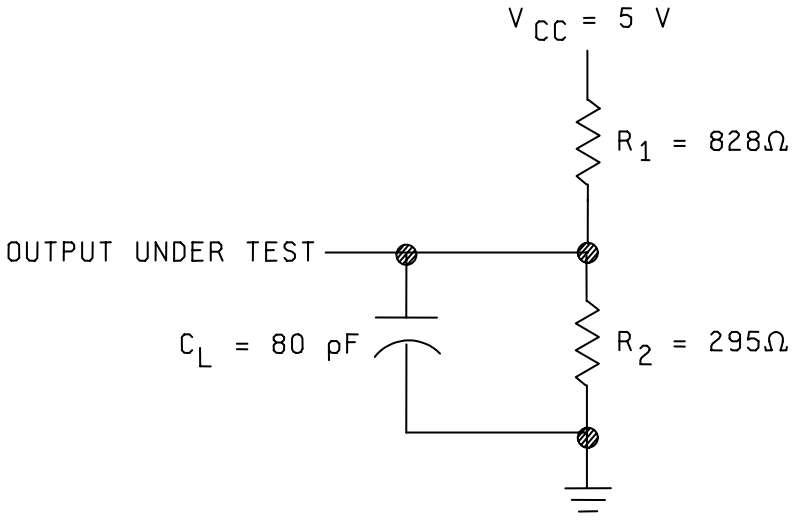
2/ A_{10} is a don't care.

ACT = active
NAC = nonactive
DNC = don't care
VLD = valid
ILD = invalid
APD = applied
OPN = open

FIGURE 3. Truth table.



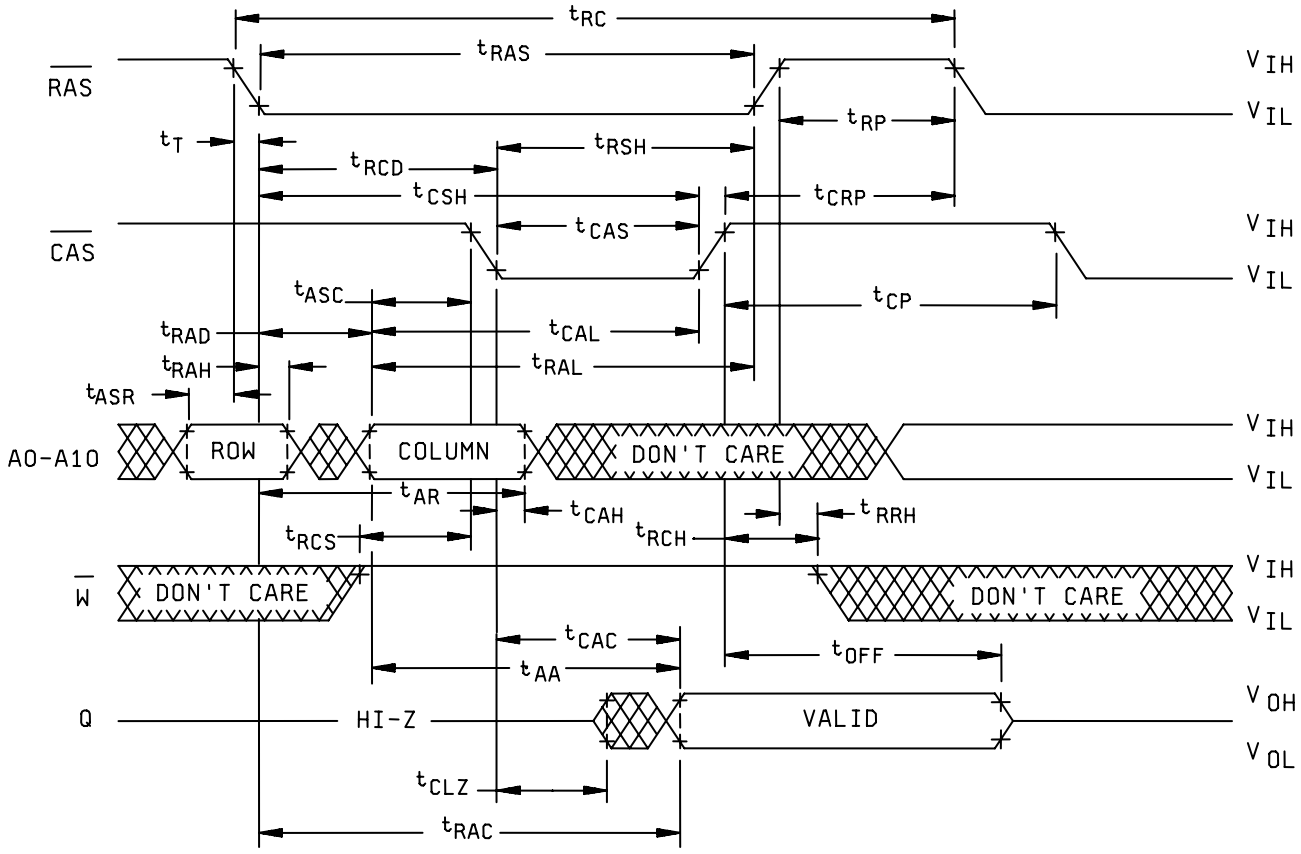
(A) LOAD CIRCUIT



(B) ALTERNATE LOAD CIRCUIT

FIGURE 4. Load circuits.

Read cycle timing



NOTE: Output may go from three-state to an invalid state prior to the specified access time.

FIGURE 5. Timing waveform diagrams.

Early write cycle timing

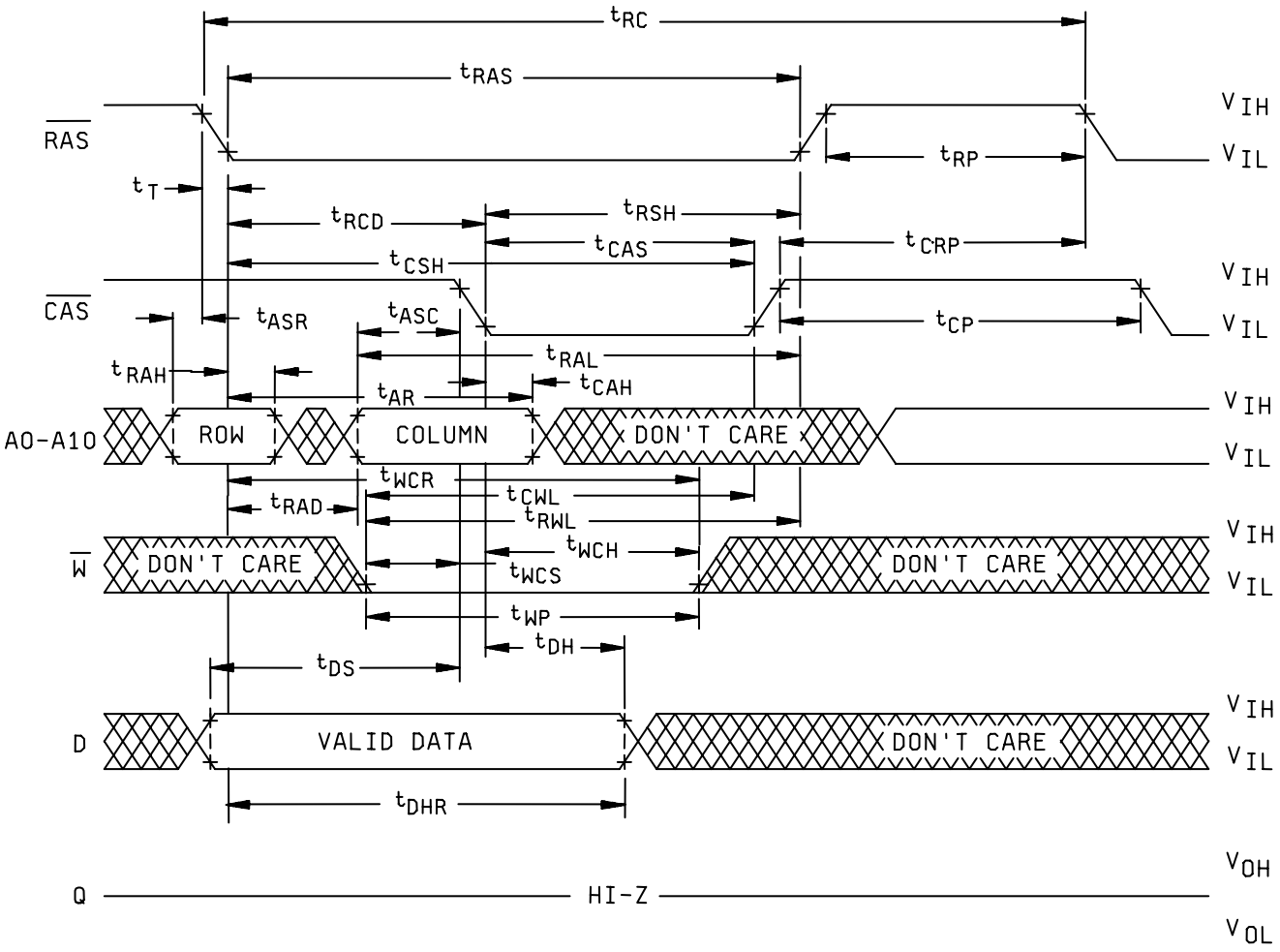


FIGURE 5. Timing wave diagrams - Continued.

Write cycle timing

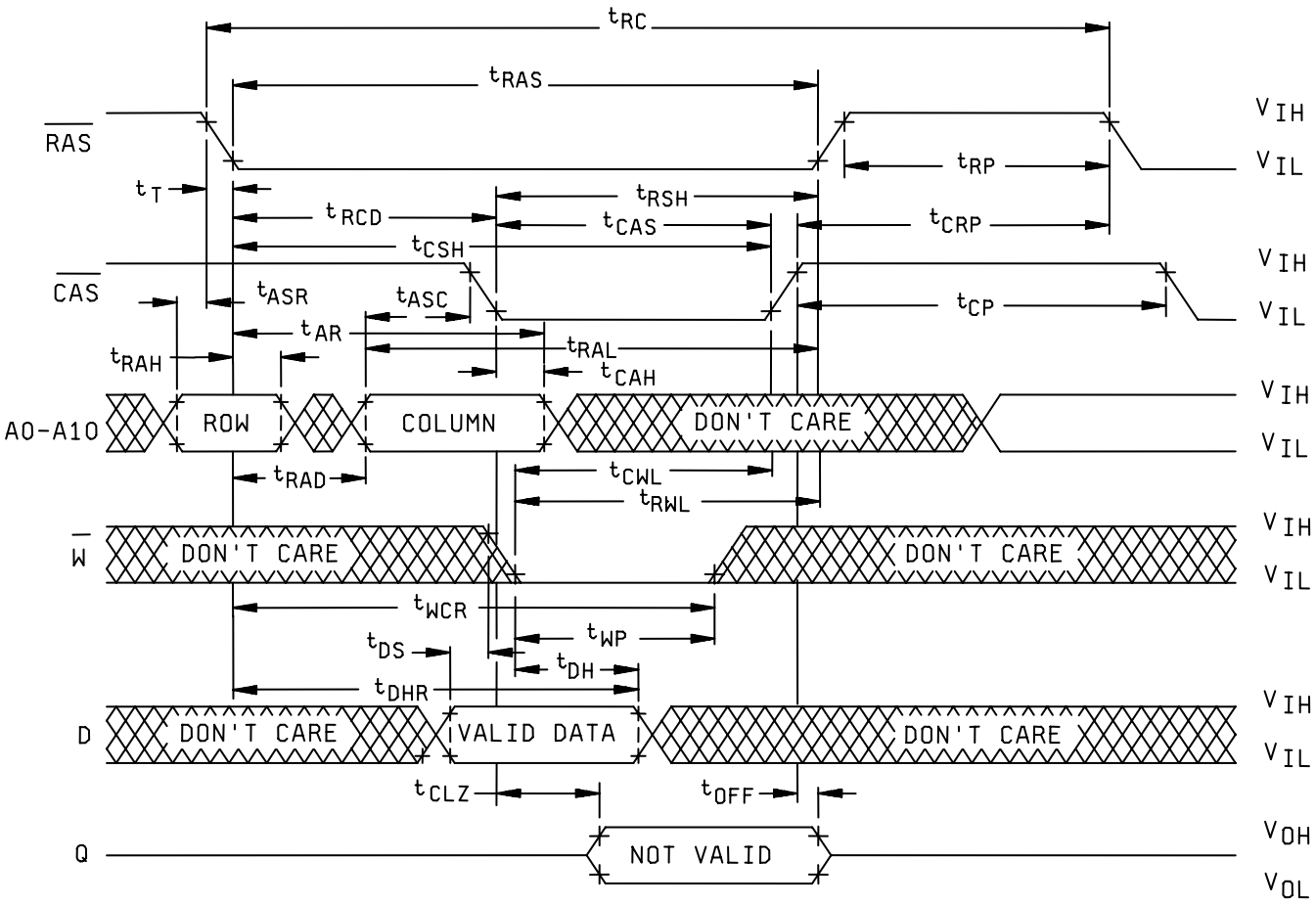
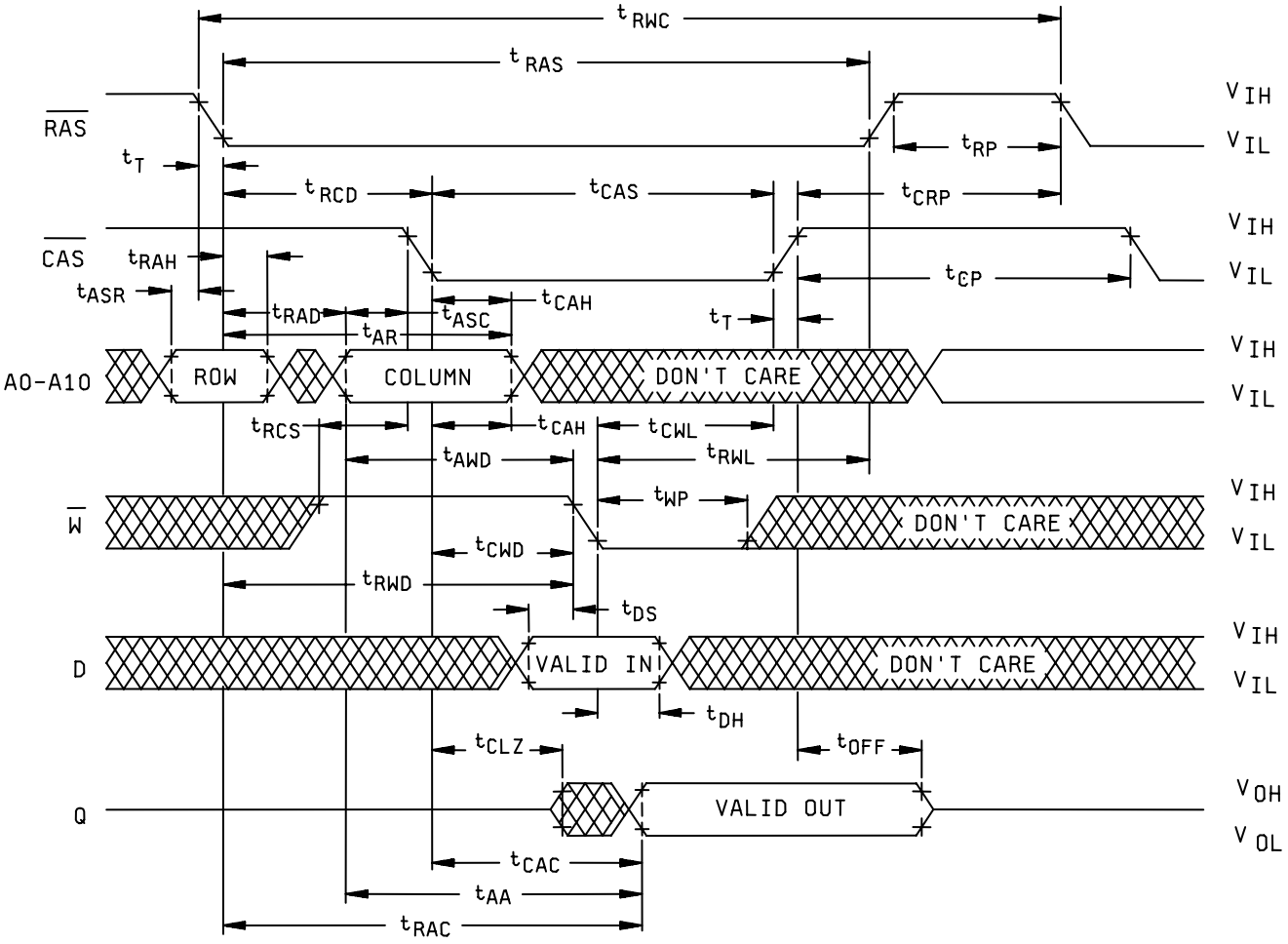


FIGURE 5. Timing wave diagrams - Continued.

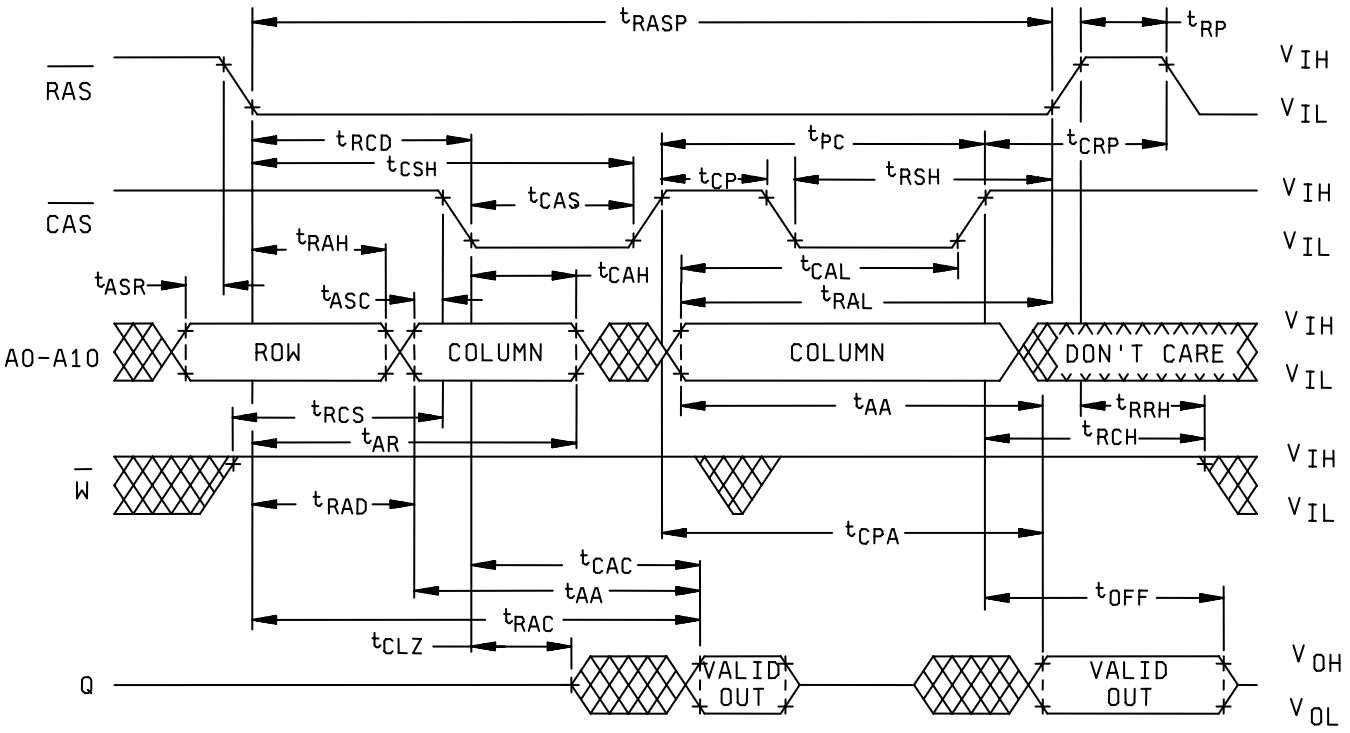
Read-write cycle timing



NOTE: Output may go from three-state to an invalid state prior to the specified access time.

FIGURE 5. Timing wave diagrams - Continued.

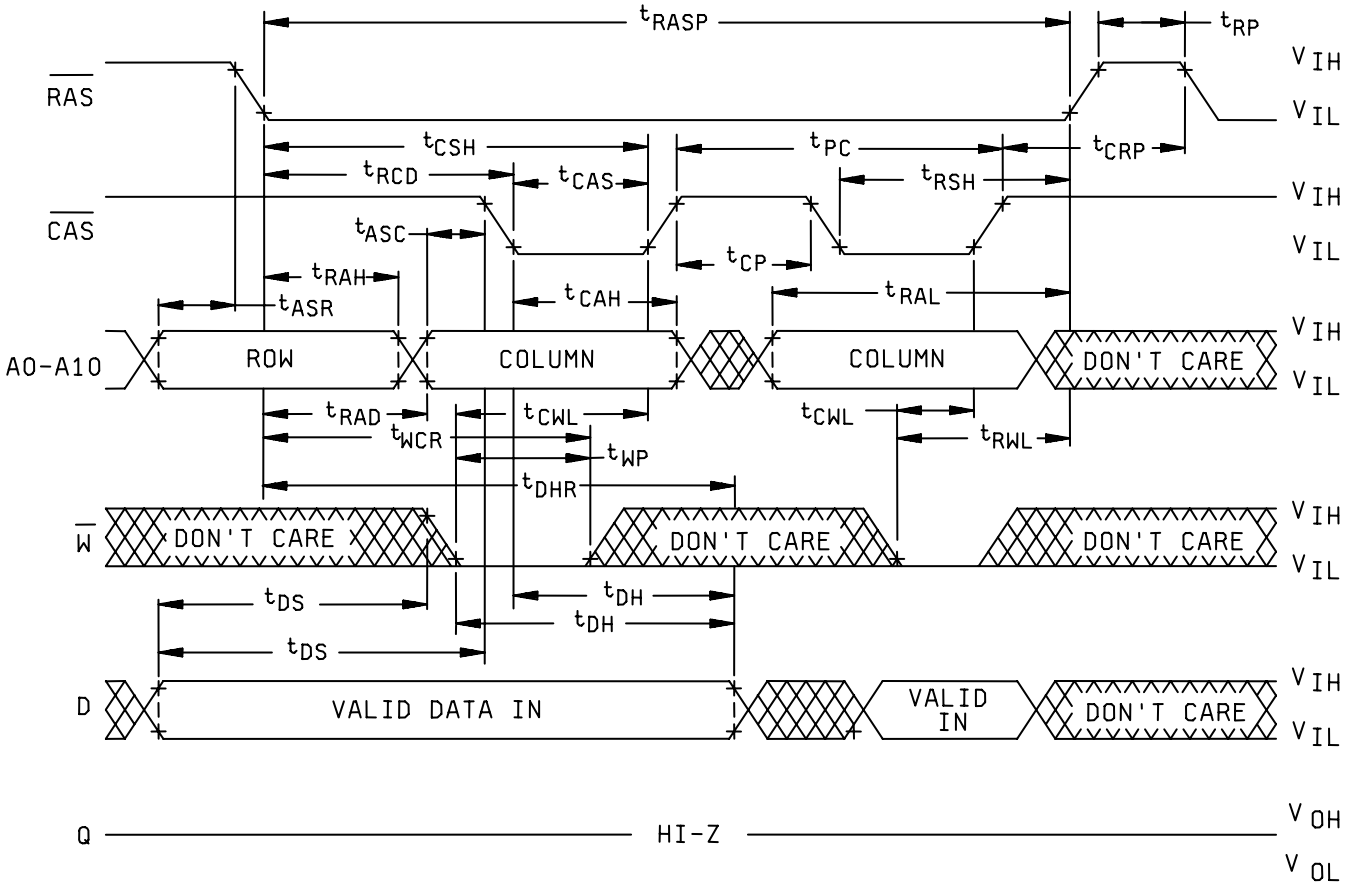
Enhanced page-mode read cycle timing



NOTES:
1. Output may go from three-state to an invalid state prior to the specified access time.
2. Access time is t_{CPA} or t_{AA} dependent.

FIGURE 5. Timing wave diagrams - Continued.

Enhanced page-mode write cycle timing

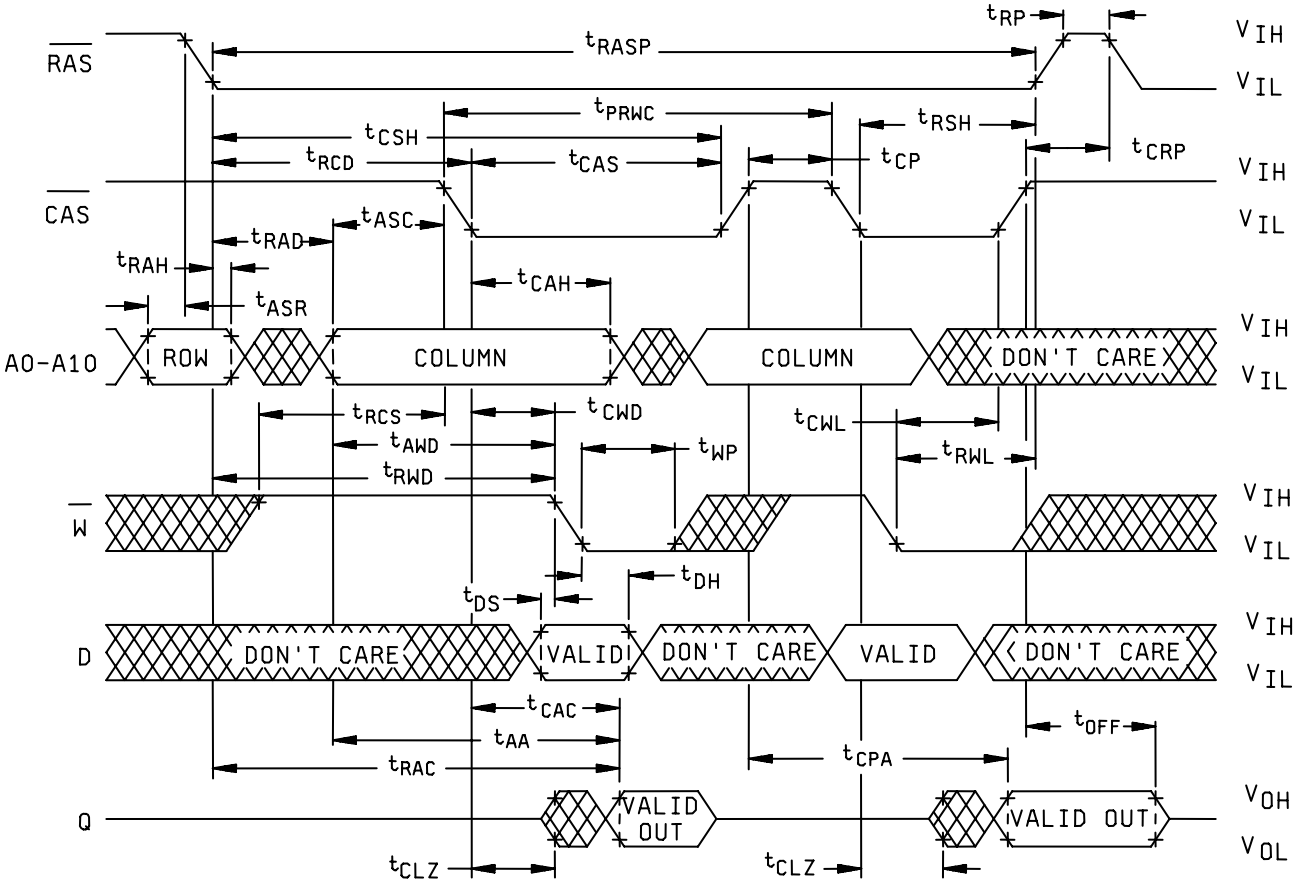


NOTES:

1. t_{DS} and t_{DH} are referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.
2. A read cycle or a read-write cycle can be intermixed with write write cycle as long as the read and read-write timing specification are not violated.

FIGURE 5. Timing wave diagrams - Continued.

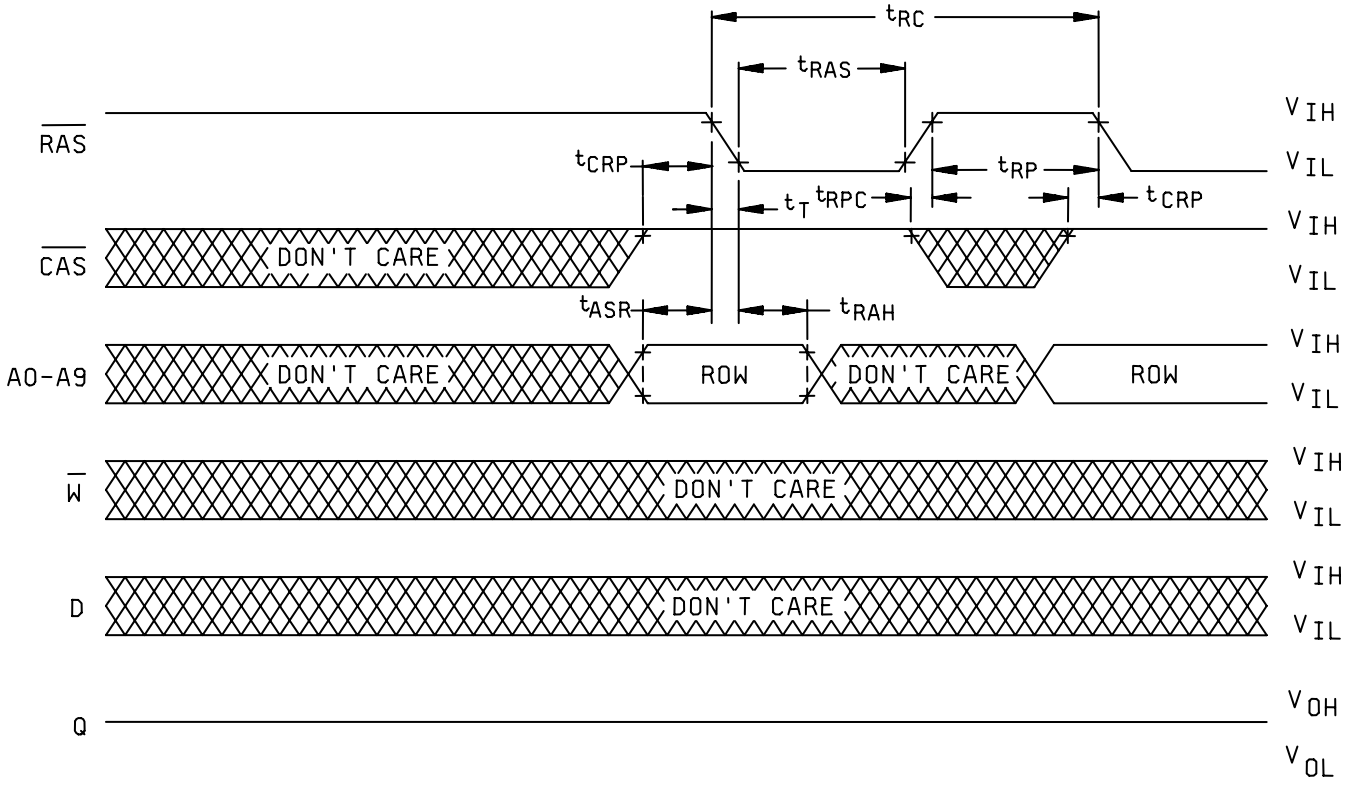
Enhanced page-mode read-write cycle timing



NOTES:
1. Output may go from three-state to an invalid state prior to the specified access time.
2. A read or read-write cycle can be intermixed with read-write cycles as long as the read and write timing specification are not violated.

FIGURE 5. Timing wave diagrams - Continued.

$\overline{RAS}$ - only refresh timing



NOTE: A_{10} is a don't care.

FIGURE 5. Timing wave diagrams - Continued.

Automatic ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$) refresh cycle timing

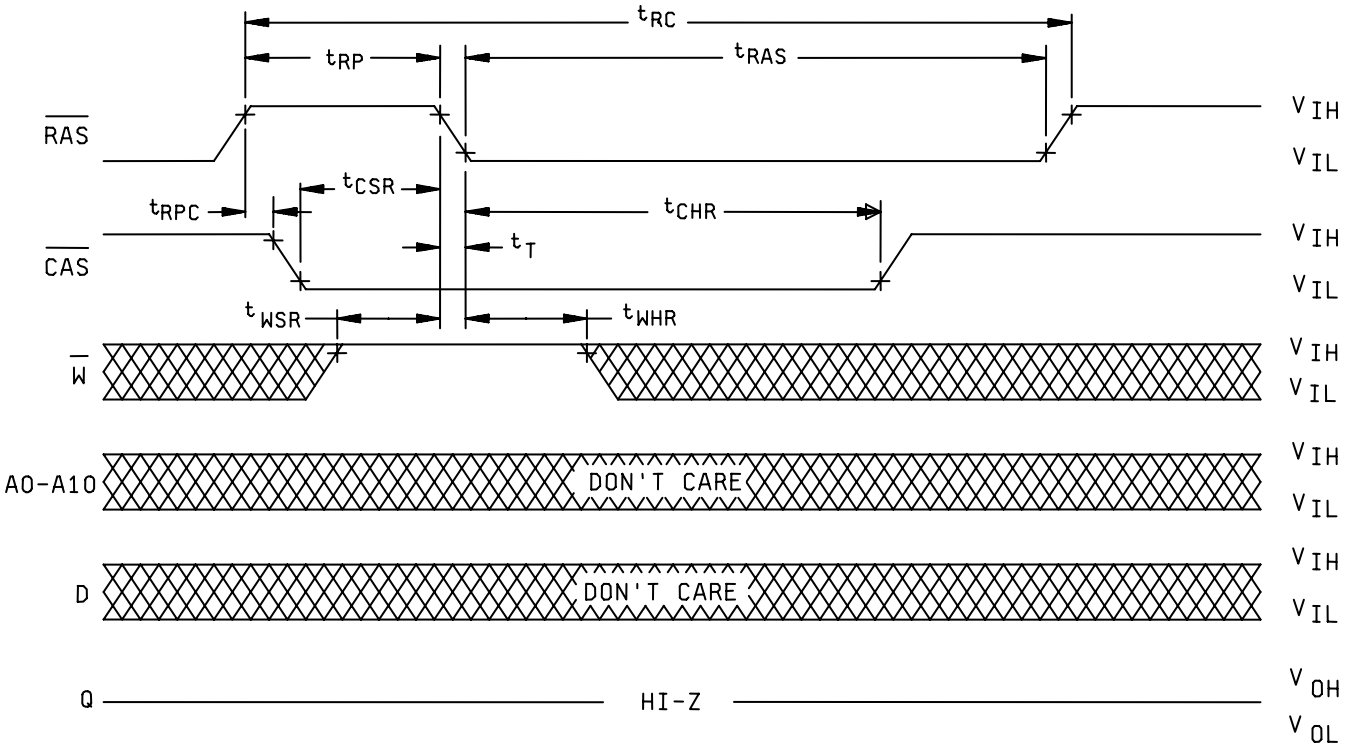


FIGURE 5. Timing wave diagrams - Continued.

Hidden refresh cycle (read)

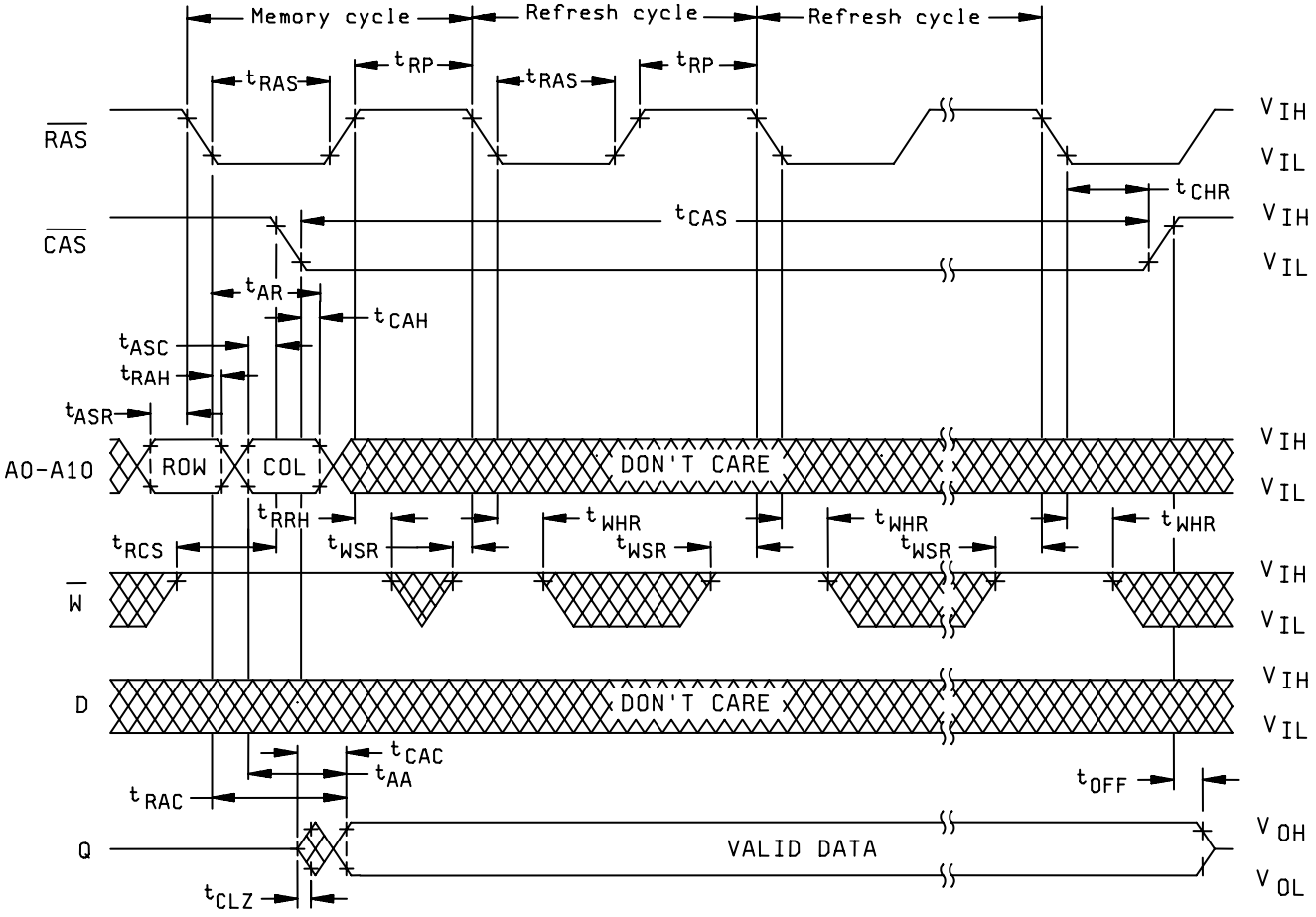


FIGURE 5. Timing wave diagrams - Continued.

Hidden refresh cycle (write)

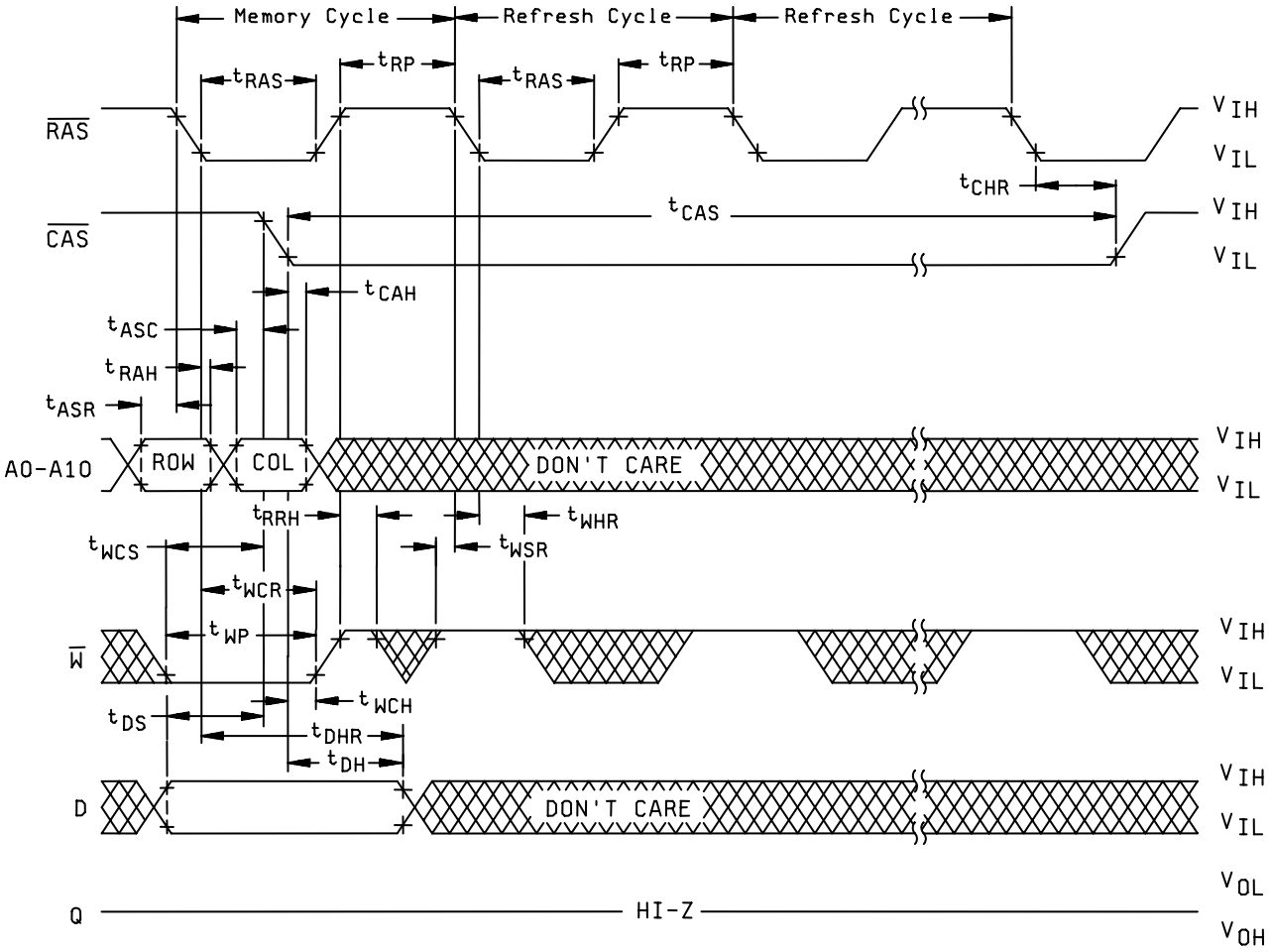


FIGURE 5. Timing wave diagrams - Continued.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after life test perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

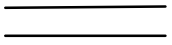
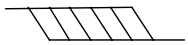
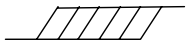
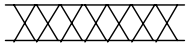
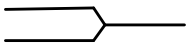
6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331 and herein:

C_{IN} and C_{OUT} ..... Input and bidirectional output, terminal-to-GND capacitance.
GND ..... Ground zero voltage potential.
I_{CC} ..... Supply current.
I_{IL} ..... Input current low.
I_{IH} ..... Input current high.
T_C ..... Case temperature.
T_A ..... Ambient temperature.
V_{CC} ..... Positive supply voltage.
V_{IC} ..... Positive input clamp voltage
O/V ..... Latch-up over-voltage
O/I ..... Latch-up over-current

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

APPENDIX A
FUNCTIONAL ALGORITHMS

A.1 SCOPE

A.1.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

A.2 APPLICABLE DOCUMENTS

This section is not applicable to this appendix.

A.3 ALGORITHMS

A.3.1 Algorithm A (pattern 1).

A.3.1.1 Output high impedance (t_{OFF}). This pattern verifies the output buffer switches to high impedence (three-state) within the specified t_{OFF} after the rise of $\overline{CAS}$. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load address location with data.
Step 3: Raise $\overline{CAS}$ and read address location and guarantee $V_{OL} < V_{OUT} < V_{OH}$ after t_{OFF} delay.

A.3.2 Algorithm B (pattern 2).

A.3.2.1 Vcc Slew. This pattern indicates sense amplifier margin by slewing the supply voltage between memory writing and reading. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load memory with background data with Vcc at 5.0 V.
Step 3: Change Vcc to 5.5 V.
Step 4: Read memory with background data.
Step 5: Load memory with background data complement.
Step 6: Change Vcc to 4.5 V.
Step 7: Read memory with background data complement.

A.3.3 Algorithm C (pattern 3).

A.3.3.1 March data. This pattern tests for address uniqueness and multiple selection. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load memory with background data.
Step 3: Read location 0.
Step 4: Write data complement in location 0.
Step 5: Repeat step 3 and 4 for all other locations in the memory (sequentially).
Step 6: Read data complement in maximum address location.
Step 7: Write data in maximum address location.
Step 8: Repeat step 6 and 7 for all other locations in the memory from maximum to minimum address.
Step 9: Read data in maximum address location.
Step 10: Write data complement in maximum address location.
Step 11: Repeat step 6 and 7 for all other locations in the memory from maximum to minimum address.
Step 12: Read memory with data complement.

A.3.4 Algorithm D (pattern 4).

A.3.4.1 Refresh test (cell retention) +125°C only. This test is used to check the retention time of the memory cells. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load memory with background data.
Step 3: Pause T_{REF} (stop all clocks).
Step 4: Read memory with background data.
Step 5: Repeat steps 2-4 with data complement.

A.3.5 Algorithm E (pattern 5).

A.3.5.1 Read-modify-write (RMW). This pattern verifies the Read-modify-write mode for the memory. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load memory with background data.
Step 3: Read memory with data and load with data complement using RMW cycle.
Step 4: Repeat step 3 for all address locations.
Step 5: Repeat steps 2 and 3 using data complement.

A.3.6 Algorithm F (pattern 6).

A.3.6.1 Page mode. This pattern verifies the Page mode for the memory. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load first page of memory with background data using Page mode cycle.
Step 3: Read first page of memory with data and load with data complement using Page mode cycle.
Step 4: Read first page of memory with data complement and load with data using Page mode cycle.
Step 5: Repeat steps 2-4 for remaining memory locations.

A.3.7 Algorithm G (pattern 7).

A.3.7.1 $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ refresh test. This test is used to verify the functionality of the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ mode of cell refreshing. It is done at +125°C only and is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load memory with background data.
Step 3: Perform 1024 $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ cycles while attempting to modify data.
Step 4: Read memory with background data.

A.3.8 Algorithm H (pattern 8).

A.3.8.1 $\overline{\text{RAS}}$-Only refresh test. This test is used to verify the functionality of the $\overline{\text{RAS}}$-only mode of cell refreshing. It is done at +125°C only and is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load memory with background data.
Step 3: Perform 1024 $\overline{\text{RAS}}$-only cycles while attempting to modify data.
Step 4: Repeat step 3 for 1 second.
Step 5: Read memory with background data.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 07-05-03

Approved sources of supply for SMD 5962-90622 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9062201MXA	3/	SMJ44100-12HR
5962-9062201MYA	0EU86 3/	MT4C1004JEC-12 SMJ44100-12HM
5962-9062201MZA	3/	SMJ44100-12HJ
5962-9062201MUA	0EU86 3/	MT4C1004JECN-12 SMJ44100-12HL
5962-9062201MTA	0EU86 3/	MT4C1004JC-12 SMJ44100-12JD
5962-9062201MVA	0EU86	MT4C1004JCN-12
5962-9062201MMA	0EU86	MT4C1004JF-12
5962-9062201MNA	0EU86	MT4C1004JCZ-12
5962-9062202MXA	3/	SMJ44100-12HR
5962-9062202MYA	0EU86 3/	MT4C1004JEC-10 SMJ44100-12HM
5962-9062202MZA	3/	SMJ44100-12HJ
5962-9062202MUA	0EU86 3/	MT4C1004JECN-10 SMJ44100-10HL
5962-9062202MTA	0EU86 3/	MT4C1004JC-10 SMJ44100-10JD
5962-9062202MVA	0EU86	MT4C1004JCN-10
5962-9062202MMA	0EU86	MT4C1004JF-10
5962-9062202MNA	0EU86	MT4C1004JCZ-10
5962-9062203MXA	3/	SMJ44100-80HR

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9062203MYA	0EU86 3/	MT4C1004JEC-8 SMJ44100-80HM
5962-9062203MZA	3/	SMJ44100-80HJ
5962-9062203MUA	0EU86 3/	MT4C1004JECN-8 SMJ44100-80HL
5962-9062203MTA	0EU86 3/	MT4C1004JC-8 SMJ44100-80JD
5962-9062203MVA	0EU86	MT4C1004JCN-8
5962-9062203MMA	0EU86	MT4C1004JCZ-8
5962-9062203MNA	0EU86	MT4C1004JF-8

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
0EU86	Austin Semiconductor Inc. 8701 Cross Park Dr. STE 105 Austin, TX 78754-4566