| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| A | Added changes in accordance with NOR 5962-R116-94. | 94-03-03 | M. A. Frye |
| B | Added 03 device, removed CAGE number 01295, and made editorial changes throughout. | 96-07-09 | M. A. Frye |
| C | Added changes in accordance with NOR 5962-R059-97. | 96-11-12 | Raymond Monnin |
| D | Added changes in accordance with NOR 5962-R193-97. | 97-03-03 | Raymond Monnin |
| E | Corrected radiation circuit. Updated boilerplate. ksr | 98-03-31 | Raymond Monnin |
| F | Add 04 and 05 devices, change case outlines from CQCC2-F172 to figure 4. Page 3, section 1.3 changed $T_J$ from 175°C to 150°C. Added appendix A for die. Added CQFP package option case U, and binning circuitry delay for 04 and 05 in Table IA. ksr | 98-09-18 | Raymond Monnin |
| G | Change the generic number for the 01 and 02 devices as well as the bin speed. Update the binning circuit delay on table IA. Update the bin speed for the 01 device in section 10.2.2. ksr | 98-11-15 | Raymond Monnin |
| H | Replaced figure 1, case outline Y with new graphic art work. ksr | 00-04-28 | Raymond Monnin |
| J | Boilerplate update, part of 5 year review. ksr | 07-05-28 | Robert M. Heber |
| K | Add device types 06 and 07. Add CAGE Code 1RU44. Updated boilerplate. lhl | 12-04-10 | Charles F. Saffle |

| REV | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SHEET | | | | | | | | | | | | | | | | | | | | |
| REV | K | K | K | K | K | K | K | K | K | K | K | K | K | K | K | K | K | K | K | |
| SHEET | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | |

| REV STATUS | REV | K | K | K | K | K | K | K | K | K | K | K | K | K | K |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OF SHEETS | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |

PMIC N/A

PREPARED BY
Rajesh Pithadia

CHECKED BY
Jeff Bowling

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
93-04-07

REVISION LEVEL
K

**STANDARD MICROCIRCUIT DRAWING**

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

**DLA LAND AND MARITIME**
**COLUMBUS, OHIO 43218-3990**
**http://www.landandmaritime.dla.mil**

# MICROCIRCUIT, MEMORY, DIGITAL, CMOS, FIELD PROGRAMMABLE GATE ARRAY, 8000 GATES, MONOLITHIC SILICON

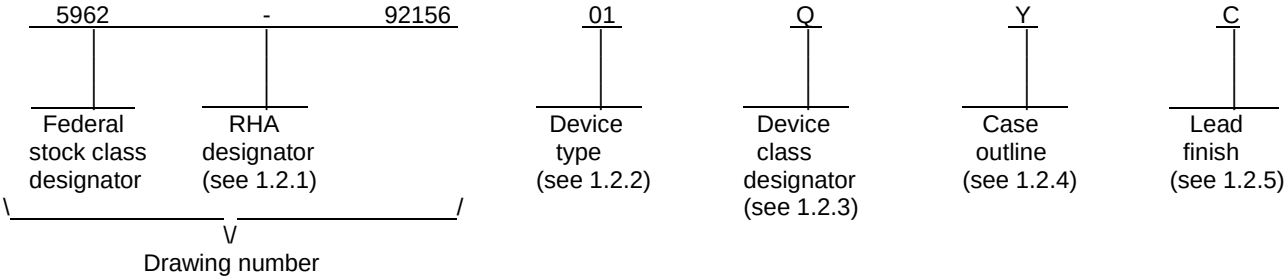
| SIZE | CAGE CODE | |
|---|---|---|
| **A** | **67268** | **5962-92156** |

SHEET 1 OF 33

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:




1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

| Device type | Generic number | Circuit function | Bin speed |
|---|---|---|---|
| 01 | 1280A | 8000 gate field programmable gate array | 200 ns |
| 02 | 1280A-1 | 8000 gate field programmable gate array | 170 ns |
| 03 | RH1280 | 8000 gate field programmable gate array (radiation hardened) | 160 ns |
| 04 | 1280XL | 8000 gate field programmable gate array | 120 ns |
| 05 | 1280XL-1 | 8000 gate field programmable gate array | 102 ns |
| 06 | RH1280B | 8000 gate field programmable gate array (radiation hardened) | 160 ns |
| 07 | RH1280B | 8000 gate field programmable gate array (radiation hardened) | 160 ns 1/ |

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

| Device class | Device requirements documentation |
|---|---|
| M | Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A |
| Q or V | Certification and qualification to MIL-PRF-38535 |

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| X | CMGA7 - P176 | 176 | Pin grid array |
| Y | See figure 1 | 172 | Quad flat pack |
| Z | CMGA7 - P176 | 177 | Pin grid array with orientation pin |
| U | See figure 1 | 172 | Quad flat pack |

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ Additional screening for device type 07 to be performed according to 4.2.2d.

1.3 Absolute maximum ratings. 2/

| | |
|---|---|
| DC supply voltage range ($V_{CC}$) | -0.5 V dc to +7.0 V dc |
| Input voltage range ($V_I$) | -0.5 V dc to $V_{CC}$ + 0.5 V dc |
| Output voltage range ($V_O$) | -0.5 V dc to $V_{CC}$ + 0.5 V dc |
| Input clamp current ($I_{IC}$) | ±20 mA |
| Output clamp current ($I_{OC}$) | ±20 mA |
| Continuous output current ($I_O$) | ±25 mA |
| Storage temperature range ($T_{STG}$) | -65°C to +150°C |
| Lead temperature (soldering, 10 seconds) | 300°C |
| Thermal resistance, junction-to-case ($\Theta_{JC}$) : | |
| Case X and Z | See MIL-STD-1835 |
| Case Y and U | 10°C/W 3/ |
| Maximum junction temperature ($T_J$) | +150°C |

1.4 Recommended operating conditions.

| | |
|---|---|
| Supply voltage ($V_{CC}$) | +4.5 V dc to +5.5 V dc |
| Case operating temperature range ($T_C$) | -55°C to +125°C |

1.5 Digital logic testing for device classes Q and V.

| | |
|---|---|
| Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) | 100 percent 4/ |

1.6 Radiation features

| | |
|---|---|
| Maximum total dose available (dose rate = 50 - 300 rad(Si)/s) | |
| For device type 03 | 300 krads(Si) 5/ |
| Maximum total dose available (dose rate ≤ 30 rad(Si)/s) | |
| For device types 06 and 07 | 100 krads(Si) 6/ |
| Single event phenomenon (SEP): | |
| Device type 03: No SEL occurs at an effective LET (see 4.4.4.2)... | ≤ 177 MeV/(mg/cm2) |
| Device types 06-07: No SEL occurs at an effective LET (see 4.4.4.2). | ≤ 80 MeV/(mg/cm2) |
| Device types 03: | |
| No SEU occurs at an effective LET (see 4.4.4.2) (C-mode) | ≤ 17 MeV/(mg/cm$^2$) |
| No SEU occurs at an effective LET (see 4.4.4.2) (S-mode ) | ≤ 4 MeV/(mg/cm$^2$) |
| Device types 06-07: | |
| No SEU occurs at an effective LET (see 4.4.4.2) (C-mode) | ≤ 5.7 MeV/(mg/cm2) |
| No SEU occurs at an effective LET (see 4.4.4.2) (S-mode) | ≤ 1.8 MeV/(mg/cm2) |
| Device types 03: No SEDR occurs at effective LET (see 4.4.4.2) | ≤ 60 MeV/(mg/cm2) |
| Device types 06-07 No SEDR occurs at effective LET (see 4.4.4.2) | ≤ 21 MeV/(mg/cm2) |

_____

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3/ When the thermal resistance for this case is specified in MIL-STD-1835, that value shall supersede the value indicated herein.

4/ 100 percent test coverage of blank programmable logic devices.

5/ For device type 03, device electrical characteristics are guaranteed for post irradiation levels at 25°C per MIL-STD-883, method 1019 for low dose rate environments (≤ 15 rad(Si)/sec).

6/ For device types 06-07 electrical characteristics are guaranteed for post irradiation levels at 25°C per MIL-STD-883, method 1019, condition B . The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition B to a maximum total dose of 100 krads(Si).

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation.

ASTM INTERNATIONAL (ASTM)

ASTM Standard F1192 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to: ASTM International, PO Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959; http://www.astm.org.)

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEDEC Standard No. 78 - IC Latch-Up Test.

(Copies of this document are available online at www.jedec.org/ or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240-S, Arlington, VA 22201).

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 and figure 1 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s).

3.2.3.1 Unprogrammed devices. The truth table or test vectors for unprogrammed devices for contracts involving no altered item drawing is not part of this drawing. When required in screening (see 4.2 herein) or quality conformance inspection group A, B, C, D, or E (see 4.4 herein), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of logic modules shall be utilized or at least 25 percent of the total logic modules shall be utilized for any altered item drawing pattern.

3.2.3.2 Programmed devices. The truth table or test vectors for programmed devices shall be as specified by an attached altered item drawing.

3.2.4 Switching test circuit and waveforms . The switching test circuit and waveforms diagram shall be as specified on figure 3.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-PRF-38535, appendix A).

3.11 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations; two processing options are provided for selection in the contract, using an altered item drawing.

3.11.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 4.4.1 and table IIA. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.11.2 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

TABLE IA. Electrical performance characteristics.

| Test | Symbol | Conditions 1/<br>4.5 V ≤ $V_{CC}$ ≤ 5.5 V<br>-55°C ≤ $T_C$ ≤ +125°C<br>unless otherwise specified | Group A Subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| High Level output voltage | $V_{OH}$ | Test one output at a time, $V_{CC}$ = 4.5 V, $I_{OH}$ = -3.2 mA | 1, 2, 3 | All | 3.7 | | V |
| Low level output voltage | $V_{OL}$ | Test one output at a time, $V_{CC}$ = 4.5 V, $I_{OL}$ = 4.0 mA | 1, 2, 3 | All | | 0.4 | V |
| Low level input voltage | $V_{IL}$ | | 1, 2, 3 | All | -0.3 | 0.8 | V |
| High level input voltage | $V_{IH}$ | | 1, 2, 3 | 01,02, 04,05 | 2.0 | $V_{CC}$ +0.3 | V |
| | | | | 03, 06, 07 | 2.2 | $V_{CC}$ +0.3 | |
| Standby supply current | $I_{DD}$ | Outputs unloaded, $V_{CC}$ = 5.5 V, $V_{IN}$ = $V_{CC}$ or GND | 1, 2, 3 | All | | 25 | mA |
| Input leakage current | $I_{IL}$ | $V_{CC}$ = 5.5 V, $V_{IN}$ = $V_{CC}$ or GND | 1, 2, 3 | All | -10 | 10 | µA |
| Output leakage current | $I_{OZ}$ | $V_{CC}$ = 5.5 V, $V_O$ = $V_{CC}$ or GND | 1, 2, 3 | All | -10 | 10 | µA |
| I/O terminal capacitance | $C_{I/O}$ | See 4.4.1c, f= 1.0 Mhz, $V_{OUT}$ = 0 V | 4 | All | | 20 | pF |
| Functional tests | FT 2/ | See 4.4.1e, $V_O$ = 0 V, $V_{CC}$ = 4.5 V | 7, 8A, 8B | All | | | |
| Binning circuit delay | $t_{PBLH}$, $t_{PBHL}$ | See figure 3, $V_{IL}$ = 0 V, $V_{IH}$ = 3.0 V, $V_{CC}$ = 4.5 V, $V_{OUT}$ = 1.5 V 3/ | 9, 10, 11 | 01 | | 200 | ns |
| | | | | 02 | | 170 | |
| | | | | 03, 06, 07 | | 160 | |
| | | | | 04 | | 120 | |
| | | | | 05 | | 102 | |

1/ All tests shall be performed under the worst case condition unless otherwise specified. Device type 03 supplied to this drawing will meet levels M, D, P, L, R, and F, of irradiation. However, this device is only tested at the "F" level. Device types 06 and 07 supplied to this drawing will meet levels M, D, P, L and R, of irradiation. However, devices 06 and 07 are only tested at the "R" level. Pre and post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, $T_A$ = +25°C.

2/ Devices are functionally tested using a serial scan test method. Data is shifted into the SDI pin and the DCLK pin is used as a clock. The data is used to drive the inputs of the internal logic and I/O modules, allowing a complete functional test to be performed. The outputs of the module can be read by shifting out the output response or by monitoring the PRA, PRB, or SDO pins. These tests form a part of the manufacturer's test tape and shall be maintained and available at the approved source(s) of supply upon request by DLA Land and Maritime or the OEM.

3/ Binning circuit delay is defined as the input-to-output delay of a special path called the "binning circuit". The binning circuit consists of one input buffer plus 16 combinatorial logic modules plus one output buffer. The logic modules are distributed along the left side of the device. These modules are configured as non-inverting buffers and are connected through programmed antifuses with typical capacitive loading.

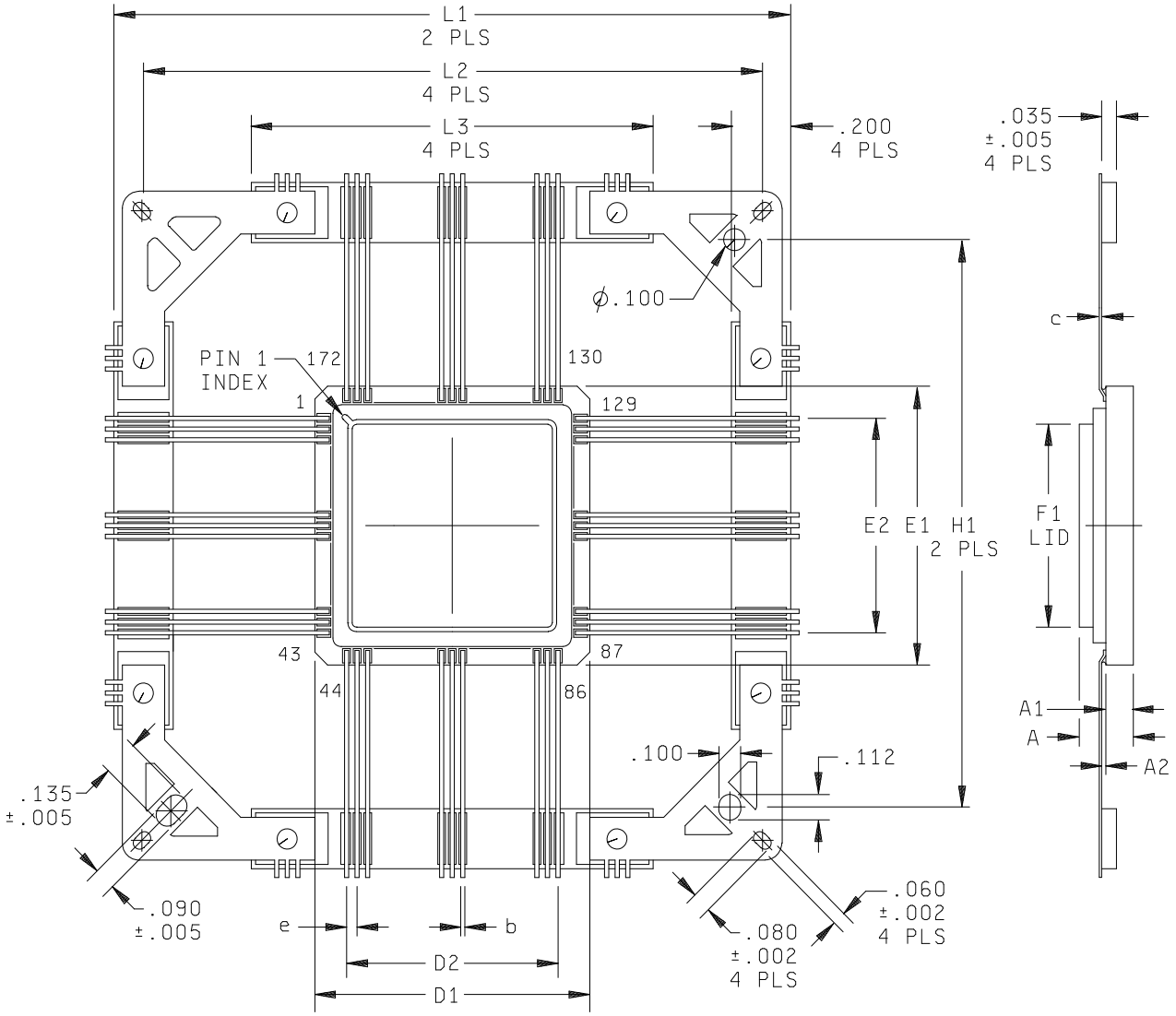
TABLE IB. SEP test limits. 1/ 2/

| Characteristics | Upset Mode | Conditions | Bias Vcc = | Device Type | Effective LET (MeV-$cm^2$/mg) | Saturated X-section |
|---|---|---|---|---|---|---|
| No Single event latch-up (SEL) occurs | All | $T_C$ = 125°C | 5.5 V | 03 | ≤ 177 | N/A |
| | | | | 06-07 | ≤ 80 | |
| No Single event upset (SEU) occurs | C-Latch (C mode) | $T_C$ = 25°C | 4.5 V | 03 | < 17 | $1.1 \times 10^{-6}$ $cm^2$/bit |
| | | | | 06-07 | < 5.7 | $1.7 \times 10^{-6}$ $cm^2$/bit |
| | 4 MHz Clock (S-mode) | $T_C$ = +25°C | 5.0 V | 03 | < 4 | $3.4 \times 10^{-6}$ $cm^2$/device |
| | | | | 06-07 | < 1.8 | $4.0 \times 10^{-6}$ $cm^2$/bit |
| No Single event dielectric (antifuse) rupture (SEDR) occurs | All | $T_C$= 125°C | 5.5 V | 03 | ≤ 60 | N/A |
| | | | | 06-07 | ≤ 21 | |

Notes:

1/ Verification test per TRB approved test plan.
2/ Table IB applies to device types 03, 06, 07 only.

Case Y




NOTES:

1. Tie bar is for reference only, the vendor supplies the tie bar with the 4 small corner holes as oblong holes, contact vendor for other tie bar options.
2. All exposed metalized areas and leads are gold plated 100 micro inches (2.5 µm) minimum thickness over 80 to 350 micro inches (2.0 to 8.9 µm) thickness nickel.
3. Seal ring area is connected to GNDA.
4. Die attach pad is connected to GNDA.
5. GNDQ (4 PLS) is connected to GNDA.
6. Tolerances unless otherwise specified: ±1% N.L.T ±0.005

FIGURE 1. Case outlines.

Case Y - Continued

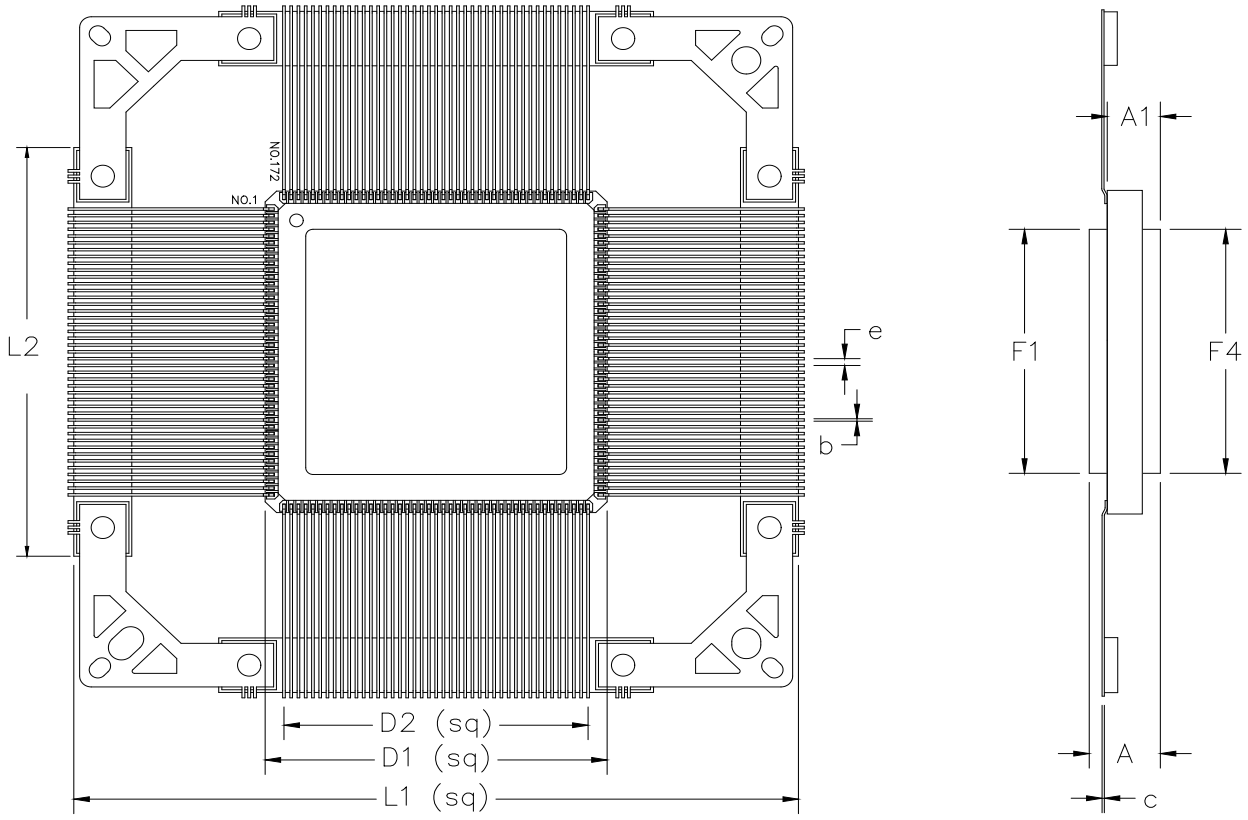
| Symbol | Dimension (unit: inch) | | |
|---|---|---|---|
| | Min. | Norm. | Max |
| A | 0.093 | 0.110 | 0.125 |
| A1 | 0.060 | 0.070 | 0.080 |
| A2 | 0.006 | 0.009 | 0.012 |
| b | 0.007 | 0.008 | 0.010 |
| c | 0.004 | 0.006 | 0.008 |
| D1/E1 | 1.168 | 1.180 | 1.192 |
| D2/E2 | 1.050 BSC | | |
| e | 0.025 BSC | | |
| F1 | 0.860 | 0.870 | 0.880 |
| L1 | 2.485 | 2.495 | 2.505 |
| L2 | 2.320 BSC | | |
| L3 | 1.485 | 1.500 | 1.515 |
| H1 | 2.140 BSC | | |
| Weight | 8.8 gm (typical) | | |

Metric conversion is for convenience only.

| Symbol | Dimension (unit: mm) | | |
|---|---|---|---|
| | Min. | Norm. | Max. |
| A | 2.36 | 2.79 | 3.18 |
| A1 | 1.52 | 1.78 | 2.03 |
| A2 | 0.15 | 0.23 | 0.30 |
| b | 0.18 | 0.20 | 0.25 |
| c | 0.10 | 0.15 | 0.20 |
| D1/E1 | 29.67 | 29.97 | 30.28 |
| D2/E2 | 26.67 BSC | | |
| e | 0.64 BSC | | |
| F1 | 21.84 | 22.10 | 22.35 |
| L1 | 63.12 | 63.37 | 63.63 |
| L2 | 58.93 | | |
| L3 | 37.72 | 38.10 | 38.48 |
| H1 | 54.36 BSC | | |
| Weight | 8.8 gm (typical) | | |

FIGURE 1. Case outlines - Continued.

Case U




NOTES:

1. Tie bar is for reference only, vendor supplies tie bar with oblong holes, contact vendor for other tie bar options.
2. All exposed metalized areas and leads are gold plated 100 microinches (2.5 µ mm) minimum thickness over 80 to 350 microinches (2.0 to 8.9 µ mm) thickness nickel.
3. Seal ring area is connected to GNDA.
4. Die attach pad is connected to GNDA.
5. GNDQ (4 PLS) is connected to GNDA.
6. Tolerances unless otherwise specified: ±1% N.L.T ±0.005

FIGURE 1. Case outlines - Continued.

Case U - Continued.

| Symbol | Dimension (inches) | | Dimension (millimeters) | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 0.116 | 0.146 | 2.95 | 3.71 |
| b | 0.007 | 0.013 | 0.17 | 0.33 |
| c | 0.004 | 0.008 | 0.10 | 0.20 |
| D1 | 1.138 | 1.162 | 28.91 | 29.52 |
| D2 | 1.050 BSC | | 26.67 BSC | |
| e | 0.025 BSC | | 0.635 BSC | |
| F1 | 0.890 | 0.900 | 22.60 | 22.86 |
| F4 | 0.881 | 0.890 | 22.38 | 22.60 |
| L1 | 2.485 | 2.505 | 63.12 | 63.63 |
| L2 | 1.690 | 1.710 | 42.93 | 43.43 |
| A1 | 0.079 | 0.103 | 2.00 | 2.62 |
| N (number of leads) | 172 | | | |
| Weight | 20 gm (Typical - with tie bar removed) | | | |

FIGURE 1. Case outlines - Continued.

Case outlines X and Z

| Device type | All | | Device type | All | | Device type | All | | Device type | All |
|---|---|---|---|---|---|---|---|---|---|---|
| Terminal number | Terminal symbol | | Terminal number | Terminal symbol | | Terminal number | Terminal symbol | | Terminal number | Terminal symbol |
| A1 | I/O | | D1 | I/O | | H1 | I/O | | M13 | I/O |
| A2 | I/O | | D2 | I/O | | H2 | VSV or $V_{CC}$ | | M14 | I/O |
| A3 | I/O | | D3 | I/O | | H3 | $V_{CC}$ | | M15 | I/O |
| A4 | I/O | | D4 | GND | | H4 | GND | | N1 | I/O |
| A5 | I/O | | D5 | $V_{CC}$ | | H12 | GND | | N2 | I/O |
| A6 | I/O | | D6 | GND | | H13 | $V_{CC}$ | | N3 | I/O |
| A7 | I/O | | D7 | PRB or I/O | | H14 | VSV or $V_{CC}$ | | N4 | I/O |
| A8 | I/O | | D8 | $V_{CC}$ | | H15 | I/O | | N5 | I/O |
| A9 | CKA or I/O | | D9 | I/O | | J1 | I/O | | N6 | I/O |
| A10 | I/O | | D10 | GND | | J2 | I/O | | N7 | I/O |
| A11 | I/O | | D11 | $V_{CC}$ | | J3 | I/O | | N8 | $V_{CC}$ |
| A12 | I/O | | D12 | GND | | J4 | $V_{CC}$ | | N9 | I/O |
| A13 | I/O | | D13 | I/O | | J12 | GND | | N10 | I/O |
| A14 | I/O | | D14 | I/O | | J13 | VKS or GND | | N11 | I/O |
| A15 | I/O | | D15 | I/O | | J14 | VPP or $V_{CC}$ | | N12 | I/O |
| B1 | I/O | | E1 | I/O | | J15 | I/O | | N13 | I/O |
| B2 | I/O | | E2 | I/O | | K1 | I/O | | N14 | I/O |
| B3 | DCK or I/O | | E3 | I/O | | K2 | I/O | | N15 | I/O |
| B4 | I/O | | E4 | GND | | K3 | I/O | | P1 | I/O |
| B5 | I/O | | E5 | GND 1/ | | K4 | GND | | P2 | I/O |
| B6 | I/O | | E12 | GND | | K12 | GND | | P3 | I/O |
| B7 | I/O | | E13 | I/O | | K13 | I/O | | P4 | I/O |
| B8 | CKB or I/O | | E14 | I/O | | K14 | I/O | | P5 | I/O |
| B9 | I/O | | E15 | I/O | | K15 | I/O | | P6 | I/O |
| B10 | I/O | | F1 | I/O | | L1 | I/O | | P7 | I/O |
| B11 | I/O | | F2 | I/O | | L2 | I/O | | P8 | I/O |
| B12 | I/O | | F3 | I/O | | L3 | I/O | | P9 | I/O |
| B13 | I/O | | F4 | $V_{CC}$ | | L4 | GND | | P10 | I/O |
| B14 | SDI or I/O | | F12 | GND | | L12 | I/O | | P11 | I/O |
| B15 | I/O | | F13 | I/O | | L13 | I/O | | P12 | I/O |
| C1 | I/O | | F14 | I/O | | L14 | I/O | | P13 | SDO or I/O |
| C2 | I/O | | F15 | I/O | | L15 | I/O | | P14 | I/O |
| C3 | MODE | | G1 | I/O | | M1 | I/O | | P15 | I/O |
| C4 | I/O | | G2 | I/O | | M2 | I/O | | R1 | I/O |
| C5 | I/O | | G3 | I/O | | M3 | I/O | | R2 | I/O |
| C6 | I/O | | G4 | GND | | M4 | GND | | R3 | I/O |
| C7 | I/O | | G12 | $V_{CC}$ | | M5 | $V_{CC}$ | | R4 | I/O |
| C8 | GND | | G13 | I/O | | M6 | GND | | R5 | I/O |
| C9 | PRA or I/O | | G14 | I/O | | M7 | I/O | | R6 | I/O |
| C10 | I/O | | G15 | I/O | | M8 | GND | | R7 | I/O |
| C11 | I/O | | | | | M9 | I/O | | R8 | I/O |
| C12 | I/O | | | | | M10 | GND | | R9 | I/O |
| C13 | I/O | | | | | M11 | $V_{CC}$ | | R10 | I/O |
| C14 | I/O | | | | | M12 | GND | | R11 | I/O |
| C15 | I/O | | | | | | | | R12 | I/O |
| | | | | | | | | | R13 | I/O |
| | | | | | | | | | R14 | I/O |
| | | | | | | | | | R15 | I/O |

1/ E5 is an orientation pin that is available on package Z only.

FIGURE 2. Terminal connections.

Case outline Y and U

| Device type | All | | Device type | All | | Device type | All | | Device type | All |
|---|---|---|---|---|---|---|---|---|---|---|
| Terminal number | Terminal symbol | | Terminal number | Terminal symbol | | Terminal number | Terminal symbol | | Terminal number | Terminal symbol |
| 1 | MODE | | 51 | I/O | | 101 | I/O | | 151 | $V_{CC}$ |
| 2 | I/O | | 52 | I/O | | 102 | I/O | | 152 | GND |
| 3 | I/O | | 53 | I/O | | 103 | GND | | 153 | I/O |
| 4 | I/O | | 54 | I/O | | 104 | I/O | | 154 | CKB or I/O |
| 5 | I/O | | 55 | GND | | 105 | I/O | | 155 | I/O |
| 6 | I/O | | 56 | I/O | | 106 | VKS | | 156 | PRB or I/O |
| 7 | GND | | 57 | I/O | | 107 | VPP | | 157 | I/O |
| 8 | I/O | | 58 | I/O | | 108 | GND | | 158 | I/O |
| 9 | I/O | | 59 | I/O | | 109 | $V_{CC}$ | | 159 | I/O |
| 10 | I/O | | 60 | I/O | | 110 | VSV | | 160 | I/O |
| 11 | I/O | | 61 | I/O | | 111 | I/O | | 161 | GND |
| 12 | $V_{CC}$ | | 62 | I/O | | 112 | I/O | | 162 | I/O |
| 13 | I/O | | 63 | I/O | | 113 | $V_{CC}$ | | 163 | I/O |
| 14 | I/O | | 64 | I/O | | 114 | I/O | | 164 | I/O |
| 15 | I/O | | 65 | GND | | 115 | I/O | | 165 | I/O |
| 16 | I/O | | 66 | $V_{CC}$ | | 116 | I/O | | 166 | $V_{CC}$ |
| 17 | GND | | 67 | I/O | | 117 | I/O | | 167 | I/O |
| 18 | I/O | | 68 | I/O | | 118 | GND | | 168 | I/O |
| 19 | I/O | | 69 | I/O | | 119 | I/O | | 169 | I/O |
| 20 | I/O | | 70 | I/O | | 120 | I/O | | 170 | I/O |
| 21 | I/O | | 71 | I/O | | 121 | I/O | | 171 | DCK or I/O |
| 22 | GND | | 72 | I/O | | 122 | I/O | | 172 | I/O |
| 23 | $V_{CC}$ | | 73 | I/O | | 123 | GND | | | |
| 24 | VSV | | 74 | I/O | | 124 | I/O | | | |
| 25 | I/O | | 75 | GND | | 125 | I/O | | | |
| 26 | I/O | | 76 | I/O | | 126 | I/O | | | |
| 27 | $V_{CC}$ | | 77 | I/O | | 127 | I/O | | | |
| 28 | I/O | | 78 | I/O | | 128 | I/O | | | |
| 29 | I/O | | 79 | I/O | | 129 | I/O | | | |
| 30 | I/O | | 80 | $V_{CC}$ | | 130 | I/O | | | |
| 31 | I/O | | 81 | I/O | | 131 | SDI or I/O | | | |
| 32 | GND | | 82 | I/O | | 132 | I/O | | | |
| 33 | I/O | | 83 | I/O | | 133 | I/O | | | |
| 34 | I/O | | 84 | I/O | | 134 | I/O | | | |
| 35 | I/O | | 85 | SDO or I/O | | 135 | I/O | | | |
| 36 | I/O | | 86 | I/O | | 136 | $V_{CC}$ | | | |
| 37 | GND | | 87 | I/O | | 137 | I/O | | | |
| 38 | I/O | | 88 | I/O | | 138 | I/O | | | |
| 39 | I/O | | 89 | I/O | | 139 | I/O | | | |
| 40 | I/O | | 90 | I/O | | 140 | I/O | | | |
| 41 | I/O | | 91 | I/O | | 141 | GND | | | |
| 42 | I/O | | 92 | I/O | | 142 | I/O | | | |
| 43 | I/O | | 93 | I/O | | 143 | I/O | | | |
| 44 | I/O | | 94 | I/O | | 144 | I/O | | | |
| 45 | I/O | | 95 | I/O | | 145 | I/O | | | |
| 46 | I/O | | 96 | I/O | | 146 | I/O | | | |
| 47 | I/O | | 97 | I/O | | 147 | I/O | | | |
| 48 | I/O | | 98 | GND | | 148 | PRA or I/O | | | |
| 49 | I/O | | 99 | I/O | | 149 | I/O | | | |
| 50 | $V_{CC}$ | | 100 | I/O | | 150 | CKA or I/O | | | |

FIGURE 2. Terminal connections - Continued.

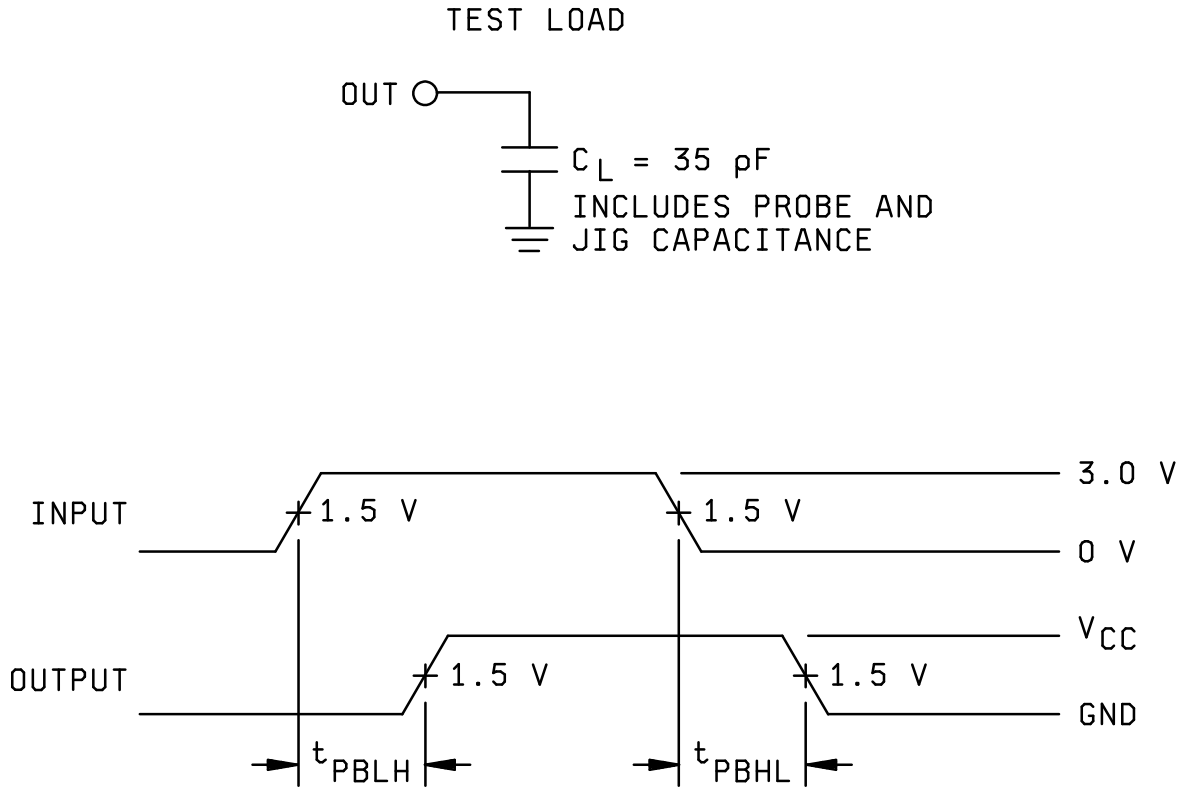



FIGURE 3. Switching test circuit and waveforms.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) $T_A$ = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

d. Additional screening for device type 07 shall include:

(1) 100% X-ray per MIL-STD-883, method 2012
(2) Increased burn-in (240 hours) dynamic burn-in
(3) interim room temperature electrical test
(4) 144 hours static burn-in with tightened class V PDA

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table IA of method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 ($C_{I/O}$ measurement) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency equal or less than 1 MHz. Sample size is five (5) devices with no failures, and all input and output terminals tested.

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's technical review board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on 5 devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard No. 78 may be used for reference.

e. Programmed device (see 3.2.3.2) - For device class M, subgroups 7, 8A, and 8B tests shall consist of verifying the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device. These tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.6 herein).

f. Unprogrammed devices shall be tested for programmability and dc and ac performance compliance to the requirements of group A, subgroups 1 and 7.

(1) A sample shall be selected from each wafer lot to satisfy programmability requirements. Eight devices shall be submitted to programming (see 3.2.3.1). If any device fails to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 18 total devices with no more than two total device failures allowable.

(2) These eight devices shall also be submitted to the requirements of the specified tests of group A, subgroups 1 and 7. If any device fails, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 18 total devices with no more than two total device failures allowable.

(3a) Eight devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9 for binning circuit delay only. If any device fails, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 18 total devices with no more than two total device failures allowable.

(3b) If the binning circuit is tested on 100 percent of the products, then the above requirement (3a) is met.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005.

b. $T_A$ = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at $T_A$ = +25°C ± 5°C, after exposure, to the subgroups specified in table IIA herein.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

| Line no. | Test requirements | Subgroups (in accordance with MIL-STD-883, TM 5005, table I) | Subgroups (in accordance with MIL-PRF-38535, table III) | |
|---|---|---|---|---|
| | | Device class M | Device class Q | Device class V |
| 1 | Interim electrical parameters (see 4.2) | | | 1, 7, 9 |
| 2 | Static burn-in (method 1015) | Not required | Not required | Required |
| 3 | Same as line 1 | | | 1*, 7* Δ |
| 4 | Dynamic burn-in (method 1015) | Required | Required | Required |
| 5 | Same as line 1 | | | 1*, 7* Δ |
| 6 | Final electrical parameters (see 4.2) | 1*, 2, 3, 7*, 8A, 8B, 9, 10, 11 | 1*, 2, 3, 7*, 8A, 8B, 9, 10, 11 | 1*, 2, 3, 7*, 8A, 8B, 9, 10, 11 |
| 7 | Group A test requirements (see 4.4) | 1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11 | 1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11 | 1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11 |
| 8 | Group C end-point electrical parameters (see 4.4) | 2, 3, 7, 8A, 8B | 2, 3, 7, 8A, 8B | 1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ |
| 9 | Group D end-point electrical parameters (see 4.4) | 2, 3, 8A, 8B | 2, 3, 8A, 8B | 2, 3, 8A, 8B |
| 10 | Group E end-point electrical parameters (see 4.4) | 1, 7, 9 | 1, 7, 9 | 1, 7, 9 |

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the functionality for unprogrammed devices or that the altered item drawing pattern exists for programmed devices.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1c.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d

TABLE IIB. Delta limits at +25°C.

| Parameter 1/ | Device types |
|---|---|
| | All |
| $I_{DD}$ | ±10% of specified value of table IA |
| $I_{OZ}$ | ±10% of specified value of table IA |
| $t_{PBLH}$, $t_{PBHL}$ | ±10 ns |

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.4.4.1 Total dose irradiation testing. For device type 03, total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A, as specified in 1.6 herein. For device types 06-07, total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition B, as specified in 1.6 herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at +25ºC ± 5ºC. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60º to the normal, inclusive (i.e. 0º≤ angle ≤ 60º). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ $10^7$ ions/cm2.

c. The flux shall be between $10^2$ and $10^5$ ions/$cm^2$. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be > 20 microns in silicon.

e. The upset test temperature shall be +25ºC. The latchup test temperature shall be at the maximum rated operating temperature ±10ºC.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. For SEP test limits, see table IB herein.

h. Supply current and voltage(s) as well as SEU, SEL and faults are monitored and recorded in-situ.

.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

4.6 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

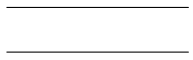
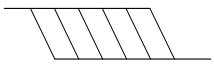
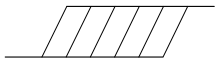
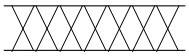
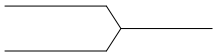
6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

| Waveform symbol | Input | Output |
|---|---|---|
|  | MUST BE VALID | WILL BE VALID |
|  | CHANGE FROM H TO L | WILL CHANGE FROM H TO L |
|  | CHANGE FROM L TO H | WILL CHANGE FROM L TO H |
|  | DON'T CARE ANY CHANGE PERMITTED | CHANGING STATE UNKNOWN |
|  | | HIGH IMPEDANCE |

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

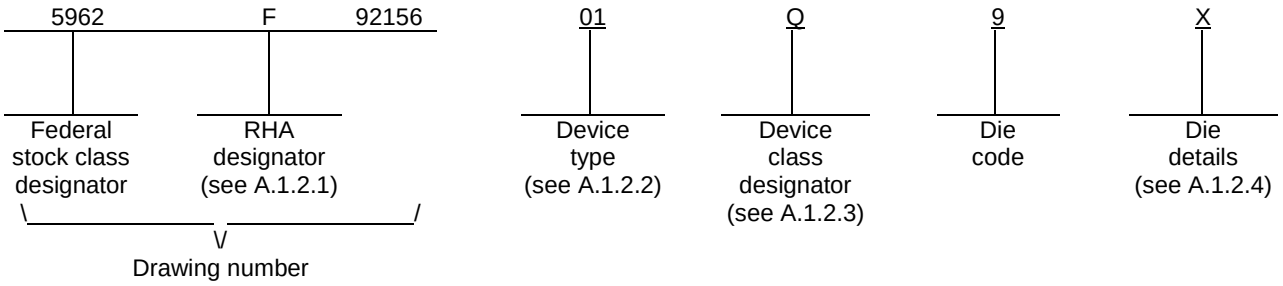
6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-92156

A.1 Scope

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QML plan for use in monolithic microcircuits, multichip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:




A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

| Device type | Generic number | Circuit function | Bin speed |
|---|---|---|---|
| 01 | 1280A | 8000 gate, field programmable gate array | 200 ns |
| 03 | RH1280 | 8000 gate, field programmable gate array | 160 ns |
| 04 | 1280XL | 8000 gate, field programmable gate array | 120 ns |

A.1.2.3 Device class designator.

| Device class | Device requirements documentation |
|---|---|
| Q or V | Certification and qualification to the die requirements of MIL-PRF-38535 |

A.1.2.4 Die code. The die code designator shall be a number 9 for all devices supplied as die only with no case outline.

A.1.2.5 Die details. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.5.1 Die physical dimensions.

| Device type | Die size | Die thickness | Die Detail | Figure Number |
|---|---|---|---|---|
| 01 | 421mils X 437mils | 15±1 mils | A | A-1 |
| 01 | 421mils X 437mils | 16±1 mils | B | A-2 |
| 03 | 365 mils X 385 mils | 25±1 mils | C | A-3 |
| 04 | 286 mils X 299 mils | 19±1 mils | D | A-4 |

A.1.2.5.2 Die bonding pad locations and electrical functions.

| Device type | Die Detail | Figure Number |
|---|---|---|
| 01 | A | A-1 |
| 01 | B | A-2 |
| 03 | C | A-3 |
| 04 | D | A-4 |

A.1.2.5.3 Interface materials.

| Device type | Top metalization | Backside metalization | Die Detail | Figure Number |
|---|---|---|---|---|
| 01 | Ti-cap+Al/Cu/Si,9-12k | None (backgrind) | A | A-1 |
| 01 | TiW+Al/Cu,9-12k | None (backgrind) | B | A-2 |
| 03 | Ti-cap+Al/Cu/Si,9-12k | None (backgrind) | C | A-3 |
| 04 | Ti-cap+Al/Cu/Si,9-12k | None (backgrind) | D | A-4 |

A.1.2.5.4 Assembly related information.

| Device type | Glassivation | Die Detail | Figure Number |
|---|---|---|---|
| 01 | Ox/Nitride | A | A-1 |
| 01 | Ox/Nitride | B | A-2 |
| 03 | Ox/Nitride | C | A-3 |
| 04 | Ox/Nitride | D | A-4 |

A.1.2.5.5 Wafer fabrication source.

| Device type | Source | Die Detail | Figure Number |
|---|---|---|---|
| 01 | Matsushita Electronics Corp. Japan | A | A-1 |
| 01 | Texas Instrument, Texas | B | A-2 |
| 03 | BAE Systems, Manassas, VA | C | A-3 |
| 04 | Chartered Semiconductor, Singapore | D | A-4 |

A.1.3 Absolute maximum ratings.
See paragraph 1.3 within the body of this drawing for details.

A.1.4 Recommended operating conditions.
See paragraph 1.4 within the body of this drawing for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS.

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The Modification in the QM plan shall not effect the form, fit or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be specified in A.1.2.5.1 and on figures A-1, A-2, A-3, and A-4.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.5.2 and on figures A-1, A-2, A-3, and A-4.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.5.3 and on figures A-1, A-2, A-3, and A-4.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.5.4 and figures A-1, A-2, A-3, and A-4.

A.3.2.5 Truth table(s). The truth table(s) shall be as defined in paragraph 3.2.3 herein.

A.3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined in parapragh 3.2.5 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.3.8 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations; two processing options are provided for selection in the contract, using an altered item drawing.

A.3.8.1 Unprogrammed die delivered to the user. All testing shall be verified through wafer probe test as defined in A.4.2.

A.3.8.2 Manufacturer-programmed die delivered to the user. The programming integrity test shall be performed during programming. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see 3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified within paragraphs 4.4.4, 4.4.4.1, 4.4.4.1.1, and 4.4.4.2 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit application (original equipment), design applications and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0540.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

| Pad# | Name | X-Coord | Y-Coord |
|---|---|---|---|
| 1 | GND | -5075 | 4932 |
| 2 | MODE | -5075 | 4668 |
| 3 | I/O | -5075 | 4495 |
| 4 | I/O | -5075 | 4184 |
| 5 | I/O | -5075 | 4009 |
| 6 | I/O | -5075 | 3837 |
| 7 | I/O | -5075 | 3662 |
| 8 | GND | -5075 | 3490 |
| 9 | I/O | -5075 | 3318 |
| 10 | I/O | -5075 | 3143 |
| 11 | I/O | -5075 | 2974 |
| 12 | I/O | -5075 | 2800 |
| 13 | VCC | -5075 | 2560 |
| 14 | I/O | -5075 | 2316 |
| 15 | I/O | -5075 | 2141 |
| 16 | I/O | -5075 | 1969 |
| 17 | I/O | -5075 | 1794 |
| 18 | GND | -5075 | 1616 |
| 19 | I/O | -5075 | 1428 |
| 20 | I/O | -5075 | 1253 |
| 21 | I/O | -5075 | 1081 |
| 22 | I/O | -5075 | 906 |
| 23 | GND | -5075 | 377 |
| 24 | VCC | -5075 | 133 |
| 25 | VSV, VCC | -5075 | -602 |
| 26 | I/O | -5075 | -848 |
| 27 | I/O | -5075 | -1022 |
| 28 | VCC | -5075 | -1276 |
| 29 | I/O | -5075 | -1528 |
| 30 | I/O | -5075 | -1702 |
| 31 | I/O | -5075 | -1875 |
| 32 | I/O | -5075 | -2053 |
| 33 | GND | -5075 | -2373 |
| 34 | I/O | -5075 | -2626 |
| 35 | I/O | -5075 | -2800 |
| 36 | I/O | -5075 | -2973 |
| 37 | I/O | -5075 | -3148 |
| 38 | GND | -5075 | -3402 |
| 39 | I/O | -5075 | -3658 |
| 40 | I/O | -5075 | -3833 |
| 41 | I/O | -5075 | -4005 |
| 42 | I/O | -5075 | -4180 |
| 43 | I/O | -5075 | -4389 |
| 44 | I/O | -5075 | -4928 |

| Pad# | Name | X-Coord | Y-Coord |
|---|---|---|---|
| 45 | GND | -4706 | -5284 |
| 46 | I/O | -4073 | -5284 |
| 47 | I/O | -3793 | -5284 |
| 48 | I/O | -3613 | -5284 |
| 49 | I/O | -3444 | -5284 |
| 50 | I/O | -3269 | -5284 |
| 51 | I/O | -3100 | -5284 |
| 52 | VCC | -2859 | -5284 |
| 53 | I/O | -2619 | -5284 |
| 54 | I/O | -2450 | -5284 |
| 55 | I/O | -2275 | -5284 |
| 56 | I/O | -2106 | -5284 |
| 57 | GND | -1945 | -5284 |
| 58 | I/O | -1782 | -5284 |
| 59 | I/O | -1613 | -5284 |
| 60 | I/O | -1438 | -5284 |
| 61 | I/O | -1269 | -5284 |
| 62 | I/O | -1095 | -5284 |
| 63 | I/O | -926 | -5284 |
| 64 | I/O | -751 | -5284 |
| 65 | I/O | -582 | -5284 |
| 66 | I/O | -407 | -5284 |
| 67 | GND | -165 | -5284 |
| 68 | VCC | 154 | -5284 |
| 69 | I/O | 453 | -5284 |
| 70 | I/O | 628 | -5284 |
| 71 | I/O | 800 | -5284 |
| 72 | I/O | 975 | -5284 |
| 73 | I/O | 1147 | -5284 |
| 74 | I/O | 1322 | -5284 |
| 75 | I/O | 1495 | -5284 |
| 76 | I/O | 1669 | -5284 |
| 77 | GND | 1912 | -5284 |
| 78 | I/O | 2160 | -5284 |
| 79 | I/O | 2335 | -5284 |
| 80 | I/O | 2507 | -5284 |
| 81 | I/O | 2682 | -5284 |
| 82 | VCC | 2852 | -5284 |
| 83 | I/O | 3013 | -5284 |
| 84 | I/O | 3188 | -5284 |
| 85 | I/O | 3360 | -5284 |
| 86 | I/O | 3533 | -5284 |
| 87 | SDO, I/O | 4151 | -5284 |
| 88 | I/O | 4709 | -5284 |

See notes at end of table

Figure A-1 and A-2. A1280A Bond Pad Locations and Functions.

| Pad# | Name | X-Coord | Y-Coord |
|---|---|---|---|
| 89 | GND | 5075 | -4833 |
| 90 | I/O | 5075 | -4375 |
| 91 | I/O | 5075 | -4166 |
| 92 | I/O | 5075 | -3991 |
| 93 | I/O | 5075 | -3818 |
| 94 | I/O | 5075 | -3644 |
| 95 | I/O | 5075 | -3471 |
| 96 | I/O | 5075 | -3297 |
| 97 | I/O | 5075 | -3124 |
| 98 | I/O | 5075 | -2950 |
| 99 | I/O | 5075 | -2777 |
| 100 | I/O | 5075 | -2602 |
| 101 | GND | 5075 | -2429 |
| 102 | I/O | 5075 | -2268 |
| 103 | I/O | 5075 | -2094 |
| 104 | I/O | 5075 | -1921 |
| 105 | I/O | 5075 | -1746 |
| 106 | GND | 5075 | -1574 |
| 107 | I/O | 5075 | -1413 |
| 108 | I/O | 5075 | -1238 |
| 109 | VKS, GND | 5075 | -604 |
| 110 | VPP, VCC | 5075 | 63 |
| 111 | GND | 5075 | 428 |
| 112 | VCC | 5075 | 665 |
| 113 | VSV, VCC | 5075 | 989 |
| 114 | I/O | 5075 | 1232 |
| 115 | I/O | 5075 | 1406 |
| 116 | VCC | 5075 | 1579 |
| 117 | I/O | 5075 | 1751 |
| 118 | I/O | 5075 | 1925 |
| 119 | I/O | 5075 | 2098 |
| 120 | I/O | 5075 | 2272 |
| 121 | GND | 5075 | 2438 |
| 122 | I/O | 5075 | 2606 |
| 123 | I/O | 5075 | 2780 |
| 124 | I/O | 5075 | 2953 |
| 125 | I/O | 5075 | 3128 |
| 126 | GND | 5075 | 3289 |
| 127 | I/O | 5075 | 3461 |
| 128 | I/O | 5075 | 3636 |
| 129 | I/O | 5075 | 3808 |
| 130 | I/O | 5075 | 3983 |
| 131 | I/O | 5075 | 4394 |
| 132 | I/O | 5075 | 4952 |

| Pad# | Name | X-Coord | Y-Coord |
|---|---|---|---|
| 133 | GND | 4620 | 5284 |
| 134 | I/O | 4062 | 5284 |
| 135 | SDI, I/O | 3882 | 5284 |
| 136 | I/O | 3609 | 5284 |
| 137 | I/O | 3436 | 5284 |
| 138 | I/O | 3261 | 5284 |
| 139 | I/O | 3089 | 5284 |
| 140 | VCC | 2842 | 5284 |
| 141 | I/O | 2629 | 5284 |
| 142 | I/O | 2457 | 5284 |
| 143 | I/O | 2282 | 5284 |
| 144 | I/O | 2110 | 5284 |
| 145 | GND | 1876 | 5284 |
| 146 | I/O | 1642 | 5284 |
| 147 | I/O | 1470 | 5284 |
| 148 | I/O | 1295 | 5284 |
| 149 | I/O | 1122 | 5284 |
| 150 | I/O | 948 | 5284 |
| 151 | I/O | 775 | 5284 |
| 152 | PRA, I/O | 595 | 5284 |
| 153 | I/O | 350 | 5284 |
| 154 | CLKA, I/O | 176 | 5284 |
| 155 | VCC | 3 | 5284 |
| 156 | GND | -172 | 5284 |
| 157 | I/O | -393 | 5284 |
| 158 | CLKB, I/O | -568 | 5284 |
| 159 | I/O | -743 | 5284 |
| 160 | PRB, I/O | -987 | 5284 |
| 161 | I/O | -1168 | 5284 |
| 162 | I/O | -1340 | 5284 |
| 163 | I/O | -1515 | 5284 |
| 164 | I/O | -1688 | 5284 |
| 165 | GND | -2003 | 5284 |
| 166 | I/O | -2288 | 5284 |
| 167 | I/O | -2460 | 5284 |
| 168 | I/O | -2635 | 5284 |
| 169 | I/O | -2807 | 5284 |
| 170 | VCC | -2987 | 5284 |
| 171 | I/O | -3160 | 5284 |
| 172 | I/O | -3333 | 5284 |
| 173 | I/O | -3507 | 5284 |
| 174 | I/O | -3680 | 5284 |
| 175 | DCLK, I/O | -4188 | 5284 |
| 176 | I/O | -4715 | 5284 |

Note: 1. All dimensions in micrometer
2. The die center is the coordinate origin (0,0).
3. VSV, VKS and Vpp pins are used for programming. For normal operation, these pins should be connected to Vcc or GND as shown.

Figure A-1 and A-2. A1280A Bond Pad Locations and Functions - Continued.

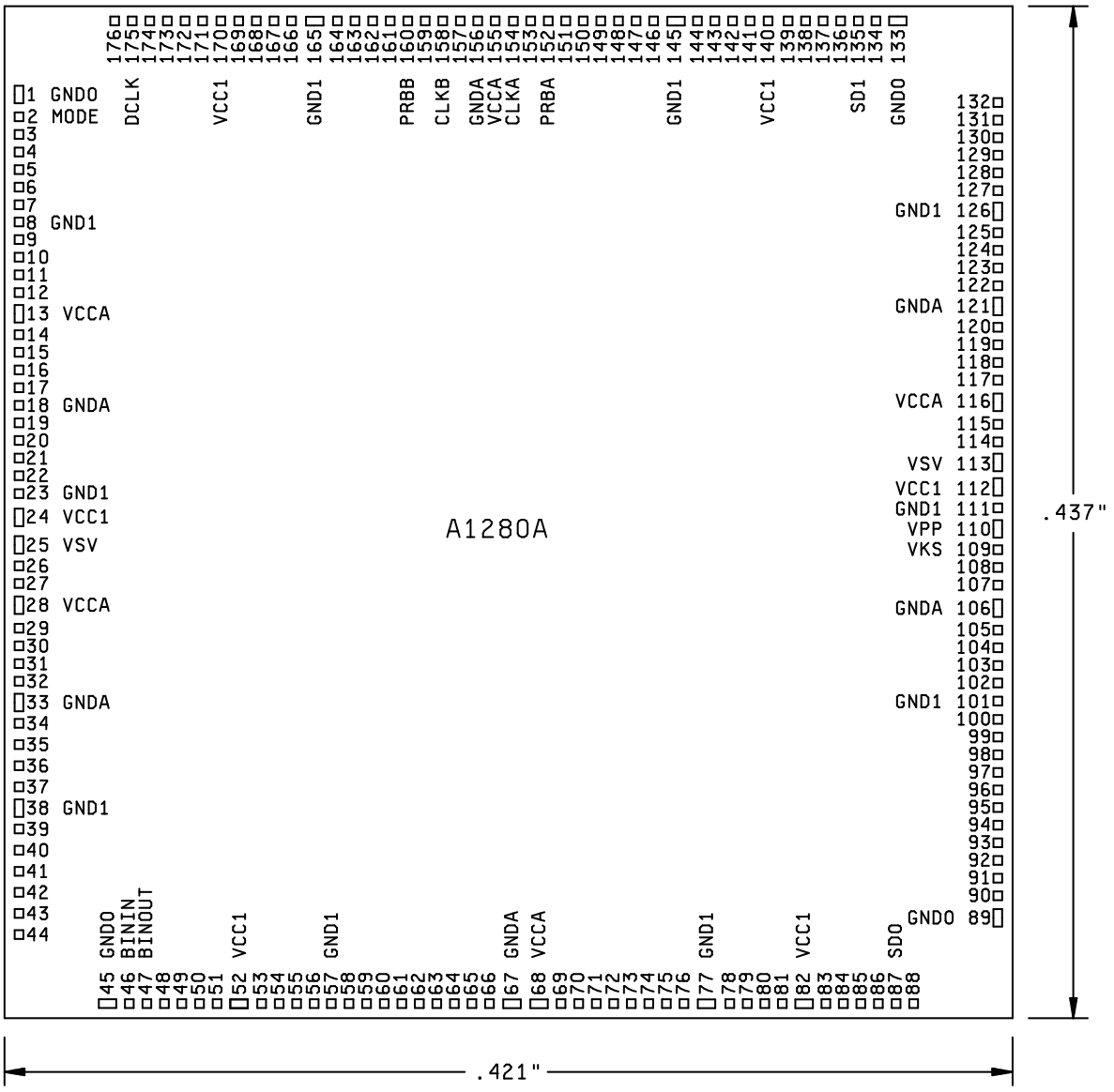



Figure A-1 and A-2. A1280A Bond Pad Locations and Functions - Continued.

| Pad # | Name | X Coords | Y Coords |
|---|---|---|---|
| 1 | GND | -4301 | 4178 |
| 2 | MODE | -4301 | 4019 |
| 3 | I/O | -4301 | 3867 |
| 4 | I/O | -4301 | 3723 |
| 5 | I/O | -4301 | 3579 |
| 6 | I/O | -4301 | 3436 |
| 7 | I/O | -4301 | 3223 |
| 8 | GND | -4301 | 2976 |
| 9 | I/O | -4301 | 2730 |
| 10 | I/O | -4301 | 2518 |
| 11 | I/O | -4301 | 2305 |
| 12 | I/O | -4301 | 2093 |
| 13 | VCC | -4301 | 1863 |
| 14 | I/O | -4301 | 1695 |
| 15 | I/O | -4301 | 1545 |
| 16 | I/O | -4301 | 1395 |
| 17 | I/O | -4301 | 1245 |
| 18 | GND | -4301 | 1076 |
| 19 | I/O | -4301 | 915 |
| 20 | I/O | -4301 | 771 |
| 21 | I/O | -4301 | 627 |
| 22 | I/O | -4301 | 483 |
| 23 | GND | -4301 | 13 |
| 24 | VCC | -4301 | -199 |
| 25 | VSV, VCC | -4301 | -726 |
| 26 | I/O | -4301 | -872 |
| 27 | I/O | -4301 | -1017 |
| 28 | VCC | -4301 | -1181 |
| 29 | I/O | -4301 | -1347 |
| 30 | I/O | -4301 | -1491 |
| 31 | I/O | -4301 | -1635 |
| 32 | I/O | -4301 | -1778 |
| 33 | GND | -4301 | -1940 |
| 34 | I/O | -4301 | -2197 |
| 35 | I/O | -4301 | -2435 |
| 36 | I/O | -4301 | -2674 |
| 37 | I/O | -4301 | -2912 |
| 38 | GND | -4301 | -3185 |
| 39 | I/O | -4301 | -3458 |
| 40 | I/O | -4301 | -3601 |
| 41 | I/O | -4301 | -3745 |
| 42 | I/O | -4301 | -3889 |
| 43 | I/O | -4301 | -4033 |
| 44 | I/O | -4301 | -4178 |

| Pad # | Name | X Coords | Y Coords |
|---|---|---|---|
| 45 | GND | -3963 | -4516 |
| 46 | I/O | -3811 | -4516 |
| 47 | I/O | -3652 | -4516 |
| 48 | I/O | -3508 | -4516 |
| 49 | I/O | -3364 | -4516 |
| 50 | I/O | -3220 | -4516 |
| 51 | I/O | -3077 | -4516 |
| 52 | VCC | -2869 | -4516 |
| 53 | I/O | -2662 | -4516 |
| 54 | I/O | -2491 | -4516 |
| 55 | I/O | -2318 | -4516 |
| 56 | I/O | -2145 | -4516 |
| 57 | GND | -1938 | -4516 |
| 58 | I/O | -1731 | -4516 |
| 59 | I/O | -1558 | -4516 |
| 60 | I/O | -1385 | -4516 |
| 61 | I/O | -1212 | -4516 |
| 62 | I/O | -1039 | -4516 |
| 63 | I/O | -867 | -4516 |
| 64 | I/O | -694 | -4516 |
| 65 | I/O | -521 | -4516 |
| 66 | I/O | -348 | -4516 |
| 67 | GND | -156 | -4516 |
| 68 | VCC | 24 | -4516 |
| 69 | I/O | 247 | -4516 |
| 70 | I/O | 451 | -4516 |
| 71 | I/O | 656 | -4516 |
| 72 | I/O | 860 | -4516 |
| 73 | I/O | 1064 | -4516 |
| 74 | I/O | 1269 | -4516 |
| 75 | I/O | 1473 | -4516 |
| 76 | I/O | 1678 | -4516 |
| 77 | GND | 1917 | -4516 |
| 78 | I/O | 2156 | -4516 |
| 79 | I/O | 2360 | -4516 |
| 80 | I/O | 2550 | -4516 |
| 81 | I/O | 2739 | -4516 |
| 82 | VCC | 2976 | -4516 |
| 83 | I/O | 3222 | -4516 |
| 84 | I/O | 3366 | -4516 |
| 85 | I/O | 3509 | -4516 |
| 86 | I/O | 3653 | -4516 |
| 87 | SDO, I/O | 3819 | -4516 |
| 88 | I/O | 3963 | -4516 |

See notes at end of table.

Figure A-3. RH1280 Bond Pad Locations and Functions

| Pad # | Name | X Coords | Y Coords |
|---|---|---|---|
| 89 | GND | 4301 | -4176 |
| 90 | I/O | 4301 | -4016 |
| 91 | I/O | 4301 | -3866 |
| 92 | I/O | 4301 | -3717 |
| 93 | I/O | 4301 | -3568 |
| 94 | I/O | 4301 | -3418 |
| 95 | I/O | 4301 | -3013 |
| 96 | I/O | 4301 | -2869 |
| 97 | I/O | 4301 | -2725 |
| 98 | I/O | 4301 | -2581 |
| 99 | I/O | 4301 | -2438 |
| 100 | I/O | 4301 | -2294 |
| 101 | GND | 4301 | -2116 |
| 102 | I/O | 4301 | -1938 |
| 103 | I/O | 4301 | -1794 |
| 104 | I/O | 4301 | -1650 |
| 105 | I/O | 4301 | -1507 |
| 106 | GND | 4301 | -1342 |
| 107 | I/O | 4301 | -1165 |
| 108 | I/O | 4301 | -1007 |
| 109 | VKS, GND | 4301 | -564 |
| 110 | VPP, VCC | 4301 | -97 |
| 111 | GND | 4301 | 96 |
| 112 | VCC | 4301 | 323 |
| 113 | VSV, VCC | 4301 | 516 |
| 114 | I/O | 4301 | 675 |
| 115 | I/O | 4301 | 833 |
| 116 | VCC | 4301 | 1010 |
| 117 | I/O | 4301 | 1178 |
| 118 | I/O | 4301 | 1328 |
| 119 | I/O | 4301 | 1478 |
| 120 | I/O | 4301 | 1628 |
| 121 | GND | 4301 | 1796 |
| 122 | I/O | 4301 | 1977 |
| 123 | I/O | 4301 | 2140 |
| 124 | I/O | 4301 | 2303 |
| 125 | I/O | 4301 | 2466 |
| 126 | GND | 4301 | 2663 |
| 127 | I/O | 4301 | 2860 |
| 128 | I/O | 4301 | 3023 |
| 129 | I/O | 4301 | 3186 |
| 130 | I/O | 4301 | 3330 |
| 131 | I/O | 4301 | 3672 |
| 132 | I/O | 4301 | 4178 |

| Pad # | Name | X Coords | Y Coords |
|---|---|---|---|
| 133 | GND | 3963 | 4516 |
| 134 | I/O | 3551 | 4516 |
| 135 | SDO, I/O | 3407 | 4516 |
| 136 | I/O | 3263 | 4516 |
| 137 | I/O | 3120 | 4516 |
| 138 | I/O | 2956 | 4516 |
| 139 | I/O | 2794 | 4516 |
| 140 | VCC | 2598 | 4516 |
| 141 | I/O | 2401 | 4516 |
| 142 | I/O | 2239 | 4516 |
| 143 | I/O | 2077 | 4516 |
| 144 | I/O | 1915 | 4516 |
| 145 | GND | 1719 | 4516 |
| 146 | I/O | 1522 | 4516 |
| 147 | I/O | 1360 | 4516 |
| 148 | I/O | 1198 | 4516 |
| 149 | I/O | 1036 | 4516 |
| 150 | I/O | 874 | 4516 |
| 151 | I/O | 712 | 4516 |
| 152 | PRA, I/O | 550 | 4516 |
| 153 | I/O | 372 | 4516 |
| 154 | CLKA, I/O | 210 | 4516 |
| 155 | VCC | 48 | 4516 |
| 156 | GND | -132 | 4516 |
| 157 | I/O | -356 | 4516 |
| 158 | CLKB, I/O | -543 | 4516 |
| 159 | I/O | -729 | 4516 |
| 160 | PRB, I/O | -932 | 4516 |
| 161 | I/O | -1119 | 4516 |
| 162 | I/O | -1305 | 4516 |
| 163 | I/O | -1492 | 4516 |
| 164 | I/O | -1678 | 4516 |
| 165 | GND | -1899 | 4516 |
| 166 | I/O | -2120 | 4516 |
| 167 | I/O | -2307 | 4516 |
| 168 | I/O | -2494 | 4516 |
| 169 | I/O | -2680 | 4516 |
| 170 | VCC | -2901 | 4516 |
| 171 | I/O | -3114 | 4516 |
| 172 | I/O | -3286 | 4516 |
| 173 | I/O | -3430 | 4516 |
| 174 | I/O | -3574 | 4516 |
| 175 | DCLK, I/O | -3717 | 4516 |
| 176 | I/O | -3963 | 4516 |

Note: 1. All dimensions in micrometer
2. The die center is the coordinate origin (0,0).
3. VSV, VKS and Vpp pins are used for programming. For normal operation, these pins should be connected to Vcc or GND as shown.

Figure A-3. RH1280 Bond Pad Locations and Functions - Continued.

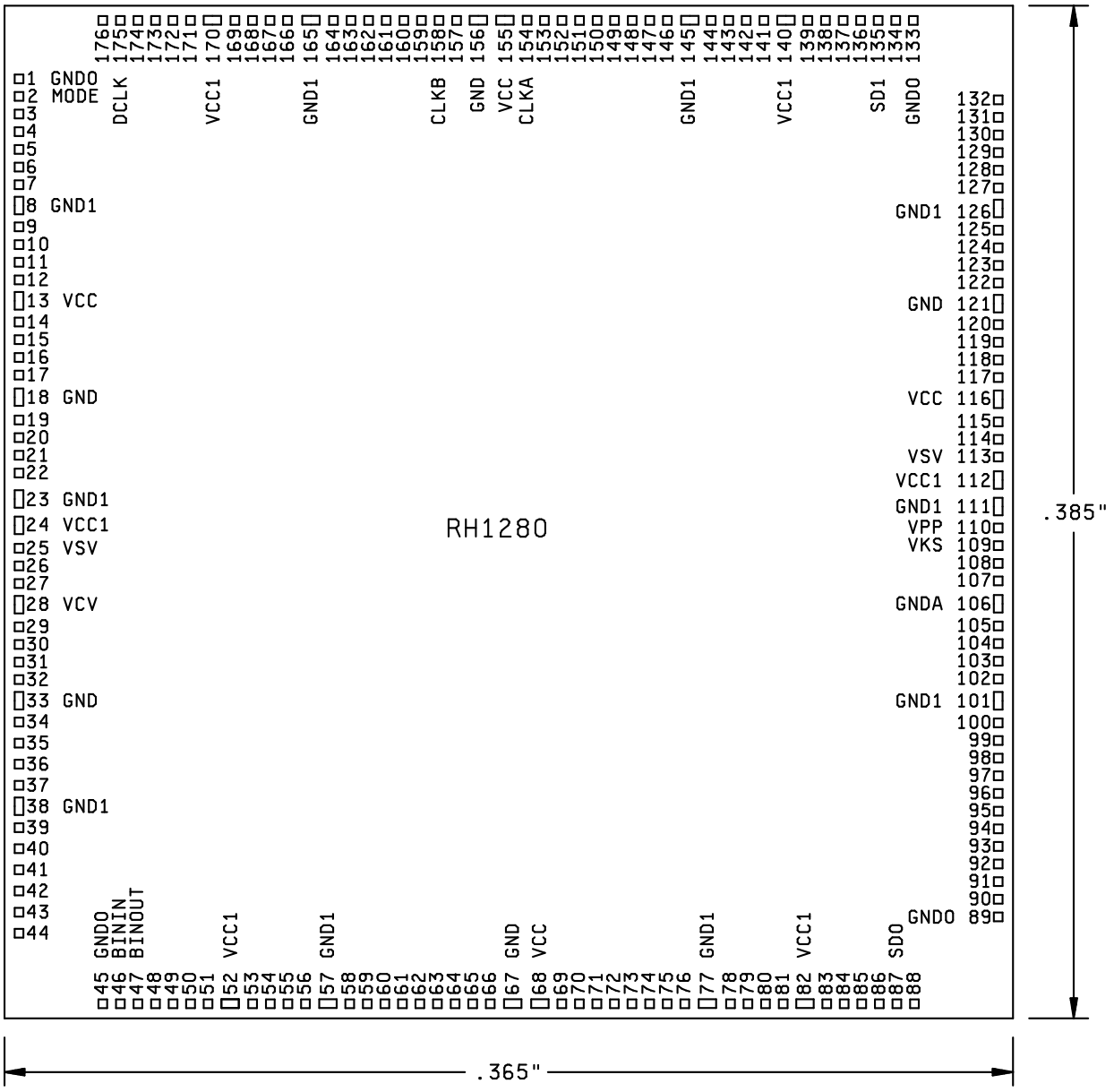



Figure A-3. RH1280 Bond Pad Locations and Functions - Continued.

| Pad # | Name | X Coords | Y Coords |
|---|---|---|---|
| 1 | GND | -3453 | 3354 |
| 2 | MODE | -3453 | 3226 |
| 3 | I/O | -3453 | 3104 |
| 4 | I/O | -3453 | 2989 |
| 5 | I/O | -3453 | 2874 |
| 6 | I/O | -3453 | 2758 |
| 7 | I/O | -3453 | 2587 |
| 8 | GND | -3453 | 2389 |
| 9 | I/O | -3453 | 2191 |
| 10 | I/O | -3453 | 2021 |
| 11 | I/O | -3453 | 1851 |
| 12 | I/O | -3453 | 1681 |
| 13 | VCC | -3453 | 1496 |
| 14 | I/O | -3453 | 1361 |
| 15 | I/O | -3453 | 1240 |
| 16 | I/O | -3453 | 1120 |
| 17 | I/O | -3453 | 999 |
| 18 | GND | -3453 | 864 |
| 19 | I/O | -3453 | 734 |
| 20 | I/O | -3453 | 619 |
| 21 | I/O | -3453 | 503 |
| 22 | I/O | -3453 | 388 |
| 23 | GND | -3453 | 11 |
| 24 | VCC | -3453 | -160 |
| 25 | VSV, VCC | -3453 | -583 |
| 26 | I/O | -3453 | -700 |
| 27 | I/O | -3453 | -817 |
| 28 | VCC | -3453 | -948 |
| 29 | I/O | -3453 | -1082 |
| 30 | I/O | -3453 | -1197 |
| 31 | I/O | -3453 | -1312 |
| 32 | I/O | -3453 | -1428 |
| 33 | GND | -3453 | -1558 |
| 34 | I/O | -3453 | -1764 |
| 35 | I/O | -3453 | -1955 |
| 36 | I/O | -3453 | -2146 |
| 37 | I/O | -3453 | -2338 |
| 38 | GND | -3453 | -2557 |
| 39 | I/O | -3453 | -2776 |
| 40 | I/O | -3453 | -2891 |
| 41 | I/O | -3453 | -3007 |
| 42 | I/O | -3453 | -3122 |
| 43 | I/O | -3453 | -3237 |
| 44 | I/O | -3453 | -3354 |

| Pad # | Name | X Coords | Y Coords |
|---|---|---|---|
| 45 | GND | -3182 | -3625 |
| 46 | I/O | -3060 | -3625 |
| 47 | I/O | -2932 | -3625 |
| 48 | I/O | -2816 | -3625 |
| 49 | I/O | -2701 | -3625 |
| 50 | I/O | -2585 | -3625 |
| 51 | I/O | -2470 | -3625 |
| 52 | VCC | -2303 | -3625 |
| 53 | I/O | -2137 | -3625 |
| 54 | I/O | -2000 | -3625 |
| 55 | I/O | -1861 | -3625 |
| 56 | I/O | -1722 | -3625 |
| 57 | GND | -1556 | -3625 |
| 58 | I/O | -1389 | -3625 |
| 59 | I/O | -1251 | -3625 |
| 60 | I/O | -1112 | -3625 |
| 61 | I/O | -973 | -3625 |
| 62 | I/O | -834 | -3625 |
| 63 | I/O | -696 | -3625 |
| 64 | I/O | -557 | -3625 |
| 65 | I/O | -418 | -3625 |
| 66 | I/O | -280 | -3625 |
| 67 | GND | -125 | -3625 |
| 68 | VCC | 19 | -3625 |
| 69 | I/O | 198 | -3625 |
| 70 | I/O | 362 | -3625 |
| 71 | I/O | 526 | -3625 |
| 72 | I/O | 690 | -3625 |
| 73 | I/O | 855 | -3625 |
| 74 | I/O | 1019 | -3625 |
| 75 | I/O | 1183 | -3625 |
| 76 | I/O | 1347 | -3625 |
| 77 | GND | 1539 | -3625 |
| 78 | I/O | 1731 | -3625 |
| 79 | I/O | 1895 | -3625 |
| 80 | I/O | 2047 | -3625 |
| 81 | I/O | 2199 | -3625 |
| 82 | VCC | 2389 | -3625 |
| 83 | I/O | 2587 | -3625 |
| 84 | I/O | 2702 | -3625 |
| 85 | I/O | 2817 | -3625 |
| 86 | I/O | 2933 | -3625 |
| 87 | SDO, I/O | 3066 | -3625 |
| 88 | I/O | 3182 | -3625 |

See notes at end of table.

Figure A-4. A1280XL(0.6µm) Bond Pad Locations and Functions.

| Pad # | Name | X Coords | Y Coords |
|---|---|---|---|
| 89 | GND | 3453 | -3352 |
| 90 | I/O | 3453 | -3224 |
| 91 | I/O | 3453 | -3104 |
| 92 | I/O | 3453 | -2984 |
| 93 | I/O | 3453 | -2864 |
| 94 | I/O | 3453 | -2744 |
| 95 | I/O | 3453 | -2419 |
| 96 | I/O | 3453 | -2303 |
| 97 | I/O | 3453 | -2188 |
| 98 | I/O | 3453 | -2072 |
| 99 | I/O | 3453 | -1957 |
| 100 | I/O | 3453 | -1842 |
| 101 | GND | 3453 | -1699 |
| 102 | I/O | 3453 | -1556 |
| 103 | I/O | 3453 | -1440 |
| 104 | I/O | 3453 | -1325 |
| 105 | I/O | 3453 | -1210 |
| 106 | GND | 3453 | -1077 |
| 107 | I/O | 3453 | -936 |
| 108 | I/O | 3453 | -808 |
| 109 | VKS, GND | 3453 | -453 |
| 110 | VPP, VCC | 3453 | -78 |
| 111 | GND | 3453 | 77 |
| 112 | VCCI | 3453 | 260 |
| 113 | VSV, VCC | 3453 | 414 |
| 114 | I/O | 3453 | 542 |
| 115 | I/O | 3453 | 669 |
| 116 | VCCI | 3453 | 811 |
| 117 | I/O | 3453 | 946 |
| 118 | I/O | 3453 | 1066 |
| 119 | I/O | 3453 | 1186 |
| 120 | I/O | 3453 | 1307 |
| 121 | GND | 3453 | 1442 |
| 122 | I/O | 3453 | 1587 |
| 123 | I/O | 3453 | 1718 |
| 124 | I/O | 3453 | 1849 |
| 125 | I/O | 3453 | 1980 |
| 126 | GND | 3453 | 2138 |
| 127 | I/O | 3453 | 2296 |
| 128 | I/O | 3453 | 2427 |
| 129 | I/O | 3453 | 2558 |
| 130 | I/O | 3453 | 2673 |
| 131 | I/O | 3453 | 2948 |
| 132 | I/O | 3453 | 3354 |

| Pad # | Name | X Coords | Y Coords |
|---|---|---|---|
| 133 | GND | 3182 | 3625 |
| 134 | I/O | 2851 | 3625 |
| 135 | SDI, I/O | 2735 | 3625 |
| 136 | I/O | 2620 | 3625 |
| 137 | I/O | 2505 | 3625 |
| 138 | I/O | 2373 | 3625 |
| 139 | I/O | 2243 | 3625 |
| 140 | VCC | 2086 | 3625 |
| 141 | I/O | 1928 | 3625 |
| 142 | I/O | 1798 | 3625 |
| 143 | I/O | 1668 | 3625 |
| 144 | I/O | 1538 | 3625 |
| 145 | GND | 1380 | 3625 |
| 146 | I/O | 1222 | 3625 |
| 147 | I/O | 1092 | 3625 |
| 148 | I/O | 962 | 3625 |
| 149 | I/O | 832 | 3625 |
| 150 | I/O | 702 | 3625 |
| 151 | I/O | 572 | 3625 |
| 152 | PRA, I/O | 442 | 3625 |
| 153 | I/O | 299 | 3625 |
| 154 | CLKA, I/O | 169 | 3625 |
| 155 | VCC | 39 | 3625 |
| 156 | GND | -106 | 3625 |
| 157 | I/O | -286 | 3625 |
| 158 | CLKB, I/O | -436 | 3625 |
| 159 | I/O | -586 | 3625 |
| 160 | PRB, I/O | -748 | 3625 |
| 161 | I/O | -898 | 3625 |
| 162 | I/O | -1048 | 3625 |
| 163 | I/O | -1198 | 3625 |
| 164 | I/O | -1347 | 3625 |
| 165 | GND | -1525 | 3625 |
| 166 | I/O | -1702 | 3625 |
| 167 | I/O | -1852 | 3625 |
| 168 | I/O | -2002 | 3625 |
| 169 | I/O | -2152 | 3625 |
| 170 | VCC | -2329 | 3625 |
| 171 | I/O | -2500 | 3625 |
| 172 | I/O | -2638 | 3625 |
| 173 | I/O | -2754 | 3625 |
| 174 | I/O | -2869 | 3625 |
| 175 | DCLK, I/O | -2984 | 3625 |
| 176 | I/O | -3182 | 3625 |

Note: 1. All dimensions in micrometer
2. The die center is the coordinate origin (0,0).
3. VSV, VKS and Vpp pins are used for programming. For normal operation, these pins should be connected to Vcc or GND as shown.

Figure A-4. A1280XL(0.6µm) Bond Pad Locations and Functions - Continued.

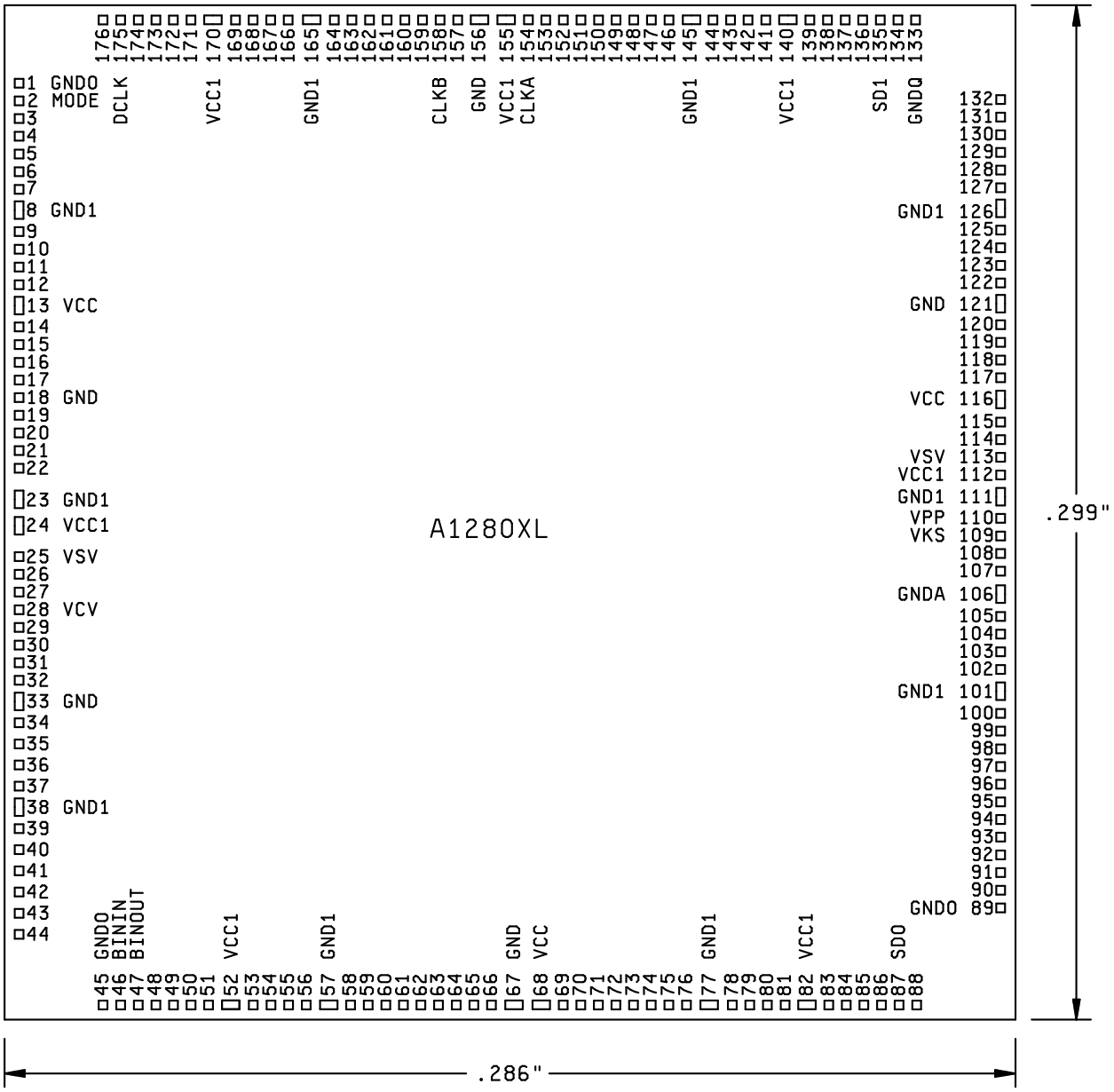



Figure A-4. A1280XL(0.6µm) Bond Pad Locations and Functions - Continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 12-04-10

Approved sources of supply for SMD 5962-92156 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

| Standard microcircuit 1/ drawing PIN | Vendor CAGE number | Vendor similar 3/ PIN |
|---|---|---|
| 5962-9215601MXC | 0J4Z0<br>2/ | A1280A-PG176B<br>TPC1280MGB176B |
| 5962-9215601MYC | 0J4Z0<br>2/ | A1280A-CQ172B<br>TPC1280MHFG172B |
| 5962-9215601MXA | 0J4Z0 | A1280A-PG176B |
| 5962-9215601MYA | 0J4Z0 | A1280A-CQ172B |
| 5962-9215601MZC | 2/<br>2/ | A1280A-PG177B<br>TPC1280MGB177B |
| 5962-9215601MUC | 2/ | RP1280A-CQ172B |
| 5962-9215601Q9A | 0J4Z0 | A1280A-DIE |
| 5962-9215601Q9B | 0J4Z0 | A1280A-DIE |
| 5962-9215602MXC | 0J4Z0<br>2/ | A1280A-1PG176B<br>TPC1280MGB176B-1 |
| 5962-9215602MYC | 0J4Z0<br>2/ | A1280A-1CQ172B<br>TPC1280MHFG172B-1 |
| 5962-9215602MXA | 0J4Z0 | A1280A-1PG176B |
| 5962-9215602MYA | 0J4Z0 | A1280A-1CQ172B |
| 5962-9215602MZC | 2/<br>2/ | A1280A-1PG177B<br>TPC1280MGB177B-1 |
| 5962-9215602MUC | 2/ | RP1280A-1CQ172B |
| 5962F9215603QYC | 2/ | RH1280-CQ172V |
| 5962F9215603Q9C | 2/ | RH1280-DIE |
| 5962-9215604QXC | 2/ | A1280XL-PG176B |
| 5962-9215604QYC | 2/ | A1280XL-CQ172B |
| 5962-9215604Q9C | 2/ | A1280XL-DIE |
| 5962-9215605QXC | 2/ | A1280XL-1PG176B |
| 5962-9215605QYC | 2/ | A1280XL-1CQ172B |
| 5962R9215606QYC | 1RU44 | 197A806-35 |
| 5962R9215607QYC | 1RU44 | 197A806-34 |

See footnotes at end of table

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.
2/ No longer available from an approved source.
3/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 0J4Z0 | Actel<br>2061 Stierlin Court.<br>Mountain View, CA 94043 |
| 1RU44 | BAE Systems<br>9300 Wellington Road<br>Manassas, VA 20110-4122 |