REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Delete input offset voltage temperature coefficient test and make change to input voltage range test as specified under TABLE I. In accordance with N.O.R. 5962-R221-94.	94-06-28	M. A. FRYE
B	Make change to terminal connections as specified under FIGURE 3. In accordance with N.O.R. 5962-R167-95.	95-07-07	M. A. FRYE
C	Add device type 03. Add case outline H. Add TABLE IIB. Replace CAGE code 34031 with CAGE code 24355. Make changes to 1.2.2, 1.2.4, 1.3, TABLE I, and TABLE II. Redrawn.	97-06-27	R. MONNIN
D	Replace reference to MIL-STD-973 with reference to MIL-PRF-38535. - ro	07-07-23	R. HEBER

REV																				
SHEET																				
REV	D	D																		
SHEET	15	16																		

REV STATUS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
CHARLES E. BESORE

APPROVED BY
MICHAEL A. FRYE

DRAWING APPROVAL DATE
93-05-24

MICROCIRCUIT, LINEAR, HIGH SPEED, VOLTAGE COMPARATOR WITH LATCH, MONOLITHIC SILICON

REVISION LEVEL	SIZE	CAGE CODE	
D	A	**67268**	**5962-92347**

SHEET 1 OF 16

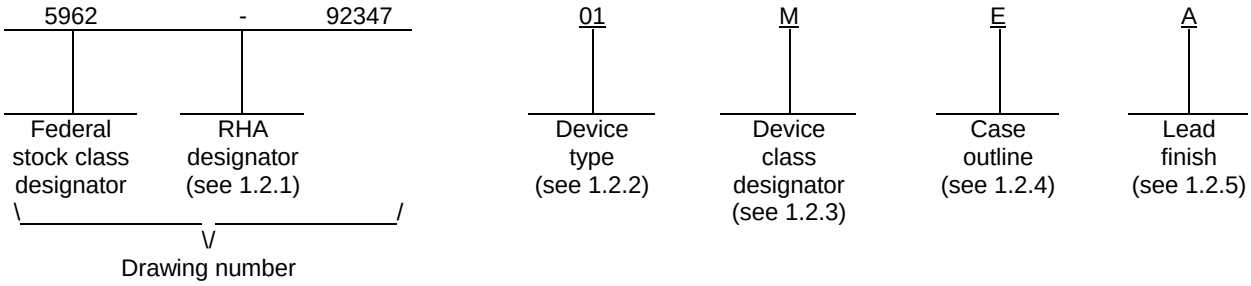
DSCC FORM 2233
APR 97

5962-E491-07

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	AD9696	Single voltage comparator with latch
02	AD9698	Dual voltage comparator with latch
03	AD9696	Single voltage comparator with latch

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
H	GDFP1-F10 or CDFP2-F10	10	Flat pack
I	MACY1-X10	10	Can
P	GDIP1-T8 or CDIP2-T8	8	Dual-in-line
X	See figure 1	8	Dual small outline with gullwing leads
Y	See figure 2	16	Dual small outline with gullwing leads

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage range ($\pm V_S$) ..... ±7 V dc
Input voltage range (V_{IN}) ..... ±5 V
Differential input voltage ..... 5.4 V
Latch enable voltage range ..... -0.5 V to $+V_S$
Output current (continuous) ..... 20 mA
Power dissipation (P_D) ..... 600 mW
Lead temperature (soldering 10 seconds) ..... +300°C
Storage temperature range ..... -65°C to +150°C
Junction temperature (T_J) ..... +175°C
Thermal resistance, junction-to-ambient (θ_{JA}):
  Cases E and Y ..... 90°C/W
  Case H ..... 140°C/W
  Case I ..... 170°C/W
  Cases P and X ..... 110°C/W
Thermal resistance, junction-to-case (θ_{JC}):
  Cases E, I, and P ..... See MIL-STD-1835
  Case H ..... 60°C/W
  Case X ..... 20°C/W
  Case Y ..... 25°C/W

1.4 Recommended operating conditions.

Supply voltage range ($\pm V_S$) ..... ±5 V dc
Ambient operating temperature range (T_A) ..... -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figures 1 and 2.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 3.

3.2.4 Timing diagram. The timing diagram shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 50 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit
					Min	Max	
Input characteristics							
Input offset voltage	V_{IO}	$R_S \le 100\ \Omega$	1	All		2.0	mV
			2,3			3.0	
Input bias current	I_{IB}		1	All		55	µA
			2,3			110	
Input offset current	I_{IO}		1	All		1.0	µA
			2,3			1.3	
Input voltage range	V_{IN}	$V_S = \pm 5$ V	1,2,3	All	-2.0	+3.5	V
		$V_S = +5$ V			+1.6	+3.5	
Common mode rejection ratio	CMRR	$V_S = \pm 5$ V	1,2,3	All	80		dB
		$V_S = +5$ V			57		
Latch enable input							
Logic “1” voltage threshold	V_{TH}		1,2,3	All	2.0		V
Logic “0” voltage threshold	V_{TH}		1,2,3	All		0.8	V
Logic “1” current	$I_{(LE)}$		1,2,3	All		10	µA
Logic “0” current	$I_{(LE)}$		1,2,3	All		1	µA
Digital outputs							
Logic “1” voltage	V_{OUT}	Source at 4 mA	1,2,3	All	2.7		V
Logic “0” voltage	V_{OUT}	Sink at 4 mA	1,2,3	All		0.5	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit
					Min	Max	
Switching performance							
Propagation delay, input to output high	t_{PD}	3/ 4/	9,10,11	01,02		7.0	ns
			9	03		7.0	
Propagation delay, input to output low	t_{PD}	3/ 4/	9,10,11	01,02		7.0	ns
			9	03		7.0	
Propagation delay, latch enable to output high	$t_{PD(E)}$	$T_A = +25°C$ 3/ 4/	9	All		8.5	ns
Propagation delay, latch enable to output low	$t_{PD(E)}$	$T_A = +25°C$ 3/ 4/	9	All		8.5	ns
Propagation delay, delta delay between outputs	$t_{PD\Delta}$	$T_A = +25°C$ 3/ 4/	9	All		1.5	
Propagation delay dispersion	t_{PDD}	100 mV to 1.0 V overdrive, $T_A = +25°C$ 3/ 4/	9	All		200	ps
Latch enable, pulse width	$t_{PW(E)}$	$T_A = +25°C$ 4/	9	All	3.5		ns
Latch enable, setup time	t_S	$T_A = +25°C$ 4/	9	All	3		ns
Latch enable, hold time	t_H	$T_A = +25°C$ 4/	9	All	3		ns
Power supply 5/							
Positive supply current	$+I_S$	$V_S = +5$ V and ± 5 V	1,2,3	01,03		32	mA
				02		64	
Negative supply current	$-I_S$	$V_S = \pm 5$ V	1,2,3	01,03		4.0	mA
				02		8.0	
Power supply rejection ratio	PSRR	$+V_S = +4.75$ V to +5.25 V,	4	All	70		dB
		$-V_S = -5.46$ V to -4.94 V	5,6		65		

1/ $+V_S = +5.0$ V and $-V_S = -5.2$ V. See figure 4.

2/ The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum, is used in this table. Negative current shall be defined as conventional current flow out of a device terminal.

3/ Propagation delays are measured with 100 mV pulse and 100 mV overdrive (V_{OD}).

4/ If not tested, shall be guaranteed to the limits specified in table I herein.

5/ Supply voltages should remain stable within ±5% for normal operation

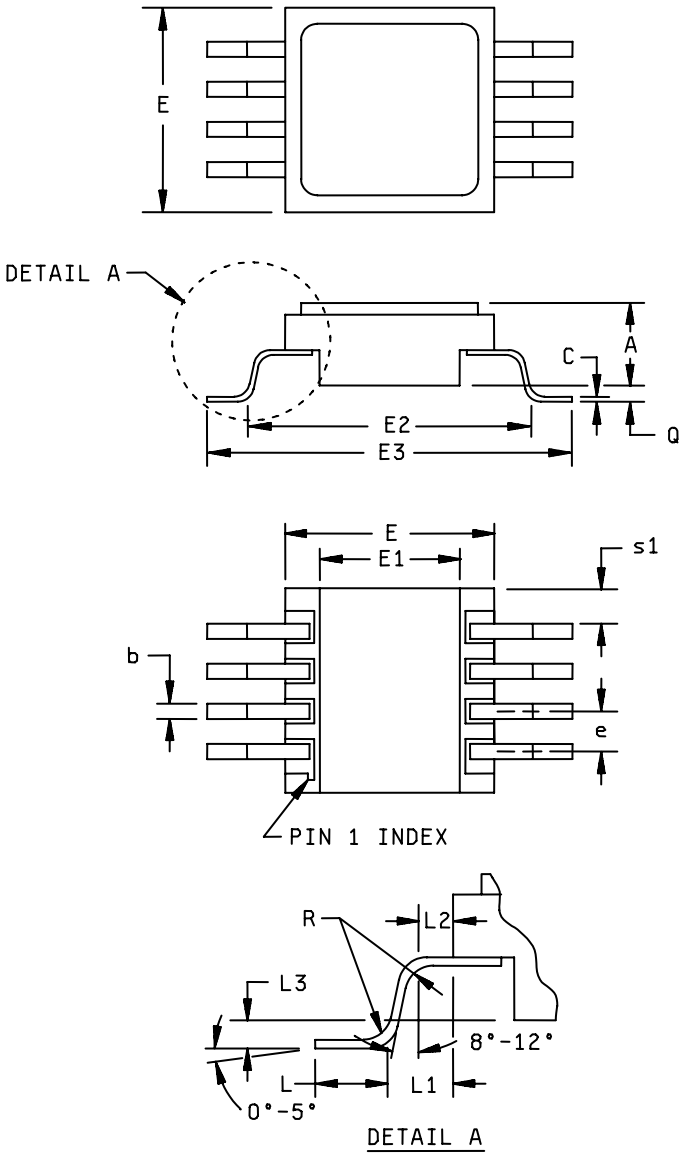


FIGURE 1. Case outline X.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.11	2.62	0.083	0.103
b	0.38	0.48	0.015	0.019
c	0.10	0.13	0.004	0.005
E	6.35	6.60	0.250	0.260
E1	4.44	---	0.175	---
E2	8.20	8.81	0.323	0.347
E3	11.00	11.61	0.433	0.457
e	1.27 BSC		0.050 BSC	
L	1.02	1.14	0.040	0.045
L1	1.40	1.68	0.055	0.066
L2	0.64	0.76	0.025	0.030
L3	0.38	0.51	0.015	0.020
R	0.38	0.51	0.015	0.020
S1	1.12	---	0.044	---
Q	0.38	---	0.015	---
N	8		8	

NOTES:
1. The case outline X was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound shall take precedence.
2. Pin 1 is identified by a tab on the braze pad on the underside of the package.
3. Lead finish shall be hot solder dipped, or gold plated with nickel underplate. The lead material is alloy 42.
4. The lid is gold plated Kovar with nickel underplate.

FIGURE 1. Case outline X – Continued.

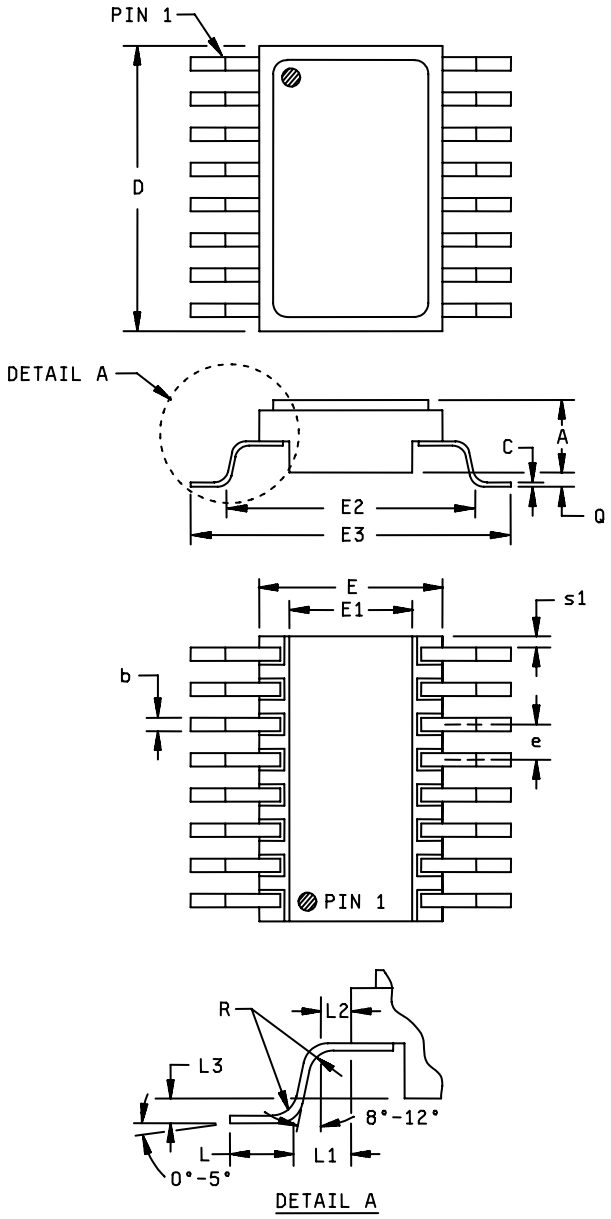


FIGURE 2. Case outline Y.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.11	2.62	0.083	0.103
b	0.38	0.48	0.015	0.019
c	0.10	.015	0.004	0.006
D	9.93	10.29	0.391	0.405
E	6.32	6.63	0.249	0.261
E1	4.44	---	0.175	---
E2	8.20	8.81	0.323	0.347
E3	11.00	11.61	0.433	0.457
e	1.27 BSC		0.050 BSC	
L	1.02	1.14	0.040	0.045
L1	1.40	1.68	0.055	0.066
L2	0.64	0.76	0.025	0.030
L3	0.38	0.51	0.015	0.020
R	0.38	0.51	0.015	0.020
S1	0.13	---	0.005	---
Q	0.38	---	0.015	---
N	16		16	

NOTES:
1. The case outline Y was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound shall take precedence.
2. Pin 1 is identified by a tab on the braze pad on the underside of the package.
3. Lead finish shall be hot solder dipped, or gold plated with nickel underplate. The lead material is alloy 42.
4. The lid is gold plated Kovar with nickel underplate.

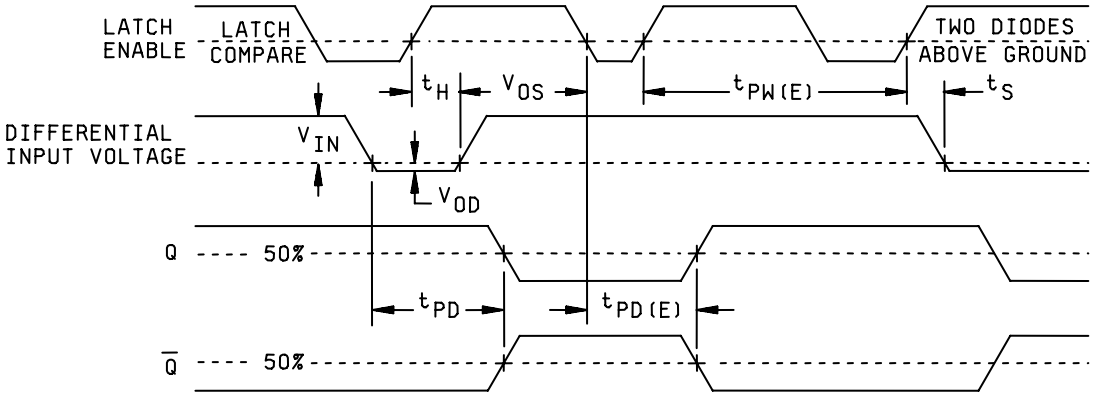
FIGURE 2. Case outline Y – Continued.

Device types	01		02		03	
Case outlines	I	P and X	E	Y	H	P
Terminal number	Terminal symbol					
1	$+V_S$	$+V_S$	$Q1_{OUT}$	NC	NC	$+V_S$
2	NC	+INPUT	$\overline{Q1}_{OUT}$	$-V_S$	$+V_S$	+INPUT
3	+INPUT	-INPUT	GROUND	-INPUT 1	+INPUT	-INPUT
4	-INPUT	$-V_S$	LATCH ENABLE 1	+INPUT 1	-INPUT	$-V_S$
5	$-V_S$	LATCH ENABLE	NC	+INPUT 2	$-V_S$	LATCH ENABLE
6	LATCH ENABLE	GROUND	$-V_S$	-INPUT 2	LATCH ENABLE	GROUND
7	GROUND	Q_{OUT}	-INPUT 1	$+V_S$	GROUND	Q_{OUT}
8	Q_{OUT}	$\overline{Q}_{OUT}$	+INPUT 1	NC	Q_{OUT}	$\overline{Q}_{OUT}$
9	$\overline{Q}_{OUT}$	---	+INPUT 2	LATCH ENABLE 2	$\overline{Q}_{OUT}$	---
10	NC	---	-INPUT 2	GND	NC	---
11	---	---	$+V_S$	$\overline{Q2}_{OUT}$	---	---
12	---	---	NC	$Q2_{OUT}$	---	---
13	---	---	LATCH ENABLE 2	$Q1_{OUT}$	---	---
14	---	---	GROUND	$\overline{Q1}_{OUT}$	---	---
15	---	---	$\overline{Q2}_{OUT}$	GND	---	---
16	---	---	$Q2_{OUT}$	LATCH ENABLE 1	---	---

FIGURE 3. Terminal connections.

Terminal symbol	Description
$Q1_{OUT}$	One of two complementary outputs. $Q1_{OUT}$ will be at logic high if voltage at +INPUT 1 is greater than voltage at –INPUT 1 at LATCH ENABLE 1 is at logic low.
$\overline{Q1}_{OUT}$	One of two complementary outputs. $\overline{Q1}_{OUT}$ will be at logic high if voltage at -INPUT 1 is greater than voltage at +INPUT 1 at LATCH ENABLE 1 is at logic low.
GROUND	Analog and digital ground.
LATCH ENABLE 1	Output at $Q1_{OUT}$ will track differential changes at the inputs when LATCH ENABLE 1 is at logic low. When LATCH ENABLE 1 is at logic high, the output at $Q1_{OUT}$ will reflect the input state at the application of the latch command, delayed by the LATCH ENABLE SETUP TIME (t_S).
NC	No connection.
$-V_S$	Negative power supply.
-INPUT 1	Inverting input of differential input stage for comparator 1.
+INPUT 1	Noninverting input of differential input stage for comparator 1.
+INPUT 2	Noninverting input of differential input stage for comparator 2.
-INPUT 2	Inverting input of differential input stage for comparator 2.
$+V_S$	Positive power supply.
LATCH ENABLE 2	Output at $Q2_{OUT}$ will track differential changes at the inputs when LATCH ENABLE 2 is at logic low. When LATCH ENABLE 2 is at logic high, the output at $Q2_{OUT}$ will reflect the input state at the application of the latch command, delayed by the LATCH ENABLE SETUP TIME (t_S).
$\overline{Q2}_{OUT}$	One of two complementary outputs. $\overline{Q2}_{OUT}$ will be at logic high if voltage at -INPUT 2 is greater than voltage at +INPUT 2 at LATCH ENABLE 2 is at logic low.
$Q2_{OUT}$	One of two complementary outputs. $Q2_{OUT}$ will be at logic high if voltage at +INPUT 2 is greater than voltage at -INPUT 2 at LATCH ENABLE 2 is at logic low.

FIGURE 3. Terminal connections – Continued.



NOTES:

1. LATCH ENABLE. Logic high voltage ≥ 2.0 V and logic low voltage ≤ 0.8 V.
2. DIFFERENTIAL INPUT VOLTAGE. Differential input signal ≤ 5.40 V, V_{IN} maximum = ±5 V, V_{IH} ≤ +5.0 V, and V_{IL} ≥ -5.0 V.

FIGURE 4. Timing waveforms.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	1,2,3,4,5,6 1/ 9,10,11	1,2,3,4,5,6, 1/ 9,10,11	1,2,3, 1/ 2/ 5,6,9,10,11
Group A test requirements (see 4.4)	1,2,3,4,5,6,9,10,11	1,2,3,4,5,6, 9,10,11	1,2,3,4,5,6, 9,10,11
Group C end-point electrical parameters (see 4.4)	1	1	1 2/
Group D end-point electrical parameters (see 4.4)	1	1	1
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1.
2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be completed with reference to the previous interim electrical parameters.

TABLE IIB. 240 hour burn-in and Group C and point electrical parameters.

Test	Symbol	240 hour limits +25°C			1000 hour limits	Limits
		Endpoint		Delta	Delta	
		MIn	Max	Min	Max	
Input offset voltage	V_{OS}		±2.0	1.5	1.9	mV
Input offset current	I_{OS}		±1	0.7	0.9	µA

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 07-07-23

Approved sources of supply for SMD 5962-92347 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9234701MIA	3/	AD9696TH/883B
5962-9234701MPA	3/	AD9696TQ/883B
5962-9234701MXA	3/	AD9696TZ/883B
5962-9234702MEA	3/	AD9698TQ/883B
5962-9234702MYA	3/	AD9698TZ/883B
5962-9234703VHA	3/	AD9696TL/QMLV
5962-9234703VPA	3/	AD9696TQ/QMLV

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply. The last known supplier is listed below.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 7910 Triad Center Drive Greensboro, NC 27409-9605