REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R366-97	97-06-25	Monica L. Poelking
B	Changes in accordance with NOR 5962-R112-98	98-05-22	Monica L. Poelking
C	Update boilerplate to MIL-PRF-38535 requirements. - CFS	05-10-17	Thomas M. Hess

REV																				
SHEET																				
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED
Thomas M. Hess

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Thomas M. Hess

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
96-07-11

REVISION LEVEL
C

MICROCIRCUIT, DIGITAL, 32-BIT MICROPROCESSOR, MONOLITHIC SILICON

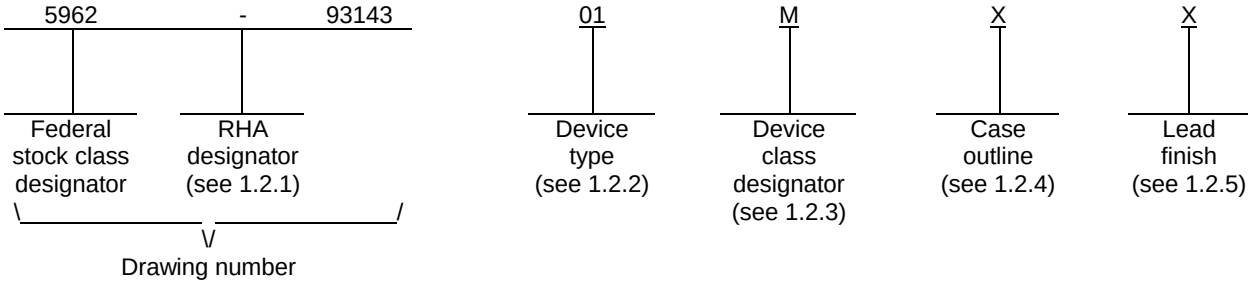
SIZE	CAGE CODE	
A	**67268**	**5962-93143**

SHEET 1 OF 34

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	68040-25	32-bit microprocessor
02	68020-33	32-bit microprocessor

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA10-179	179	Pin grid array
Y	See figure 1	196	Leaded chip carrier with non-conductive tie bar
Z	See figure 1	196	Ceramic leaded chip carrier, gull-wing lead

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.3 V dc to +7.0 V dc
Input voltage range (V_{IN})	-0.8 V dc to +7.0 V dc
Storage temperature range (T_{STG})	-65°C to +150°C
Maximum power dissipation (P_D):	
Large buffers enabled	7.7 W
Small buffers enabled	6.3 W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case X	+1.0°C/W
Case Y	+1.0°C/W
Case Z	+1.0°C/W

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.75 V dc to +5.25 V dc
Logic high input voltage range (V_{IH})	+2.0 V dc to V_{CC} + 0.3 V dc
Logic low input voltage range (V_{IL})	GND - 0.3 V dc to 0.8 V dc
Minimum high level output voltage (V_{OH})	2.4 V dc
Maximum low level output voltage (V_{OL})	0.5 V dc
Frequency of operation (f_{OP}):	
Device 01	25 MHz
Device 02	33 MHz
Case operating temperature range (T_C)	-55°C to T_J max
Maximum operating junction temperature (T_J)	+125°C 2/
Minimum operating case temperature (T_C)	-55°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ This device is not tested at T_C = +125°C. Testing is performed by setting the junction temperature T_J = +125°C and allowing the case and ambient temperatures to rise and fall as necessary so as not to exceed the maximum junction temperature.

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation.

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture.

(Copies of these documents are available from the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, Piscataway, NJ 08854-4150.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Switching test circuit and waveforms. The switching test circuit and waveforms shall be as specified on figure 4.

3.2.5 Boundary scan instruction codes. The boundary scan instruction codes shall be as specified on figure 5.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

3.11 IEEE 1149.1 compliance. All device types shall be compliant to IEEE 1149.1.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_C \le T_J$ max V_{CC} min $\le V_{CC} \le V_{CC}$ max unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input high voltage	V_{IH}		1,2,3	All	2.0	V_{CC}	V
Input low voltage	V_{IL}		1,2,3	All	GND	0.8	V
Undershoot voltage	V_U		1,2,3	All		-0.8	V
Supply current	I_{CC}	$V_{CC} = V_{CC}$ max 4/ 100% large buffer	1,2,3	All		1.47	A
		$V_{CC} = V_{CC}$ max 4/ 100% small buffer				1.20	
Input leakage current, AVEC, BCLK, BG, CDIS, IPLn, MDIS, PCLK, RSTI, SCn, TBI, TCI, TCK, TEA	I_{IN}	V_{IN} = 2.4 V/0.5 V $V_{CC} = V_{CC}$ max	1,2,3	All	-20	20	µA
High impedance (off-state) leakage current, An, BB, CIOUT, Dn, LOCK, LOCKE, R/W, SIZn, TA, TDO, TIP, TLNn, TMn, TS, TTn, UPAn	I_{TSI}	V_{IN} = 2.4 V/0.5 V $V_{CC} = V_{CC}$ max	1,2,3	All	-20	20	µA
Signal low input current, TMS, TDI, TRST	I_{IL}	V_{IL} = 0.8 V $V_{CC} = V_{CC}$ max	1,2,3	All	-1.1	-0.18	mA
Signal high input current, TMS, TDI, TRST	I_{IH}	V_{IH} = 2.0 V $V_{CC} = V_{CC}$ max	1,2,3	All	-0.94	-0.16	mA
Output high voltage	V_{OH}	Large buffers, I_{OH} = 35 mA, $V_{CC} = V_{CC}$ min	1,2,3	All	2.4		V
		Small buffers, I_{OH} = 5.0 mA, $V_{CC} = V_{CC}$ min			2.4		
Output low voltage	V_{OL}	Large buffers, I_{OL} = 35 mA, $V_{CC} = V_{CC}$ min	1,2,3	All		0.5	V
		Small buffers, I_{OL} = 5.0 mA, $V_{CC} = V_{CC}$ min				0.5	
Input capacitance	C_{IN}	V_{IN} = 0 V, f = 1.0 MHz, T_A = +25 C, see 4.4.1c	4	All		25	pF
Functional testing		$V_{CC} = V_{CC}$ min, see 4.4.1b	7,8	All			
Frequency of operation	f_{MAX}	$V_{CC} = V_{CC}$ min	9,10,11	01	20	25	MHz
				02	20	33	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_C \le T_J$ max V_{CC} min $\le V_{CC} \le V_{CC}$ max unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Clock timing							
PCLK cycle time	1	See figure 4. $V_{CC} = V_{CC}$ min	9,10,11	01	20	25	ns
				02	15	25	
PCLK rise time 5/	2		9,10,11	01, 02		1.7	ns
PCLK fall time 5/	3		9,10,11	01, 02		1.6	ns
PCLK duty cycle (measured from 1.5 V to 1.5 V 5/	4		9,10,11	01	47.5	52.5	%
				02	46.67	53.33	
PCLK pulse width high (measured from 1.5 V to 1.5 V for 25 MHz) 5/	4a		9,10,11	01	9.5	10.5	ns
				02	7	8	
PCLK pulse width low (measured from 1.5 V to 1.5 V for 25 MHz) 5/	4b		9,10,11	01	9.5	10.5	ns
				02	7	8	
BCLK cycle time	5		9,10,11	01	40	50	ns
				02	30	60	
BCLK rise and fall time	6, 7		9,10,11	01		4.0	ns
				02		3.0	
BCLK duty cycle (measured from 1.5 V to 1.5 V) 5/	8		9,10,11	01, 02	40	60	%
BCLK pulse width high (measured from 1.5 V to 1.5 V) 5/	8a		9,10,11	01	16	24	ns
				02	12	18	
BCLK pulse width low (measured from 1.5 V to 1.5 V) 5/	8b		9,10,11	01	16	24	ns
				02	12	18	
PCLK, BCLK frequency stability 5/	9		9,10,11	01, 02		1000	ppm
PCLK to BCLK skew	10		9,10,11	01		9.0	ns
				02		n/a	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_C \le T_J$ max V_{CC} min $\le V_{CC} \le V_{CC}$ max unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Output timing								
BCLK to address CIOUT, LOCK, LOCKE, R/W, SIZn, TLN, TMn, TTn, and UPAn valid 6/	11	See figure 4 $V_{CC} = V_{CC}$ min	Large buffer 7/	9,10,11	01	9.0	21	ns
					02	6.5	18	
			Small buffer 7/		01	9.0	30	
					02	6.5	25	
BCLK to output invalid (output hold)	12		Large buffer 7/	9,10,11	01	9.0		ns
					02	6.5		
			Small buffer 7/		01	9.0		
					02	6.5		
TCLK to TS valid	13		Large buffer 7/	9,10,11	01	9.0	21	ns
					02	6.5	18	
			Small buffer 7/		01	9.0	30	
					02	6.5	25	
BCLK to TIP valid	14		Large buffer 7/	9,10,11	01	9.0	21	ns
					02	6.5	18	
			Small buffer 7/		01	9.0	30	
					02	6.5	25	
BCLK to data-out valid 8/	18		Large buffer 7/	9,10,11	01	9.0	23	ns
					02	6.5	20	
			Small buffer 7/		01	9.0	32	
					02	6.5	27	
BCLK to data-out invalid (output hold) 8/	19		Large buffer 7/	9,10,11	01	9.0		ns
					02	6.5		
			Small buffer 7/		01	9.0		
					02	6.5		
BCLK to output low impedance 6/ 8/	20		Large buffer 7/	9,10,11	01	9.0		ns
					02	6.5		
			Small buffer 7/		01	9.0		
					02	6.5		
BCLK to data-out high impedance 9/	21		Large buffer 7/	9,10,11	01	9.0	20	ns
					02	6.5	17	
			Small buffer 7/		01	9.0	20	
					02	6.5	17	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_C \le T_J$ max V_{CC} min $\le V_{CC} \le V_{CC}$ max unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Output timing - Continued.								
BCLK to multiplexed address valid 6/	26	See figure 4 $V_{CC} = V_{CC}$ min	Large buffer 7/	9,10,11	01	19	31	ns
					02	14	26	
			Small buffer 7/		01	19	40	
					02	14	33	
BCLK to multiplexed address driven	27 6/ 9/		Large buffer 7/	9,10,11	01	19		ns
					02	14		
			Small buffer 7/		01	19		
					02	14		
BCLK to multiplexed address high impedance 6/ 8/ 9/	28		Large buffer 7/	9,10,11	01	9.0	18	ns
					02	6.5	15	
			Small buffer 7/		01	9.0	18	
					02	6.5	15	
BCLK to multiplexed data driven 6/ 9/	29		Large buffer 7/	9,10,11	01	19	33	ns
					02	14	20	
			Small buffer 7/		01	19	33	
					02	14	20	
BCLK to multiplexed data valid 8/	30		Large buffer 7/	9,10,11	01	19	33	ns
					02	14	28	
			Small buffer 7/		01	19	42	
					02	14	35	
BCLK to address CIOUT, LOCK, LOCKE, R/W, SIZn, TS, TLNn, TMn, TTn, and UPAn high impedance 6/	38	See figure 4. $V_{CC} = V_{CC}$ min	Large buffer 7/	9,10,11	01	9.0	18	ns
					02	6.5	15	
			Small buffer 7/		01	9.0	18	
					02	6.5	15	
BCLK to BB, TA, and TIP high impedance	39		Large buffer 7/	9,10,11	01	19	28	ns
					02	14	23	
			Small buffer 7/		01	19	28	
					02	14	23	
BCLK to BR and BB valid	40		Large buffer 7/	9,10,11	01	9.0	21	ns
					02	6.5	18	
			Small buffer 7/		01	9.0	30	
					02	6.5	25	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_C \le T_J$ max V_{CC} min $\le V_{CC} \le V_{CC}$ max unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Output timing - Continued.								
BCLK to MI valid	43	See figure 4. $V_{CC} = V_{CC}$ min	Large buffer 7/	9,10,11	01	9.0	21	ns
					02	6.5	18	
			Small buffer 7/		01	9.0	30	
					02	6.5	25	
BCLK to TA valid	48		Large buffer 7/	9,10,11	01	9.0	21	ns
					02	6.5	18	
			Small buffer 7/		01	9.0	30	
					02	6.5	25	
BCLK to IPEND, PSTn and RSTO valid	50		Large buffer 7/	9,10,11	01	9.0	21	ns
					02	6.5	18	
			Small buffer 7/		01	9.0	30	
					02	6.5	25	
Input timing								
Data-in valid to BCLK (setup)	15	See figure 4. $V_{CC} = V_{CC}$ min		9,10,11	01	5.0		ns
					02	4.0		
BCLK to data-in invalid (Hold)	16			9,10,11	01,02	4.0		ns
BCLK to data-in high impedance (read followed by write)	17			9,10,11	01		49	ns
					02		36.5	
TA valid to BCLK (setup)	22a			9,10,11	01,02	10		ns
TEA valid to BCLK (setup)	22b			9,10,11	01,02	10		ns
TCI valid to BCLK (setup)	22c			9,10,11	01,02	10		ns
TBI valid to BCLK (setup)	22d			9,10,11	01	11		ns
					02	10		
BCLK to TA, TEA, TCI, and TBI invalid (hold)	23			9,10,11	01,02	2.0		ns
AVEC valid to BCLK (setup)	24			9,10,11	01,02	5.0		ns
BCLK to AVEC invalid (hold)	25			9,10,11	01,02	2.0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_C \le T_J$ max V_{CC} min $\le V_{CC} \le V_{CC}$ max unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input timing - Continued.							
DLE width high	31	See figure 4.	9,10,11	01,02	8.0		ns
Data-in valid to DLE (setup)	32	$V_{CC} = V_{CC}$ min	9,10,11	01,02	2.0		ns
DLE to data-in valid (hold)	33		9,10,11	01,02	8.0		ns
BCLK to DLE hold	34		9,10,11	01,02	3.0		ns
DLE high to BCLK	35		9,10,11	01	16		ns
				02	12		
Data-in valid to BCLK (DLE mode setup)	36		9,10,11	01,02	5.0		ns
BCLK to data-in invalid (DLE mode hold)	37		9,10,11	01,02	4.0		ns
BB valid to BCLK (setup)	41a		9,10,11	01,02	7.0		ns
BG valid to BCLK (setup)	41b		9,10,11	01	8.0		ns
				02	7.0		
CDIS and MDIS valid to BCLK (setup)	41c		9,10,11	01	10		ns
				02	8		
IPLn valid to BCLK (setup)	41d		9,10,11	01	4.0		ns
				02	3.0		
BCLK to BB, BG, CDIS, IPLn, and MDIS invalid (hold)	42		9,10,11	01,02	2.0		ns
Address valid to BCLK (setup)	44a		9,10,11	01	8.0		ns
				02	7.0		
SIZn valid to BCLK (setup)	44b		9,10,11	01	12		ns
				02	8		
TTn valid to BCLK (setup)	44c		9,10,11	01	6.0		ns
				02	8.5		
R/W valid to BCLK (setup)	44d		9,10,11	01	6.0		ns
				02	5.0		
SCn valid to BCLK (setup)	44e		9,10,11	01	10		ns
				02	11		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_C \le T_J$ max V_{CC} min $\le V_{CC} \le V_{CC}$ max unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input timing - Continued.							
BCLK to address SIZn, TTn, R/W, and SCn invalid (hold)	45	See figure 4. $V_{CC} = V_{CC}$ min	9,10,11	01,02	2.0		ns
TS valid to BCLK (setup)	46		9,10,11	01	5.0		ns
				02	9.0		
BCLK to TS invalid (hold)	47		9,10,11	01,02	2.0		ns
BCLK to BB high impedance (device assumes bus mastership)	49		9,10,11	01,02		9.0	ns
RSTI valid to BCLK	51		9,10,11	01	5.0		ns
				02	4.0		
BCLK to RSTI invalid	52		9,10,11	01,02	2.0		ns
Mode select setup to RSTI negated 10/	53		9,10,11	01,02	20		ns
RSTI negated to mode select invalid 10/	54		9,10,11	01,02	2.0		ns
JTAG timing							
TCK frequency		$V_{CC} = V_{CC}$ min	9,10,11	01,02	0	10	MHz
TCK cycle time	1		9,10,11	01,02	100		ns
TCK clock pulse width measured at 1.5 V	2		9,10,11	01,02	40		ns
TCK rise and fall times	3		9,10,11	01,02	0	10	ns
$\overline{\text{TRST}}$ setup time to TCK falling edge	4		9,10,11	01,02	40		ns
$\overline{\text{TRST}}$ assert time	5		9,10,11	01,02	100		ns
Boundry scan input data setup time	6		9,10,11	01,02	50		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_C \le T_J$ max V_{CC} min $\le V_{CC} \le V_{CC}$ max unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
JTAG timing - Continued.							
Boundry scan input data hold time	7	$V_{CC} = V_{CC}$ min	9,10,11	01,02	50		ns
TCK to output data valid	8		9,10,11	01,02	0	50	ns
TCK to output high impedance	9		9,10,11	01,02	0	50	ns
TMS, TDI data setup time	10		9,10,11	01,02	20		ns
TMS, TDI data hold time	11		9,10,11	01,02	5		ns
TCK to TDO data valid	12		9,10,11	01,02	0	20	ns
TCK to TDO high impedance	13		9,10,11	01,02	0	20	ns

1/ All testing to be performed using worst-case test conditions unless otherwise specified.
2/ The following pins are active low: AVEC, BG, BS, BR, CDIS, DIQUT, IPEND, IPLO, IPL1, IPL2, LOCK, LOCKE, NDIS, MI, RSTO, RSTI, TA, TBI, TCI, TEA, TIP, TRST, TS, and W of R/W.
3/ Maximum operating junction temperature (T_J) = +125°C. Minimum case operating temperature (T_C) = -55°C. This device is not tested at T_C = +125°C. Testing is performed by setting the junction temperature T_J = +125°C and allowing the case and ambient temperatures to rise and fall as necessary so as not to exceed the maximum junction temperature.
4/ Power dissipation may vary in between limits depending on the application.
5/ If not tested, shall be guaranteed to the limits specified in table I.
6/ Timing parameters 11, 20, and 38 for address bus output timing apply when normal bus operation is selected. Parameters 26, 27, and 28 should be used when the multiplexed bus mode of operation is enabled.
7/ Output timing is specified for a valid signal measured at the pin. Large buffer timing is specified driving a 50Ω transmission line with a length characterized by a 2.5 ns one way propagation delay, terminated through 50Ω to 2.5 V. Large buffer output impedance is 4-12Ω, resulting in incident wave switching for this environment. All large buffer outputs must be terminated to guarantee operation.
Small buffer timing is specified driving an un-terminated 30Ω transmission line with a length characterized by a 2.5 ns one-way propagation delay. Small buffer output impedance is typically 30Ω; the smaller buffer specifications include approximately 5 ns for the signal to propagate the length of the transmission line and back.
8/ Timing parameters 18 and 19 for data bus output timing apply when normal bus operation is selected. Parameters 28 and 29 should be used when the multiplexed bus mode of operation is enabled.
9/ Timing parameters 21, 27, 28, and 29 are measured from BCLK edges. By design the device cannot drive address and data simultaneously during multiplexed operations.
10/ The levels on CDIS, MDIS, and the IPL2-IPL0 signals enable or disable the multiplexed bus mode, data latch enable mode, and driver impedance selection respectively.

Case Y

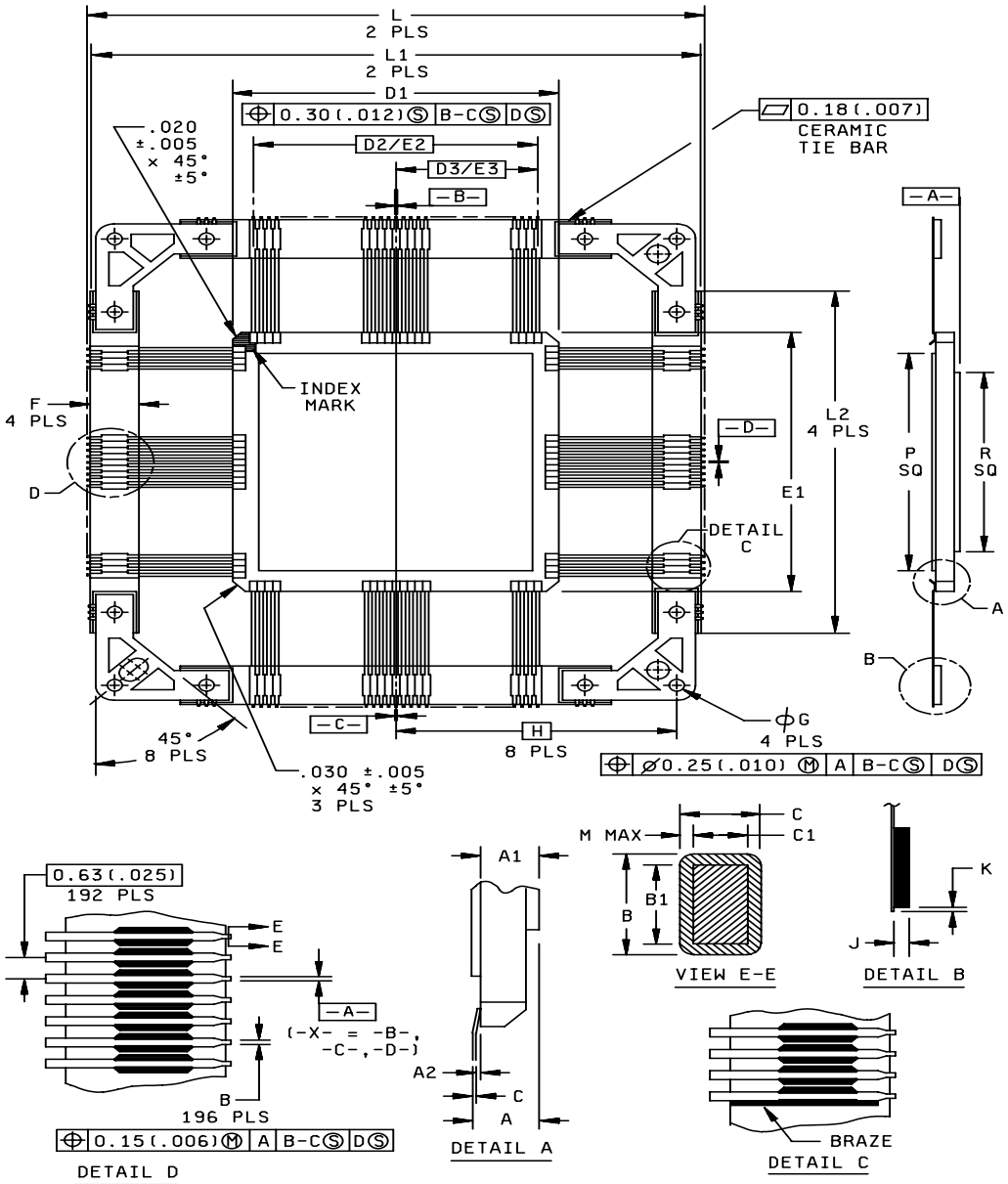


FIGURE 1. Case outlines.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-93143
		REVISION LEVEL C	SHEET 14

Case Y

Dimensions	Millimeters		Inches	
A	2.184	3.302	0.086	0.130
A1	2.032	2.794	0.080	0.110
A2	0.152	0.305	0.006	0.012
B	0.178	0.330	0.007	0.013
B1	0.178	0.254	0.007	0.010
C	0.102	0.229	0.004	0.009
C1	0.102	0.152	0.004	0.006
D1, E1	33.655	34.163	0.325	1.345
D2, E2	30.480 BSC		1.200 BSC	
D3, E3	15.240 BSC		0.600 BSC	
F	4.445	5.715	0.175	0.225
G	1.498	1.549	0.059	0.061
H	2.921 BSC		1.150 BSC	
J	0.762	1.016	0.030	0.040
K	- - -	0.508	- - -	0.020
L	63.500	64.516	2.500	2.540
L1	63.119	63.627	24.85	2.505
L2	42.926	43.434	1.690	1.710
M	- - -	0.038	- - -	0.0015
N	196			
P	28.067	28.575	1.105	1.125
R	22.606	23.114	0.890	0.910
ND	49			

NOTES:

1/ Pin 1 index mark shall be located within the shaded area shown.
2/ Generic lead attach dogleg depiction. May be flat lead configuration
3/ Includes lead attach dogleg height and lid height, whichever is greater.
4/ Dimension N: number of terminals.
5/ Dimension ND: number of terminals per package edge.
6/ Controlling dimensions are in inches.
7/ Dimensions B1 and C1 apply to base metal only. Dimension M applies to the plating thickness.

FIGURE 1. Case outlines - Continued.

Case Z

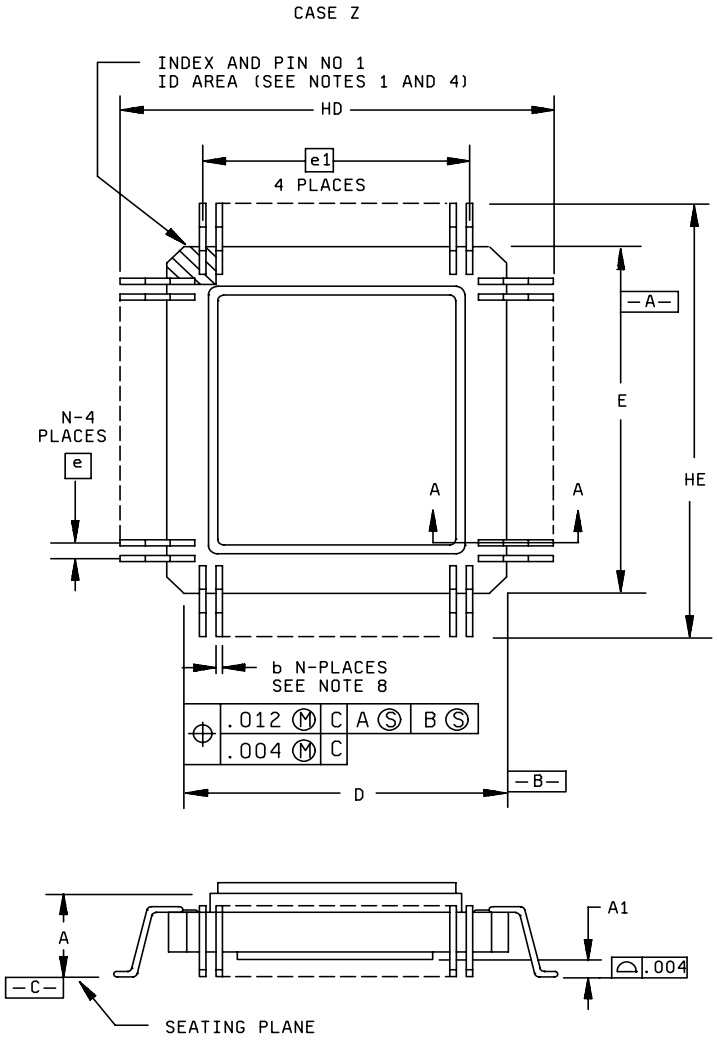
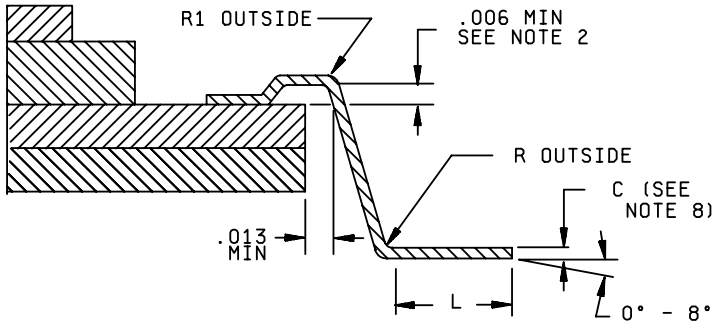


FIGURE 1. Case outlines - Continued.

Case Z



SECTION A-A

Case Z				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		4.19		0.165
A1	0.473	0.873	0.0185	0.0345
b	0.192	0.280	0.0075	0.0110
c	0.102	0.177	0.004	0.007
D/E	33.66	34.16	1.325	1.345
e	.635 BSC		0.025 BSC	
e1	30.35	30.61	1.195	1.205
HD/HE	38.62	38.98	1.521	1.535
L	0.613	1.013	0.024	0.04
N	196		196	
R	0.3	0.8	0.012	0.032
R1	0.23		0.009	

NOTES:

1. A terminal 1 identification mark shall be located at the index corner in the shaded area shown. Terminal 1 is located immediately adjacent to and counterclockwise from the index corner. Terminal numbers increase in a counterclockwise direction when viewed as shown.
2. Generic lead attach dogleg depiction.
3. Dimension N: Number of terminals.
4. Corner shapes (square, notch, radius, etc.) may vary from that shown on the drawing. The index corner shall be clearly unique.
5. Metric equivalents are given for general information only.
6. Controlling dimension: Inch.
7. Datums X and Y to be determined where center leads exit the body.
8. Dimensions b and c include lead finish.

FIGURE 1. Case outlines - Continued.

Case X

Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
A1	A31	C10	V_{CC}	K1	A15	R10	GND
A2	D3	C11	GND	K2	A16	R11	GND
A3	D4	C12	V_{CC}	K3	GND	R12	V_{CC}
A4	D5	C13	GND	K16	GND	R13	GND
A5	D6	C14	V_{CC}	K17	TM2	R14	$\overline{PST2}$
A6	D7	C15	D23	K18	A1	R15	$\overline{TIP}$
A7	D9	C16	D25	L1	A14	R16	TS
A8	D10	C17	V_{CC}	L2	GND	R17	$\overline{V_{CC}}$
A9	D11	C18	D28	L3	GND	R18	$\overline{LOCKE}$
A10	D12	D1	A24	L16	V_{CC}	S1	IPEND
A11	D13	D2	GND	L17	GND	S2	GND
A12	D14	D3	A30	L18	A0	S3	TDI
A13	D15	D16	D27	M1	A13	S4	TCK
A14	D17	D17	GND	M2	V_{CC}	S5	$\overline{TMS}$
A15	D19	D18	D31	M3	V_{CC}	S6	$\overline{MDIS}$
A16	D20	E1	A22	M16	GND	S7	RSTI
A17	D21	E2	A26	M17	V_{CC}	S8	V_{CC}
A18	D24	E3	A28	M18	TM1	S9	GND
B1	A29	E16	D29	N1	A12	S10	$\overline{GND}$
B2	GND	E17	D30	N2	GND	S11	TBI
B3	D1	E18	A8	N3	$\overline{A11}$	S12	$\overline{SC1}$
B4	GND	F1	A21	N16	R/$\overline{W}$	S13	TEA
B5	V_{CC}	F2	GND	N17	GND	S14	PST1
B6	GND	F3	A25	N18	TM0	S15	GND
B7	D8	F16	A9	P1	A10	S16	V_{CC}
B8	GND	F17	GND	P2	TT1	S17	$\overline{GND}$
B9	V_{CC}	F18	A7	P3	TT0	S18	LOCK
B10	GND	G1	A20	P16	SIZ1	T2	$\overline{TDO}$
B11	D16	G2	V_{CC}	P17	SIZ0	T3	TRST
B12	D18	G3	A23	P18	TLN1	T4	$\overline{GND}$
B13	GND	G16	A6	Q1	UPA1	T5	$\overline{CDIS}$
B14	V_{CC}	G17	V_{CC}	Q2	GND	T6	$\overline{IPL2}$
B15	GND	G18	A5	Q3	UPA0	T7	$\overline{IPL1}$
B16	D22	H1	A18	Q16	$\overline{MI}$	T8	$\overline{IPL0}$
B17	GND	H2	GND	Q17	GND	T9	$\overline{DLE}$
B18	D26	H3	V_{CC}	Q18	$\overline{TLN0}$	T10	$\overline{TCI}$
C1	A27	H16	V_{CC}	R1	$\overline{CIOUT}$	T11	AVEC
C2	V_{CC}	H17	GND	R2	$\overline{V_{CC}}$	T12	$\overline{SC0}$
C3	D0	H18	A4	R3	$\overline{RSTO}$	T13	$\overline{BG}$
C4	D2	J1	A17	R4	GND	T14	$\overline{TA}$
C5	V_{CC}	J2	A19	R5	V_{CC}	T15	PST0
C6	GND	J3	V_{CC}	R6	GND	T16	PST3
C7	GND	J16	V_{CC}	R7	BCLK	T17	$\overline{BB}$
C8	V_{CC}	J17	A2	R8	V_{CC}	T18	BR
C9	GND	J18	A3	R9	PCLK		

FIGURE 2. Terminal connections.

Case Y

Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	D0	50	GND	99	GND	148	GND
2	D1	51	GND	100	TIP	149	GND
3	V_{CC}	52	D28	101	PST3	150	IPEND
4	GND	53	D29	102	V_{CC}	151	CIOUT
5	D2	54	V_{CC}	103	PST2	152	V_{CC}
6	D3	55	D30	104	PST1	153	UPA0
7	GND	56	D31	105	GND	154	UPA1
8	D4	57	GND	106	GND	155	GND
9	GND	58	A9	107	PST0	156	TT0
10	GND	59	A8	108	TA	157	TT1
11	D5	60	V_{CC}	109	TEA	158	V_{CC}
12	V_{CC}	61	A7	110	BG	159	GND
13	D6	62	A6	111	SC1	160	A10
14	D7	63	GND	112	SC0	161	A11
15	GND	64	A5	113	GND	162	GND
16	D8	65	A4	114	V_{CC}	163	GND
17	D9	66	V_{CC}	115	TBI	164	A12
18	V_{CC}	67	A3	116	AVEC	165	A13
19	GND	68	A2	117	TCI	166	V_{CC}
20	D10	69	GND	118	GND	167	A14
21	D11	70	A1	119	GND	168	A15
22	GND	71	A0	120	DLE	169	GND
23	D12	72	V_{CC}	121	GND	170	A16
24	D13	73	GND	122	GND	171	A17
25	V_{CC}	74	TM2	123	PCLK	172	GND
26	D14	75	TM1	124	GND	173	V_{CC}
27	D15	76	GND	125	GND	174	A18
28	GND	77	GND	126	V_{CC}	175	A19
29	D16	78	TM0	127	V_{CC}	176	GND
30	D17	79	TLN1	128	BCLK	177	A20
31	V_{CC}	80	V_{CC}	129	GND	178	A21
32	GND	81	TLN0	130	GND	179	V_{CC}
33	D18	82	SIZ0	131	IPL0	180	A22
34	D19	83	GND	132	IPL1	181	A23
35	GND	84	GND	133	IPL2	182	GND
36	D20	85	R/W	134	RSTI	183	GND
37	D21	86	LOCKE	135	CDIS	184	A24
38	V_{CC}	87	V_{CC}	136	MDIS	185	A25
39	D22	88	GND	137	V_{CC}	186	V_{CC}
40	V_{CC}	89	SIZ1	138	GND	187	A26
41	D23	90	LOCK	139	TMS	188	A27
42	GND	91	GND	140	TRST	189	GND
43	D24	92	MI	141	GND	190	A28
44	D25	93	BR	142	TCK	191	A29
45	GND	94	V_{CC}	143	TD1	192	V_{CC}
46	V_{CC}	95	TS	144	TD0	193	A30
47	D26	96	BB	145	RSTO	194	A31
48	D27	97	GND	146	GND	195	GND
49	GND	98	GND	147	GND	196	GND

FIGURE 2. Terminal connections.

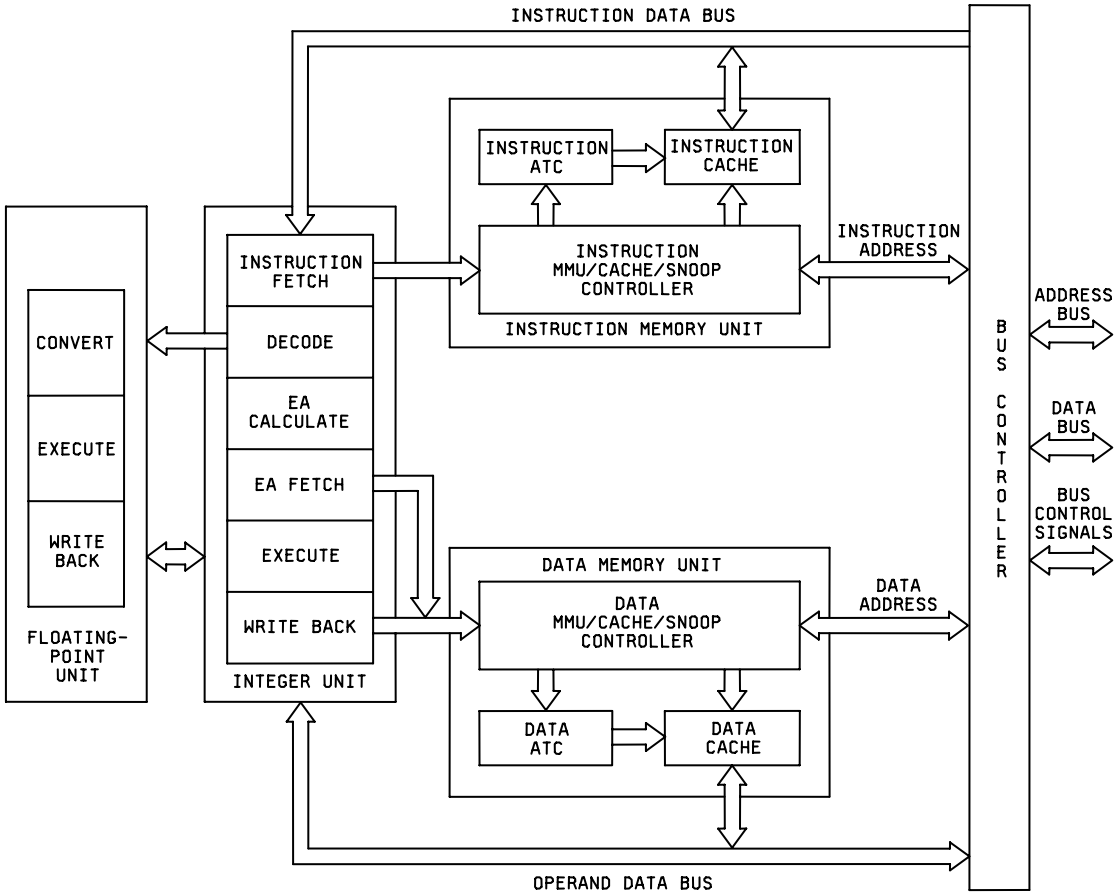


FIGURE 3. Block diagram.

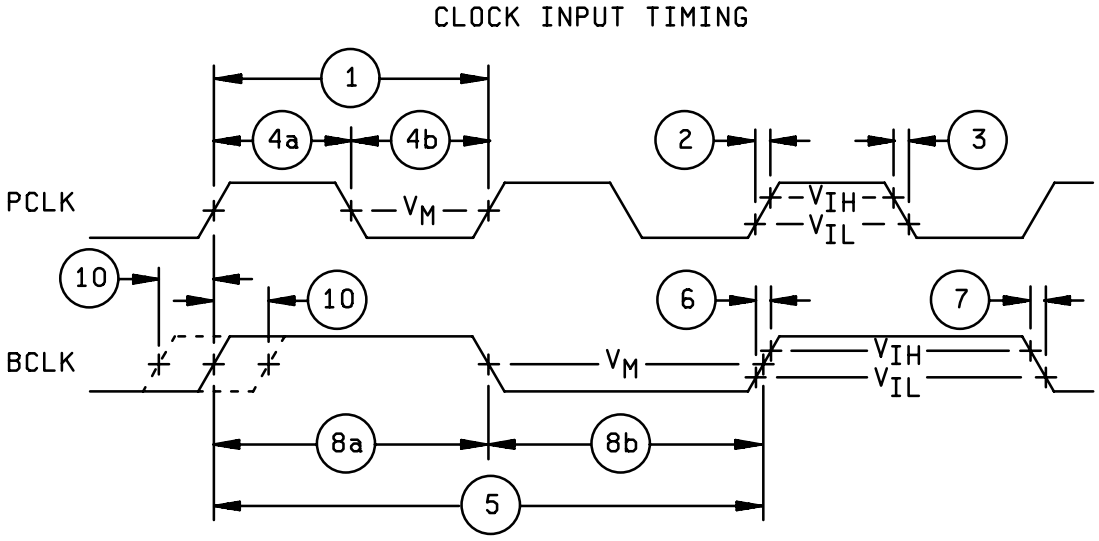
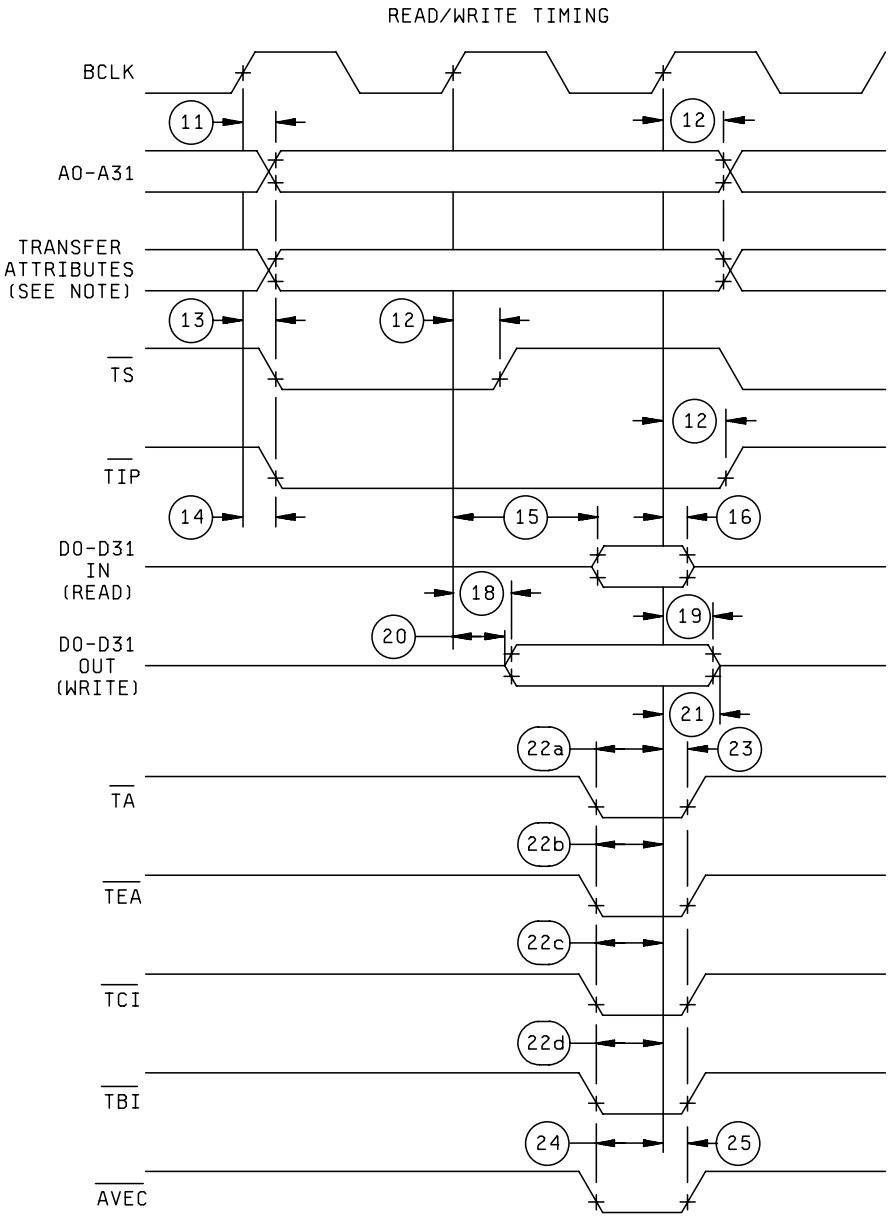


FIGURE 4. Switching test circuit and waveforms.



Note: Transfer attribute signals = UPAn, SIZn, TTN, TMn, TLNn, R/$\overline{W}$, $\overline{LOCK}$, $\overline{LOCKE}$, and $\overline{CIOUT}$.

FIGURE 4. Switching test circuit and waveforms - Continued.

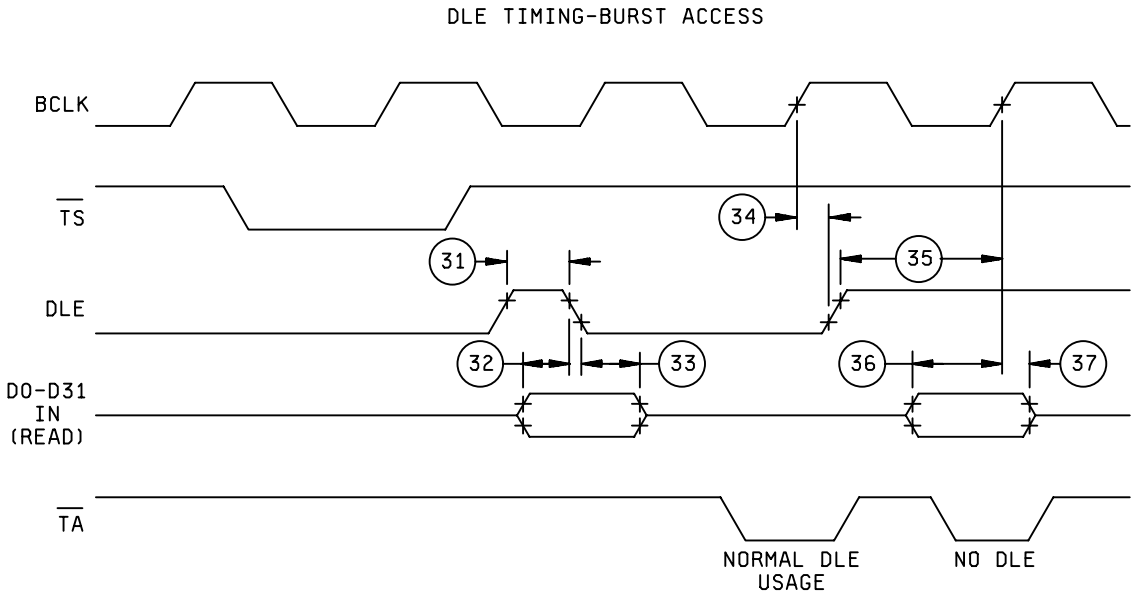


FIGURE 4. Switching test circuit and waveforms - Continued.

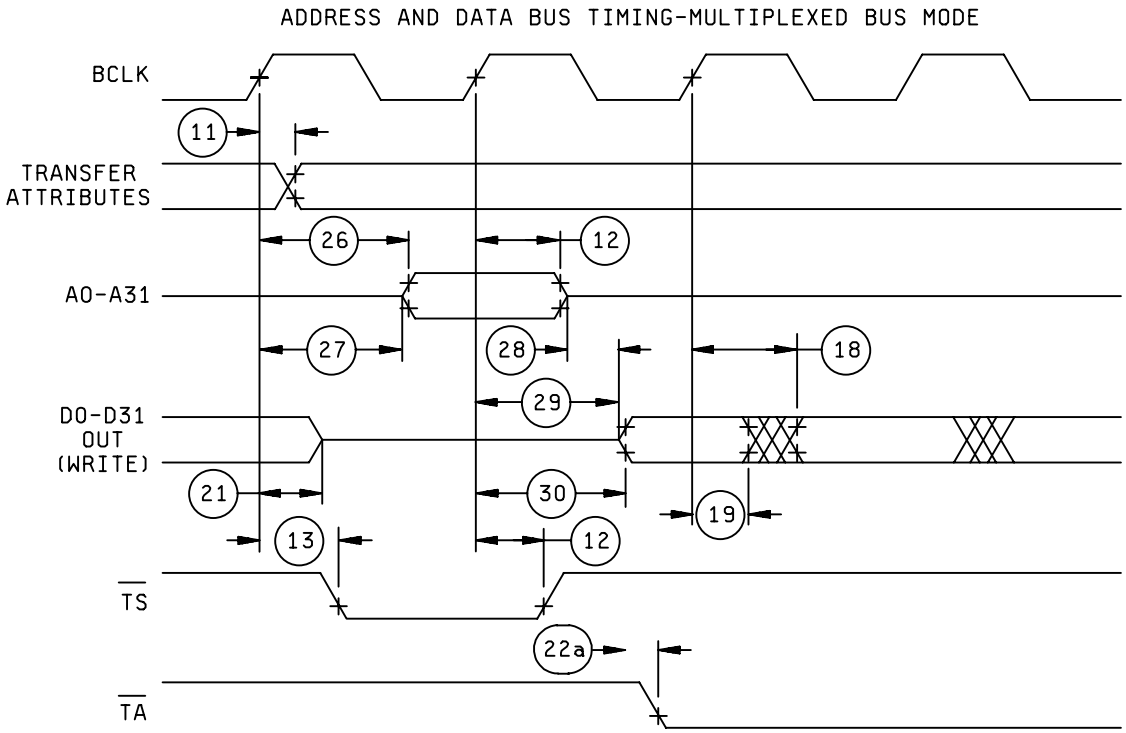


FIGURE 4. Switching test circuit and waveforms - Continued.

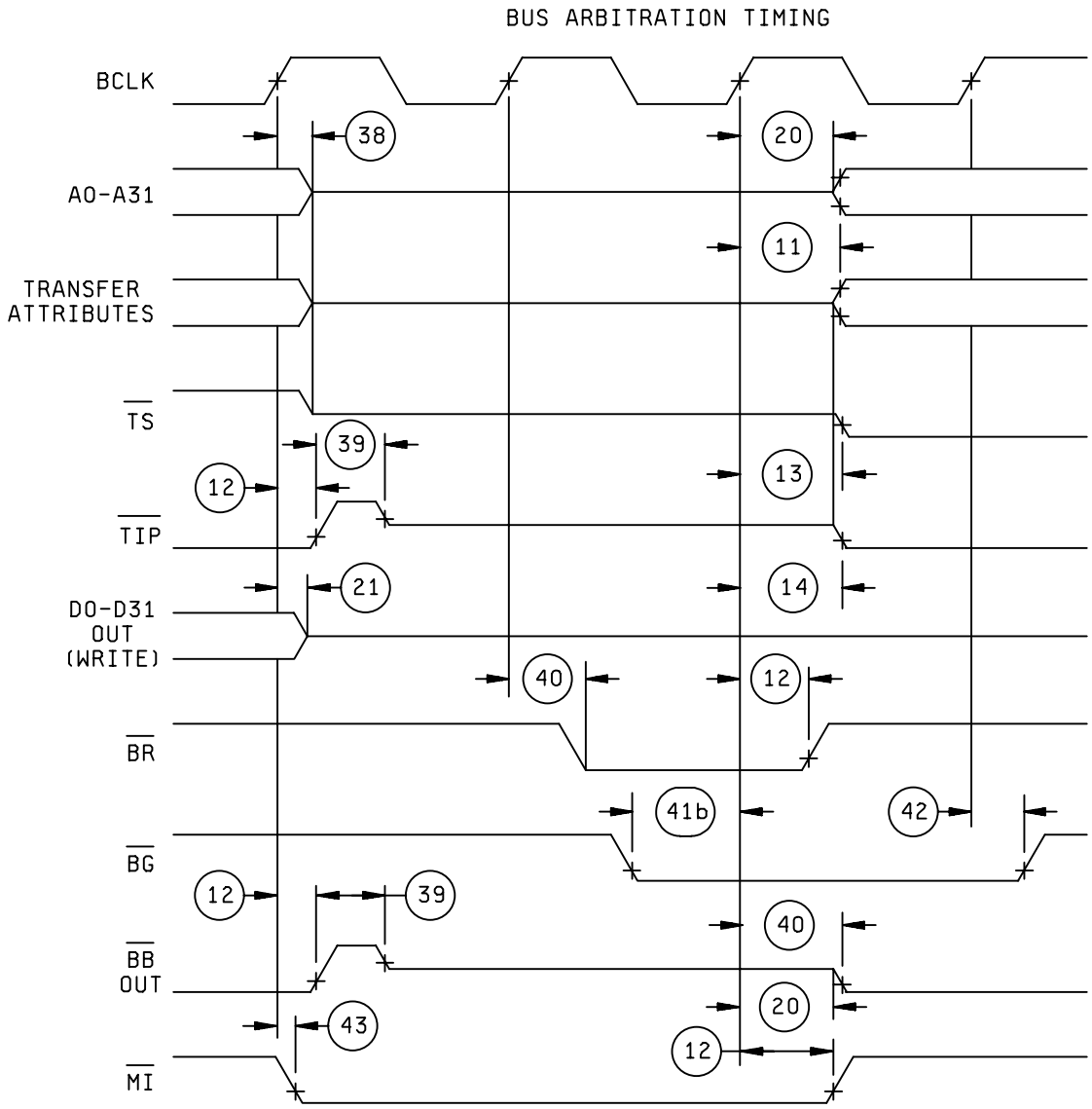


FIGURE 4. Switching test circuit and waveforms - Continued.

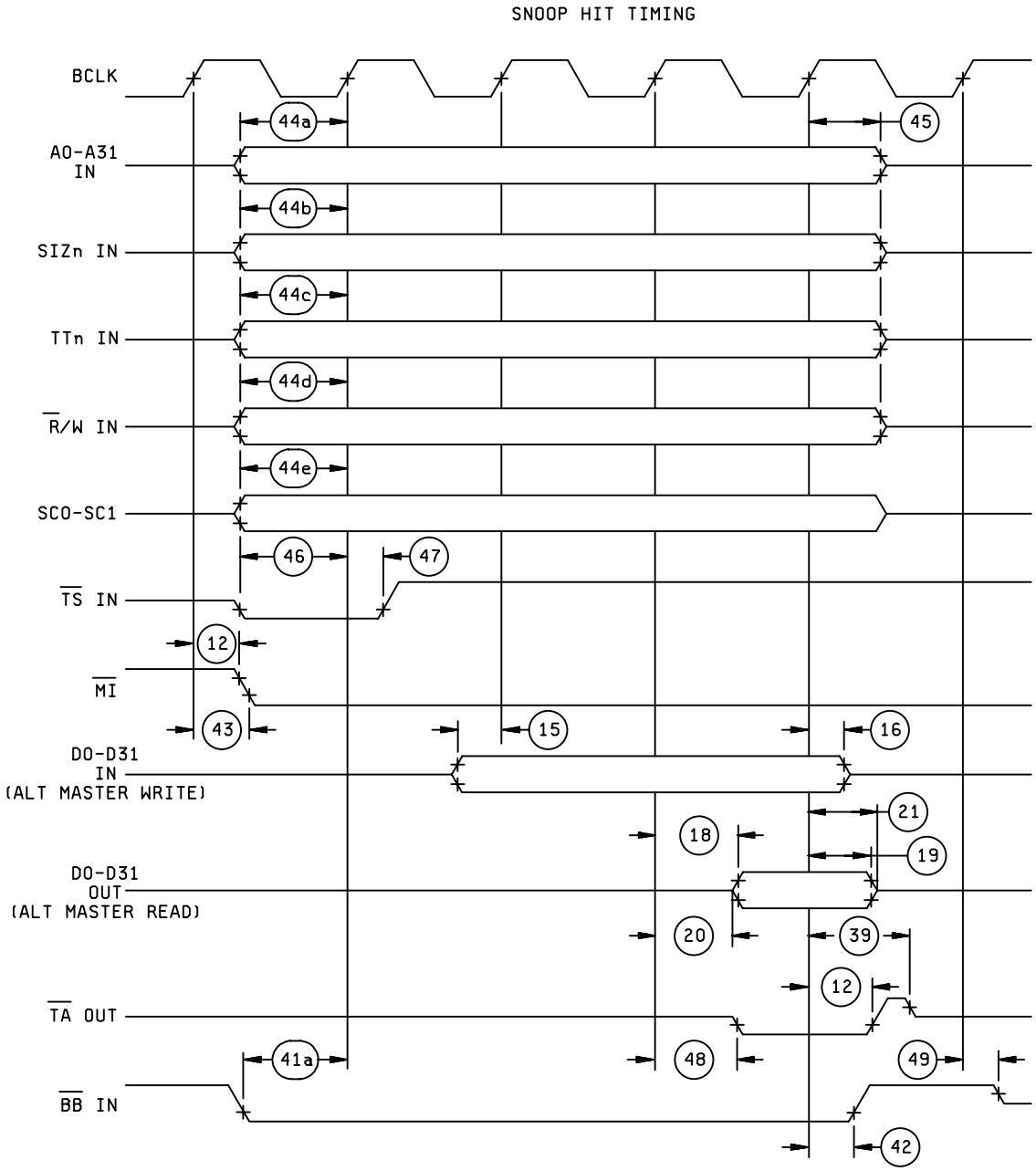


FIGURE 4. Switching test circuit and waveforms – Continued.

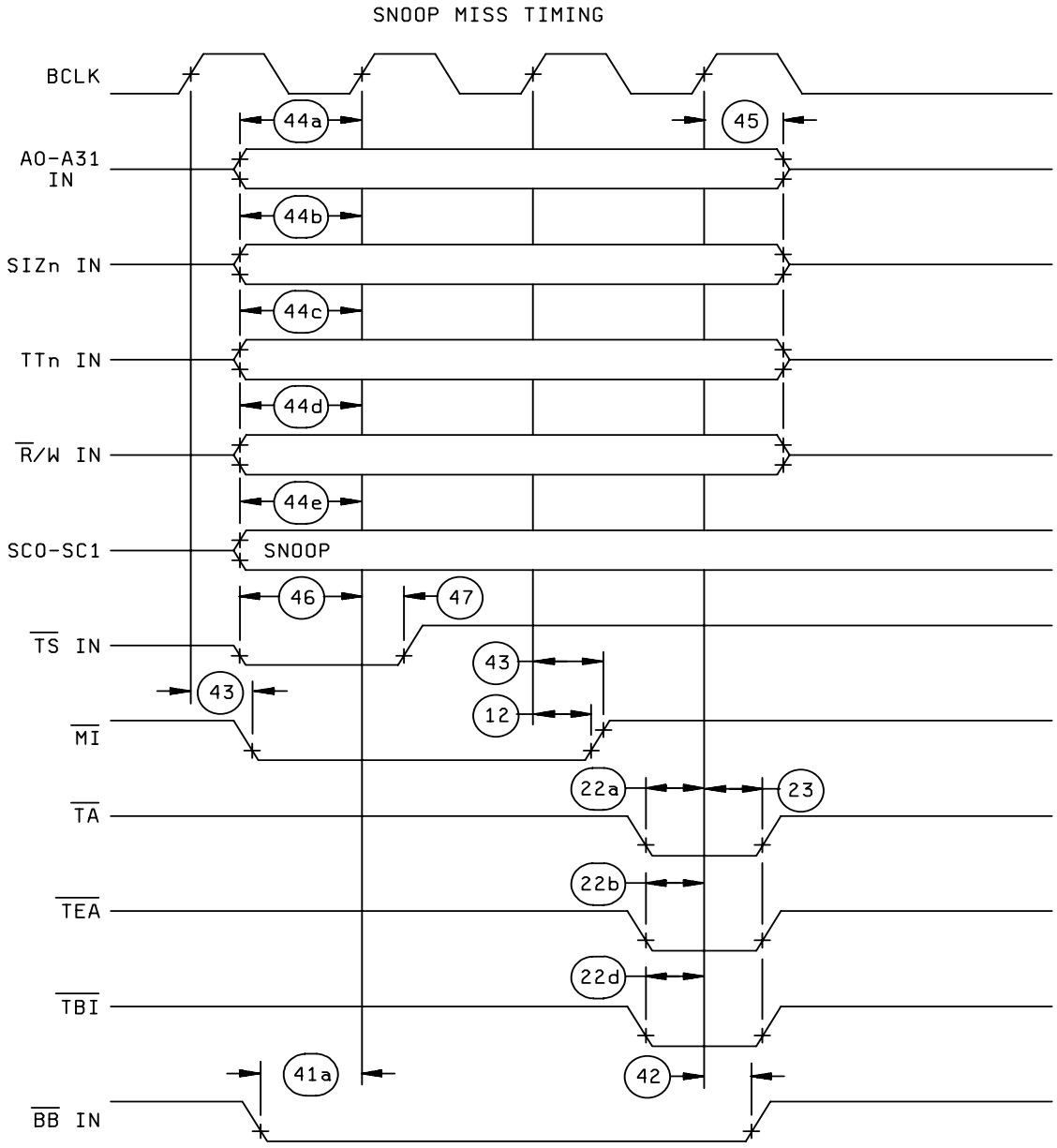


FIGURE 4. Switching test circuit and waveforms - Continued.

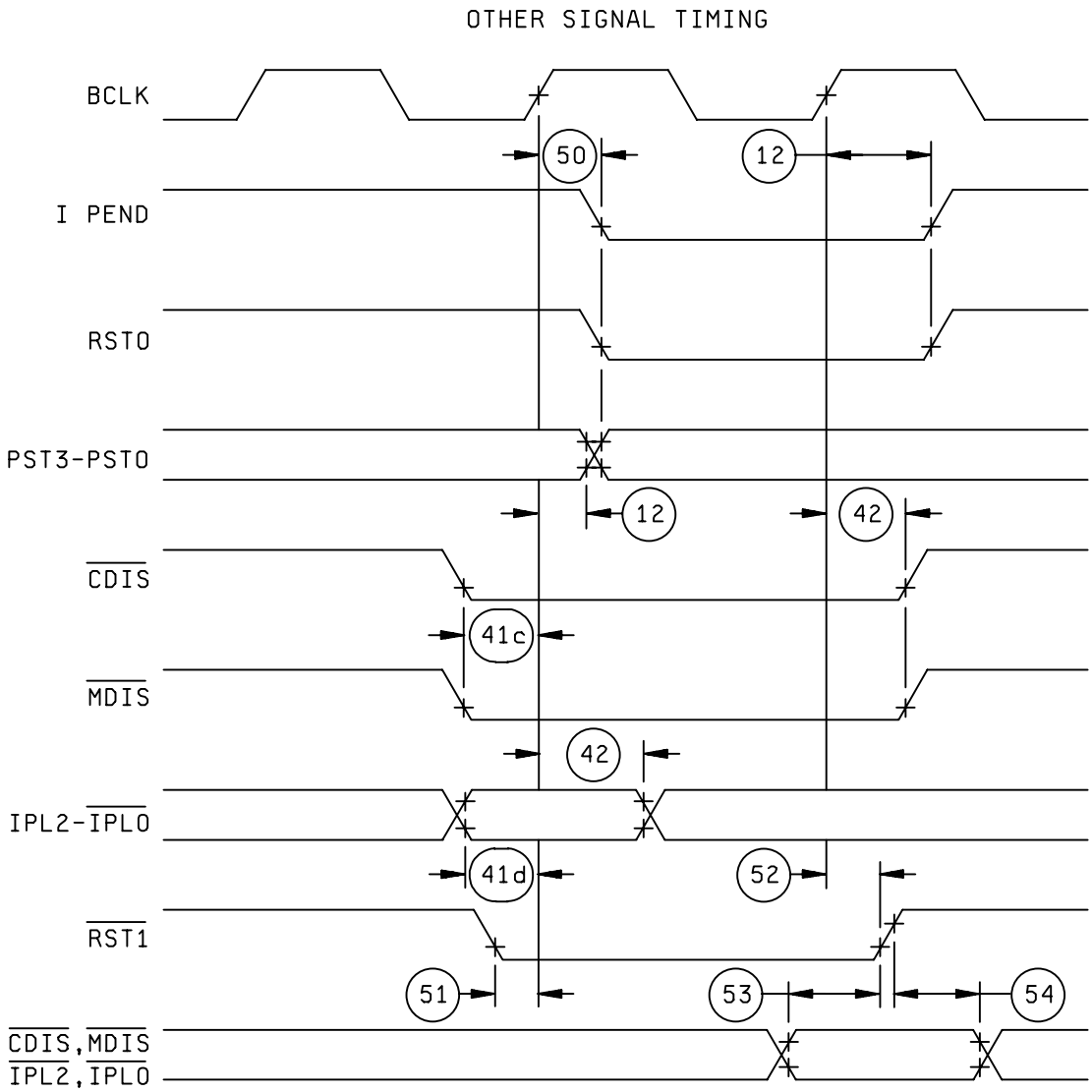


FIGURE 4. Switching test circuit and waveforms - Continued.

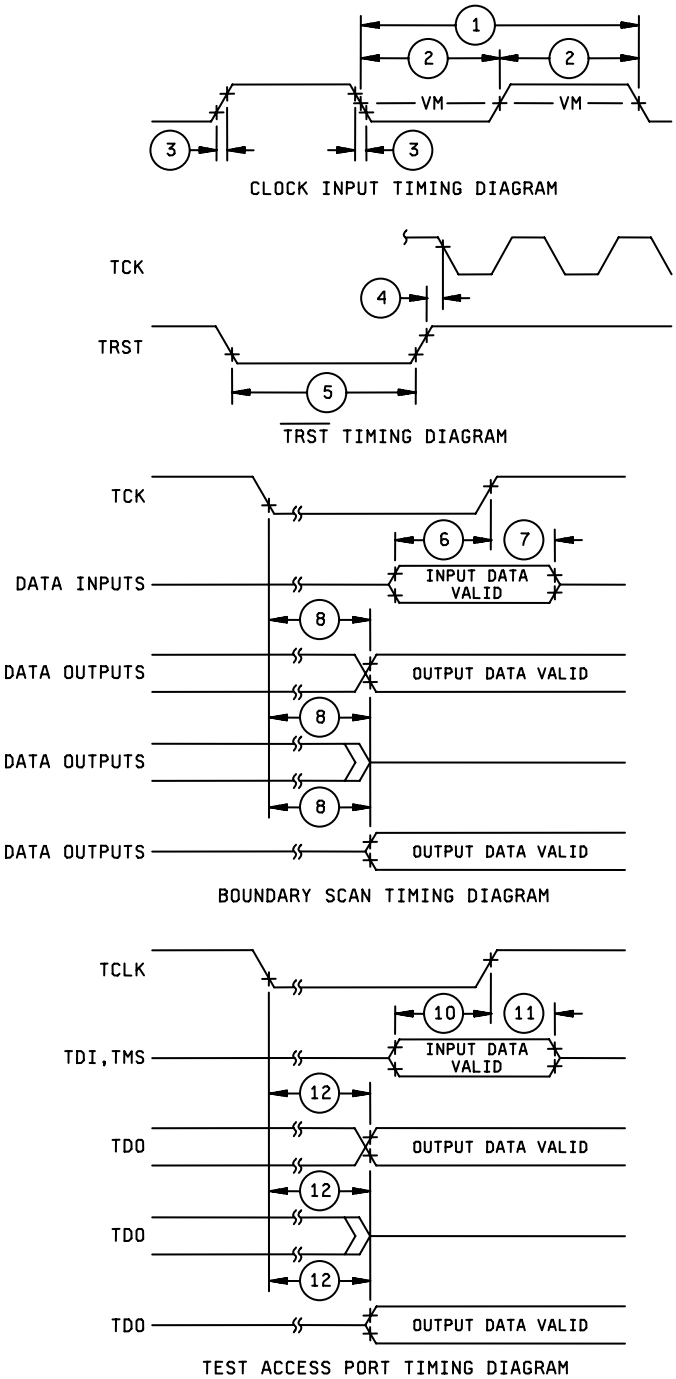


FIGURE 4. Switching test circuit and waveforms - Continued.

Bit 2	Bit 1	Bit 0	Instruction selected	Test data register accessed
0	0	0	EXTEST	BOUNDARY SCAN
0	0	1	HIGHZ	BYPASS
0	1	0	SAMPLE/PRELOAD	BOUNDARY SCAN
0	1	1	DRVCTLT	BOUNDARY SCAN
1	0	0	SHUTDOWN	BYPASS
1	0	1	PRIVATE	BYPASS
1	1	0	DRVCTLS	BOUNDARY SCAN
1	1	1	BYPASS	BYPASS

FIGURE 5. Boundary scan instruction codes.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	---	---	----

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331, and as follows:

A31-A0 (Address bus) 32-bit address bus used to address any of the 4-Gbytes.

D31-D0 (Data bus) 32-bit data bus used to transfer up to 32 bits of data per bus transfer.

TT1,TT0 (Transfer type) Indicates the general transfer type: normal, MOVE16, alternate logical function code, and acknowledge.

TM2, TM0 (Transfer modifier) Indicates supplemental information about the access.

TLN1, TLN0 (Transfer line number) Indicates which cache line in a set is being pushed or loaded by current line transfer.

UPA1, UPA0 (User programmable attributes) User-defined signals, controlled by the corresponding user attribute bits from address translation entry.

$\overline{R/W}$ (Read/write) Identifies a transfer as a read or a write.

SIZ1, SIZ0 (Transfer size) Indicates the data transfer size. These signals, together with A0 and A1, define the active sections of the data bus.

$\overline{LOCK}$ (Bus lock) Indicates a bus transfer is part of a read-modify-write operation, and that the sequence of transfers should not be interrupted.

$\overline{LOCKE}$ (Bus lock end) Indicates the current transfer is the last in a locked sequence transfer.

$\overline{CIOUT}$ (Cache inhibit out) Indicates the processor will not cache the current bus transfer.

$\overline{TS}$ (Transfer start) Indicates the beginning of a bus transfer.

$\overline{TIP}$ (Transfer in progress) Asserted for the duration of a bus transfer.

$\overline{TA}$ (Transfer acknowledge) Asserted to acknowledge a bus transfer.

$\overline{TEA}$ (Transfer error acknowledge) Indicates an error condition exists for a bus transfer.

$\overline{TCI}$ (Transfer cache inhibit) Indicates the current bus transfer should not be cached.

$\overline{TBI}$ (Transfer burst inhibit) Indicates the slave cannot handle a line burst access.

DLE (Data latch enable) Alternate clock input used to latch input data when the processor is operating in DLE mode.

SC1, SC0 (Snoop control) Indicates the snooping operation required during an alternate master access.

$\overline{MI}$ (Memory inhibit) Inhibits memory devices from responding to an alternate master access during snooping operations.

$\overline{BR}$ (Bus request) Asserted by the processor to request bus mastership.

$\overline{BG}$ (Bus grant) Asserted by an arbiter to grant bus mastership to the processor.

$\overline{BB}$ (Bus busy) Asserted by the current bus master to indicate that it has assumed ownership of the bus.

$\overline{CDIS}$ (Cache disable) Dynamically disables the internal caches to assist emulator support.

$\overline{MDIS}$ (MMU disable) Disables the translation mechanism of MMU's.

$\overline{RSTI}$ (Reset in) Processor reset.

$\overline{RSTO}$ (Reset out) Asserted during execution of a RESET instruction to reset external devices.

$\overline{IPL2}$-$\overline{IPL0}$ (Interrupt priority level) Provides an encoded interrupt level to the processor.

$\overline{IPEND}$ (Interrupt pending) Indicates an interrupt is pending.

$\overline{AVEC}$ (Autovector) Used during an interrupt acknowledge transfer to request internal generation of the vector number.

PST3-PST0 (Processor status) Indicates internal processor status.

BCLK (Bus clock) Clock input used to derive all bus signal timing.

PCLK (Processor clock) Clock input used for internal logic timing. The PCLK frequency is exactly 2x the BCLK frequency.

TCK (Test clock) Clock signal for the IEEE P1149.1 test access port (TAP).

TMS (Test mode select) Selects the principle operations of the test-support circuitry.

TDI (Test data input) Serial data input for the TAP.

TDO (Test data output) Serial data output for the TAP.

$\overline{TRST}$ (Test reset) Provides an asynchronous reset of the TAP controller.

V_{CC} (Power supply) Power supply.

GND (Ground) Ground connection.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 05-10-17

Approved sources of supply for SMD 5962-93143 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9314301MXA	F8385	TS68040MR1B/C25A
5962-9314301MXC	F8385	TS68040MRB/C25A
5962-9314301MYC	F8385	TS68040MFTBC25A
5962-9314301MZA	F8385	TS68040MF1B/C25A
5962-9314301MZC	F8385	TS68040MFB/C25A
5962-9314302MXA	F8385	TS68040MR1B/C33A
5962-9314302MXC	F8385	TS68040MRB/C33A
5962-9314302MYC	F8385	TS68040MFTBC33A
5962-9314302MZA	F8385	TS68040MF1B/C33A
5962-9314302MZC	F8385	TS68040MFB/C33A

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
F8385	Atmel Grenoble Avenue De Rochepleine BP123 Saint Egreve CEDEX 38521, France