REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26							

REV STATUS OF SHEETS	REV															
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
95-11-22

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, 32-BIT RISC MICROPROCESSOR, 3.3 V, JTAG, MONOLITHIC SILICON

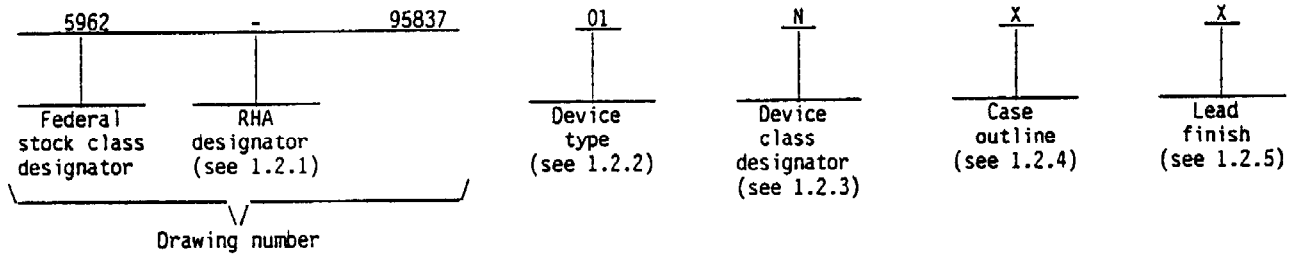
SIZE	CAGE CODE	
A	67268	5962-95837

SHEET 1 OF 26

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Three product assurance classes consisting of space application (device class V), military high reliability (device classes M and Q), and non-traditional military (device class N) with a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". For device class N, the user is cautioned to assure that the device is appropriate for the application environment. When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes N, Q, and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Temperature range	Speed
01	80486DX4	32-bit microprocessor	-55°C to 125°C	75 MHz
02	80486DX4	32-bit microprocessor	-55°C to 125°C	100 MHz
03	80486DX4	32-bit microprocessor	-40°C to 125°C	75 MHz
04	80486DX4	32-bit microprocessor	-40°C to 125°C	100 MHz
05	80486DX4	32-bit microprocessor	-40°C to 110°C	75 MHz
06	80486DX4	32-bit microprocessor	-40°C to 110°C	100 MHz

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883 1/
N	Certification and qualification to MIL-I-38535 with a non-traditional performance environment 2/
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA9-P168	168	Ceramic, pin grid array
Y	See Figure 1	196	Leaded chip carrier with unformed leads

1.2.5 Lead finish. The lead finish shall be as specified in MIL-I-38535 for device classes N, Q, and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1/ For this drawing device class M shall not apply.
2/ Any device outside the traditional performance environment (i.e., an operating temperature range of -55°C to +125°C and which requires hermetic packaging).

1.3 Absolute maximum ratings. 1/

Storage temperature range	-65°C to +150°C
Supply voltage with respect to ground range	V_{CC} - 0.5 V to +4.6 V
Voltage on any pin with respect to ground range	-0.5 V to V_{CC} + 0.5 V
Maximum power dissipation (P_D)	5 W
Lead temperature (soldering, 10 seconds)	300°C
Thermal resistance, junction-to-case (θJ_C):	
Case X	See MIL-STD-1835
Case Y	2.5°C/W
Maximum junction temperature (T_J)	150°C

1.4 Recommended operating conditions.

Case operating temperature range	See 1.2.2
Supply voltage, (V_{CC})	3.3 V ±5%

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	98.5 percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes N, Q, and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions for device classes N, Q, and V shall be as specified in MIL-I-38535 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Switching waveforms The switching waveforms shall be as specified in figure 4

3.3.5 Boundry scan instruction codes The boundry scan instruction codes shall be as specified in figure 5.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device classes N, Q, and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes N, Q, and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. A certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes N, Q, and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device classes N, Q, and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection. Qualification inspection for device classes N, Q, and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input low voltage	V_{IL}	Frequency = 8 MHz	1,2,3	All	-0.3	0.8	V
Input high voltage	V_{IH}	Frequency = 8 MHz	1,2,3	All	2.0	V_{CC5} +0.3	V
Output low voltage	V_{OL}	I_{OL} = 2.0 mA 2/ I_{OL} = 100 µA 2/	1,2,3	All		0.45	V
Output high voltage	V_{OH}	I_{OH} = -2.0 mA 2/	1,2,3	All	2.4		V
Input leakage current	I_{LI}	$0 \le V_{IN} \le V_{CC}$	1,2,3	All	-15	+15	µA
Input leakage current	I_{IH}	VIN = 2.4 V 3/	1,2,3	All		200	µA
Input leakage current	I_{IL}	VIN = 0.45 V 4/	1,2,3	All		-400	µA
Output leakage current	I_{LO}	VIN = GND and V_{CC}	1,2,3	All	-15	+15	µA
Supply current active power supply	I_{CC}	V_{CC} = V_{CC} MAX 5/	1,2,3	01,03,05 02,04,06		1100 1450	mA
Supply current active leakage current	I_{CC5}	V_{CC} = V_{CC} MAX	1,2,3	All		300	µA
Supply current stop grant	I_{CCSG}	V_{CC} = V_{CC} MAX 6/	1,2,3	01,03,05 02,04,06		75 100	mA
Supply current stop clock	I_{CCSC}	V_{CC} = V_{CC} MAX 7/ Frequency = 0 MHz	1,2,3	All		1.0	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
CLK input capacitance	C_{CLK}	Frequency = 1 MHz See 4.4.1.c	4	All		12	pF
Input capacitance	C_{IN}	Frequency = 1 MHz See 4.4.1.c	4	All		10	pF
Input/output capacitance	$C_{I/O}$	Frequency = 1 MHz See 4.4.1.c	4	All		14	pF
Output capacitance	C_O	Frequency = 1 MHz See 4.4.1.c	4	All		14	pF
Functional test		See 4.4.1.b	7,8	All			
System clock frequency	f	1X clock driven to Clk input	9,10,11	01,03,05 02,04,06	8 8	25 33	MHz
System clock period	t_1	See figure 4	9,10,11	01,03,05 02,04,06	40 30	125 125	ns
System clock high time	t_2	at 2.0 V See figure 4	9,10,11	01,03,05 02,04,06	14 11		ns
System clock low time	t_3	at 0.8 V See figure 4	9,10,11	01,03,05 02,04,06	14 11		ns
System clock fall time 8/	t_4	2.0 V to 0.8 V See figure 4	9,10,11	01,03,05 02,04,06		4 3	ns
System clock rise time 8/	t_5	0.8 V to 2.0 V See figure 4	9,10,11	01,03,05 02,04,06		4 3	ns
A2-A31,PWT,PCD,BE0-3#,M/IO#, D/C#,W/R#,ADS#,LOCK#, FERR#,BREQ,HLDA VALID DELAY, CACHE#, HITM#	t_6	See figure 4	9,10,11	01,03,05 02,04,06	2 2	19 14	ns
A2-A31,PWT,PCD,BE0-3#,M/IO#, D/C#,W/R#,ADS#,LOCK# FLOAT DELAY,CACHE#	t_7	See figure 4 8/	9,10,11	01,03,05 02,04,06		28 20	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
PCHK# VALID DELAY	t_8	See figure 4	9,10,11	01,03,05 02,04,06	2 2	24 14	ns
BLAST#, PLOCK#, SMIACT# Valid delay	t_{8a}	See figure 4	9,10,11	01,03,05 02,04,06	2 2	24 14	ns
BLAST#, PLOCK# FLOAT DELAY	t_9	See figure 4 8/	9,10,11	01,03,05 02,04,06		28 20	ns
D0-D31,DP0-3 WRITE DATA VALID DELAY	t_{10}	See figure 4	9,10,11	01,03,05 02,04,06	2 2	20 14	ns
D0-D31,DP0-3 WRITE DATA FLOAT DELAY 8/	t_{11}	See figure 4	9,10,11	01,03,05 02,04,06		28 20	ns
EADS#, INV SETUP TIME	t_{12}	See figure 4	9,10,11	01,03,05 02,04,06	8 5		ns
EADS#, INV HOLD TIME	t_{13}	See figure 4	9,10,11	01,03,05 02,04,06	3 3		ns
KEN#,BS16#,BS8#, WB/WT# setup time	t_{14}	See figure 4	9,10,11	01,03,05 02,04,06	8 5		ns
KEN#,BS16#,BS8#, WB/WT# setup time	t_{15}	See figure 4	9,10,11	01,03,05 02,04,06	3 3		ns
RDY#,BRDY# SETUP TIME	t_{16}	See figure 4	9,10,11	01,03,05 02,04,06	8 5		ns
RDY#,BRDY# HOLD TIME	t_{17}	See figure 4	9,10,11	01,03,05 02,04,06	3 3		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
HOLD,AHOLD SETUP TIME	t_{18}	See figure 4	9,10,11	01,03,05 02,04,06	8 6		ns
BOFF# SETUP TIME	t_{18a}	See figure 4	9,10,11	01,03,05 02,04,06	8 7		ns
HOLD,AHOLD,BOFF# HOLD TIME	t_{19}	See figure 4	9,10,11	01,03,05 02,04,06	3 3		ns
RESET, FLUSH#, A20M#,NMI, INTR,IGNNE#, SRESET, STPCLK#, SMI# setup time	t_{20}	See figure 4 9/	9,10,11	01,03,05 02,04,06	8 5		ns
RESET, FLUSH#, A20M#,NMI, INTR,IGNNE#, SRESET, STPCLK#,SMI# HOLD TIME	t_{21}	9/ See figure 4	9,10,11	01,03,05 02,04,06	3 3		ns
D0-D31,DP0-3,A4-A31 READ SETUP TIME	t_{22}	See figure 4	9,10,11	01,03,05 02,04,06	5 5		ns
D0-D31,DP0-3,A4-A31 READ HOLD TIME	t_{23}	See figure 4	9,10,11	01,03,05 02,04,06	3 3		ns
JTAG 10/							
TCK frequency	t24	1X clock See figure 5	9,10,11	All		25	MHz
TCK period	t_{25}	See figure 5	9,10,11	All	40		ns
TCK high time	t_{26}	VIN = 2.0 V See figure 5	9,10,11	All	10		ns
TCK low time	t_{27}	V_{IN} = 0.8 V See figure 5	9,10,11	All	10		ns
TCK rise time	t_{28}	$0.8V \le V_{IN} \le 2.0V$ See figure 5	9,10,11	All		4	ns
TCK fall time	t_{29}	$2.0V \le V_{IN} \le 0.8V$ See figure 5	9,10,11	All		4	ns

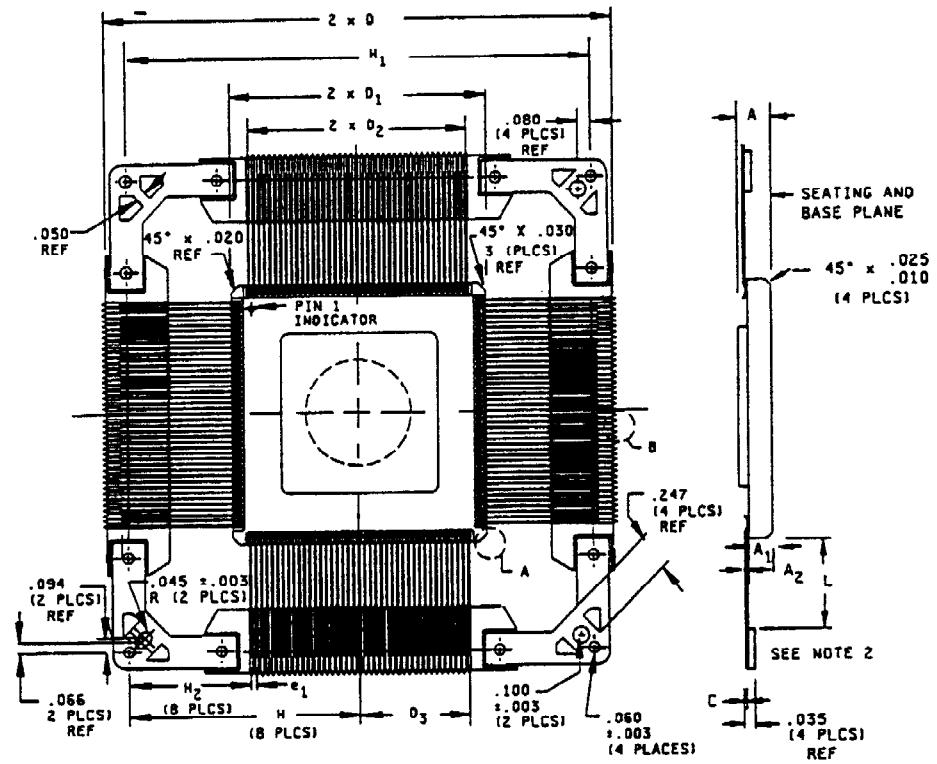
See footnotes at end of table.

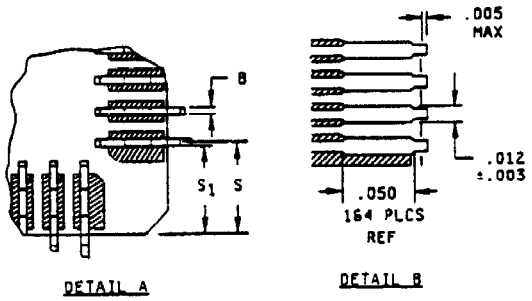
TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
TDI, TMS Setup time	t_{30}	See figure 5	9,10,11	All	8		ns
TDI, TMS hold time	t_{31}	See figure 5	9,10,11	All	7		ns
TDO valid delay	t_{32}	See figure 5	9,10,11	All	3	25	ns
TDO float delay	t_{33}	See figure 5	9,10,11	All		30	ns
All outputs (non-test) valid delay	t_{34}	See figure 5	9,10,11	All	3	25	ns
All outputs (non-test) float delay	t_{35}	See figure 5	9,10,11	All		36	ns
All inputs (non-test) setup time	t_{36}	See figure 5	9,10,11	All	8		ns
All inputs (non-test) hold time	t_{37}	See figure 5	9,10,11	All	7		ns

1/ All testing to be performed using worst-case test conditions unless otherwise specified. All timing specifications assume C_L = 50 pF.
2/ Actual value tested may vary due to test hardware limitations, however, specified value is guaranteed.
3/ Parameter is for input pins with internal pulldown resistors.
4/ Parameter is for input pins with internal pullup resistors.
5/ This parameter is for proper power supply selection. It is measured using the worst-case instruction mix at V_{CC} = 3.465 V.
6/ The I_{CC} stop grant specification refers to the I_{CC} value once the device enters the stop grant or halt auto powerdown state.
7/ The I_{CC} stop clock specification refers to the I_{CC} value once the device enters the stop clock state. V_{IH} and V_{IL} must be equal to V_{CC} and 0V, respectively, in order to meet the I_{CC} stop clock specifications.
8/ Guaranteed by design characterization but not tested.
9/ A reset pulse width of 15 CLK cycles is required for warm resets (RESET or SRESET). Power-up resets (cold restes) require RESET to be asserted for at least 1ms after V_{CC} and CLK are stable.
10/ Test pins (TCK, TDI, TDO, TMS) are exceptions. These pins are tested and guaranteed to the following limits:
V_{IL} = 0 V
V_{IH} = 3 V
$V_{OL} = V_{OH}$ = 1.5 V
$I_{OL} = I_{OH}$ = 0 mA

Case Y





Inches	mm
.003	0.08
.005	0.13
.010	0.25
.012	0.30
.020	0.51
.025	0.64
.030	0.76
.035	0.89
.045	1.14
.050	1.27
.060	1.52
.066	1.68
.060	2.03
.094	2.39
.247	6.27

FIGURE 1. Case outline.

Case Y

Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	2.23	2.92	Solid lid	0.088	0.115	Solid lid
A_1	1.96	2.39		0.077	0.094	
B	0.20	0.25		0.008	0.010	
C	0.10	0.20		0.004	0.008	
D	63.50	64.01		2.500	2.520	
D_1	33.65	34.16		1.325	1.345	
D_2	30.48 Basic			1.200 Basic		
e_1	0.58	0.69		0.023	0.027	
H	29.21 Basic			1.150 Basic		
H_1	58.42 Basic			2.30 Basic		
H_2	19.05 Basic			0.750 Basic		
L	9.27	10.03		0.365	0.395	
N	196			196		
S	1.270	2.03	Reference	0.050	0.080	Reference
S_1	1.14	1.93	Reference	0.045	0.076	Reference
Issue	IWS 7/90					

FIGURE 1. Case outline - Continued.

Case X

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
	A27	A26	A23	VOLDET	A14	V_{SS}	A12	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	A10	V_{SS}	A6	A4	ADS#	
S	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	S
	A28	A25	V_{CC}	V_{SS}	A18	V_{CC}	A15	V_{CC}	V_{CC}	V_{CC}	V_{CC}	A11	A8	V_{CC}	A3	BLAST#	CLKMUL	
R	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	R
	A31	V_{SS}	A17	A19	A21	A24	A22	A20	A16	A13	A9	A5	A7	A2	BRED	PLOCK#	PCHK#	
Q	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	Q
	D0	A29	A30												HLDA	V_{CC}	V_{SS}	
P	O	O	O												O	O	O	P
	D2	D1	DP0												LOCK#	M/IO#	W/R#	
N	O	O	O												O	O	O	N
	V_{SS}	V_{CC}	D4												D/C#	V_{CC}	V_{SS}	
H	O	O	O												O	O	O	H
	V_{SS}	D6	D7												PWT	V_{CC}	V_{SS}	
L	O	O	O												O	O	O	L
	V_{SS}	V_{CC}	D14												BED#	V_{CC}	V_{SS}	
K	O	O	O												O	O	O	K
	V_{CC5}	D5	D16												BE2#	BE1#	PCD	
J	O	O	O												O	O	O	J
	V_{SS}	D3	DP2												BRDY#	V_{CC}	V_{SS}	
H	O	O	O												O	O	O	H
	V_{SS}	V_{CC}	D12												STPCLK#	V_{CC}	V_{SS}	
G	O	O	O												O	O	O	G
	DP1	D8	D15												KEN#	RDY#	BE3#	
F	O	O	O												O	O	O	F
	V_{SS}	V_{CC}	D10												HOLD	V_{CC}	V_{SS}	
E	O	O	O												O	O	O	E
	D9	D13	D17												A20M#	BS8#	BOFF#	
D	O	O	O												O	O	O	D
	D11	D18	CLK	V_{CC}	V_{CC}	D27	D26	D28	D30	SRESET	V_{CC}	SMIACT#	NC	FERR#	FLUSH#	RESET	BS16#	
C	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	C
	D19	D21	V_{SS}	V_{SS}	V_{SS}	D25	V_{CC}	D31	V_{CC}	SMI#	V_{CC}	CACHE#	WB/WT#	TMS	NMI	TDO	EADS#	
B	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	B
	D20	D22	TCK	D23	DP3	D24	V_{SS}	D29	V_{SS}	INV	V_{SS}	HITM#	INC	TDI	IGNNE#	INTR	AHOLD	
A	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	A
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

Note:
The 5 Volt reference voltage input pin (V_{CC5}) is the reference voltage for the 5v-tolerant I/O buffers. This signal should be connected to the +5 V ±5% for use with 5 V system logic, If all inputs to the device are from 3 V system logic this pin should be connected to 3.3 V ±5%. # indicates active low signal.

FIGURE 2. Terminal connections.

Case outlines	Y										
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	D21	34	SMIACT#	67	W/R#	100	BLAST#	133	V_{SS}	166	V_{SS}
2	D22	35	V_{SS}	68	V_{SS}	101	ADS#	134	TDI	167	D5
3	D23	36	SRESET	69	HLDA	102	A2	135	V_{CC}	168	V_{CC}
4	DP3	37	V_{CC}	70	V_{CC}	103	A3	136	TMS	169	D6
5	D24	38	WB/WT#	71	CLK	104	A4	137	V_{SS}	170	V_{SS}
6	D25	39	V_{SS}	72	V_{SS}	105	V_{SS}	138	A18	171	D7
7	V_{SS}	40	HITM#	73	V_{SS}	106	A5	139	V_{CC}	172	V_{CC}
8	D26	41	V_{CC}	74	V_{CC}	107	V_{CC}	140	A19	173	DP1
9	V_{CC}	42	N/C	75	V_{CC}	108	N/C	141	V_{SS}	174	V_{SS}
10	D27	43	V_{SS}	76	V_{SS}	109	V_{SS}	142	A20	175	D8
11	V_{SS}	44	N/C	77	N/C	110	A6	143	A21	176	V_{CC}
12	D28	45	N/C	78	V_{CC}	111	V_{CC}	144	A22	177	D9
13	V_{CC}	46	NMI	79	TCK	112	A7	145	A23	178	V_{SS}
14	D29	47	INTR	80	V_{SS}	113	V_{SS}	146	A24	179	D10
15	V_{SS}	48	FLUSH#	81	AHOLD	114	A8	147	A25	180	V_{CC}
16	D30	49	RESET	82	V_{CC}	115	V_{CC}	148	A26	181	D11
17	V_{CC}	50	A20M#	83	HOLD	116	A9	149	A27	182	V_{SS}
18	D31	51	EADS#	84	V_{SS}	117	V_{SS}	150	A28	183	D12
19	V_{SS}	52	PCD	85	KEN#	118	A10	151	A29	184	V_{CC}
20	IGNNE#	53	PWT	86	V_{CC}	119	V_{CC}	152	A30	185	D13
21	V_{CC}	54	D/C#	87	RDY#	120	A11	153	A31	186	V_{SS}
22	STPCLK#	55	M/IO#	88	V_{SS}	121	V_{SS}	154	V_{SS}	187	D14
23	V_{SS}	56	V_{SS}	89	CLKMUL	122	A12	155	DP0	188	V_{CC}
24	TDO	57	BE3#	90	V_{CC}	123	V_{CC}	156	V_{CC}	189	D15
25	V_{CC}	58	V_{CC}	91	BS8#	124	A13	157	D0	190	V_{SS}
26	FERR#	59	BE2#	92	V_{SS}	125	V_{SS}	158	V_{SS}	191	DP2
27	V_{SS}	60	V_{SS}	93	BS16#	126	A14	159	D1	192	D16
28	INV	61	BE1#	94	BOFF#	127	V_{CC}	160	V_{CC}	193	D17
29	V_{CC}	62	V_{CC}	95	BRDY#	128	A15	161	D2	194	D18
30	SMI#	63	BE0	96	PCHK#	129	V_{SS}	162	V_{SS}	195	D19
31	V_{SS}	64	V_{SS}	97	V_{CC5}	130	A16	163	D3	196	D20
32	CACHE#	65	BREQ	98	LOCK#	131	V_{CC}	164	V_{CC}		
33	V_{CC}	66	V_{CC}	99	PLOCK#	132	A17	165	D4		

Note:
The 5 Volt reference voltage input pin (V_{CC5}) is the reference voltage for the 5v-tolerant I/O buffers. This signal should be connected to the +5 V ±5% for use with 5 V system logic, If all inputs to the device are from 3 V system logic this pin should be connected to 3.3 V ±5%. # indicates active low signal.

FIGURE 2. Terminal connections - Continued.

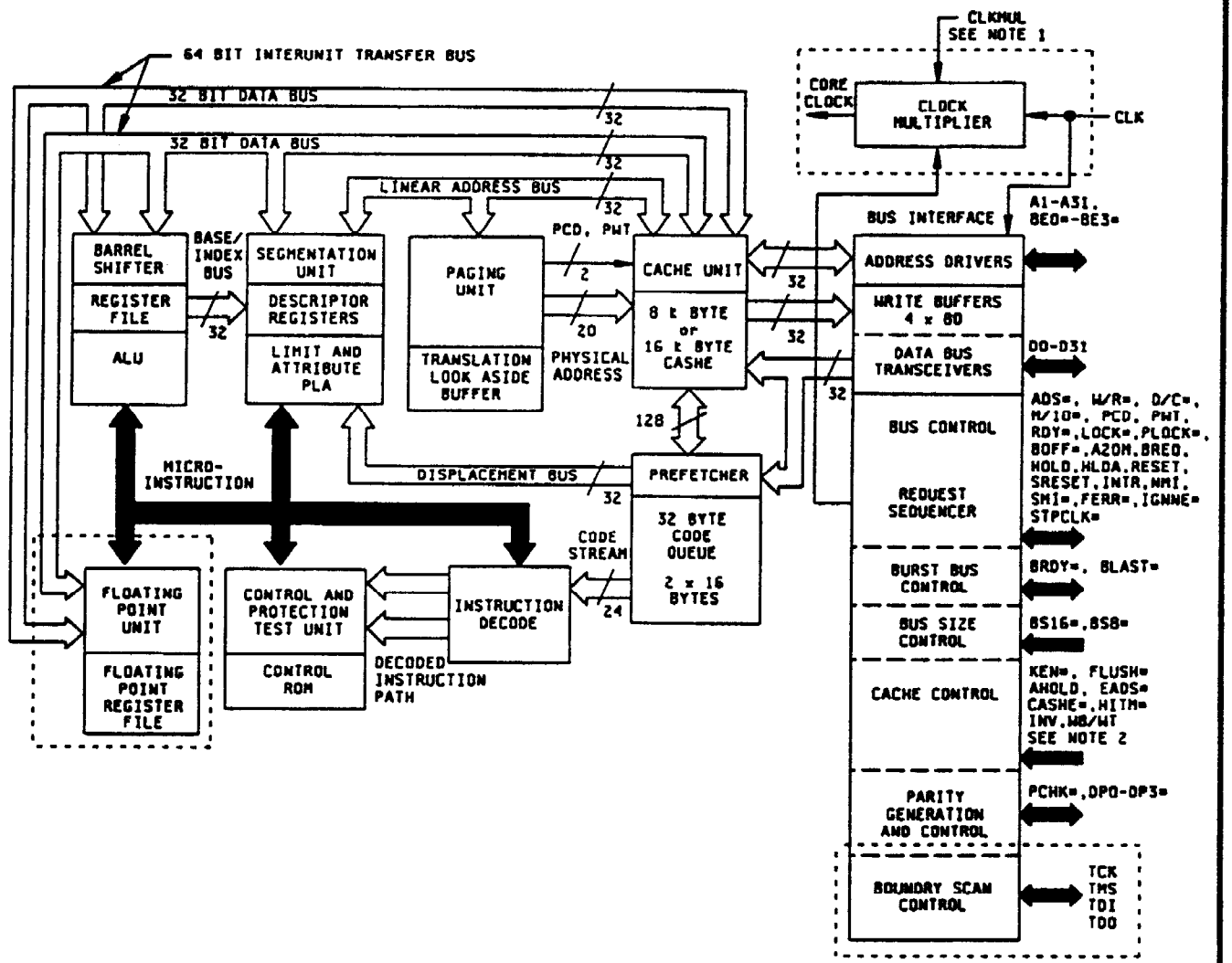
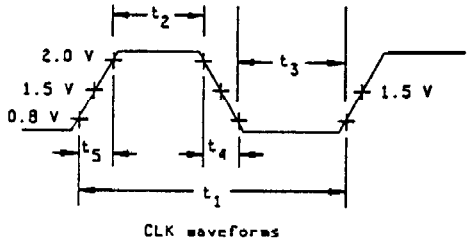
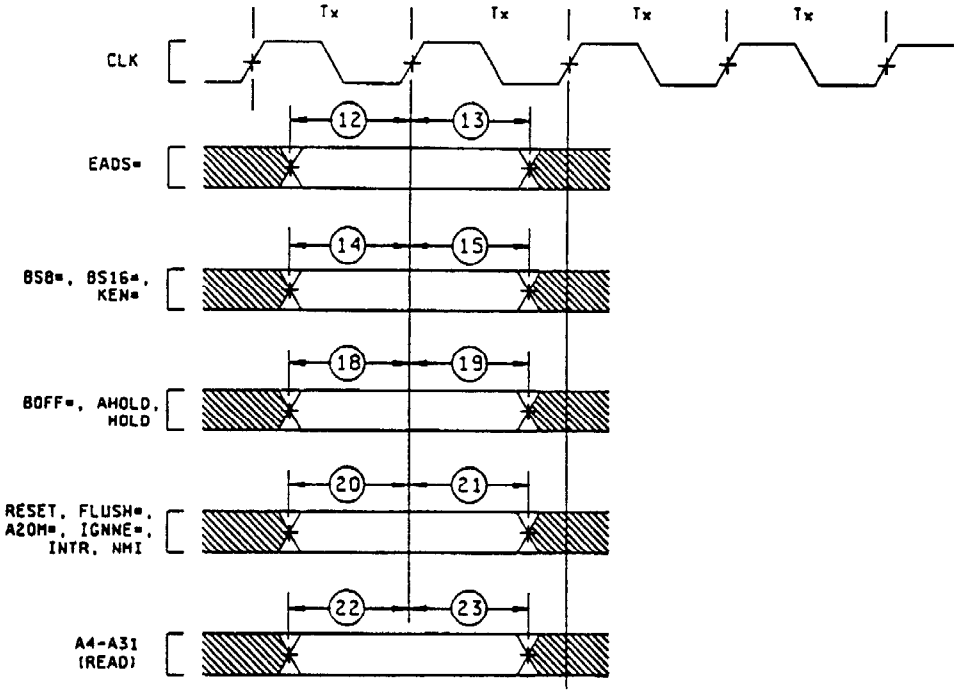


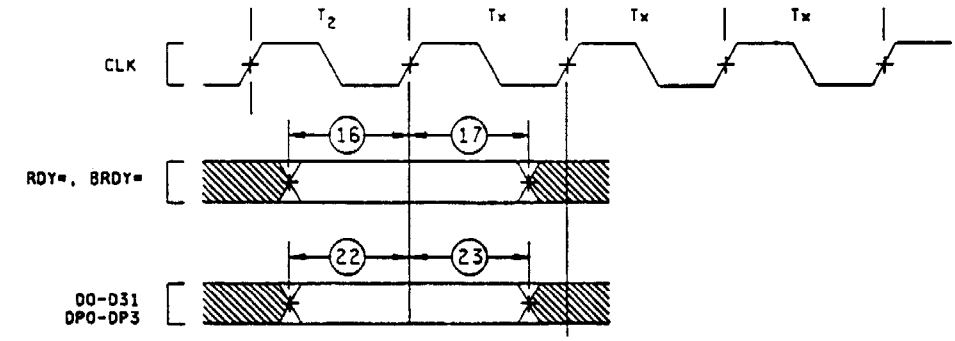
FIGURE 3. Block Diagram



CLK waveforms

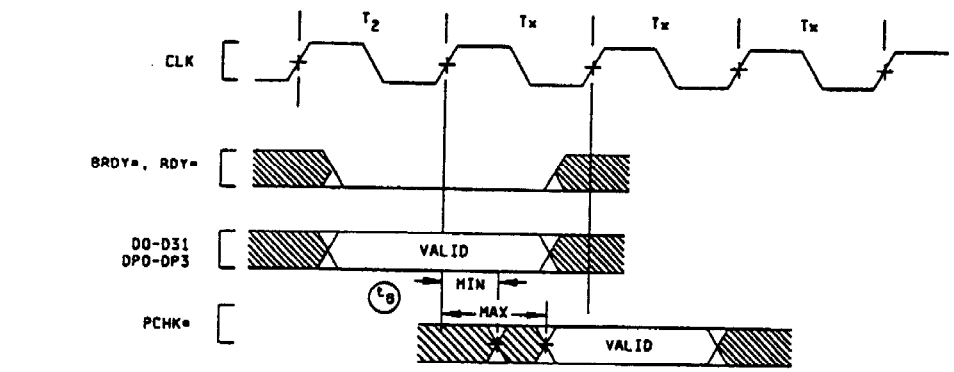


Input setup and hold timing

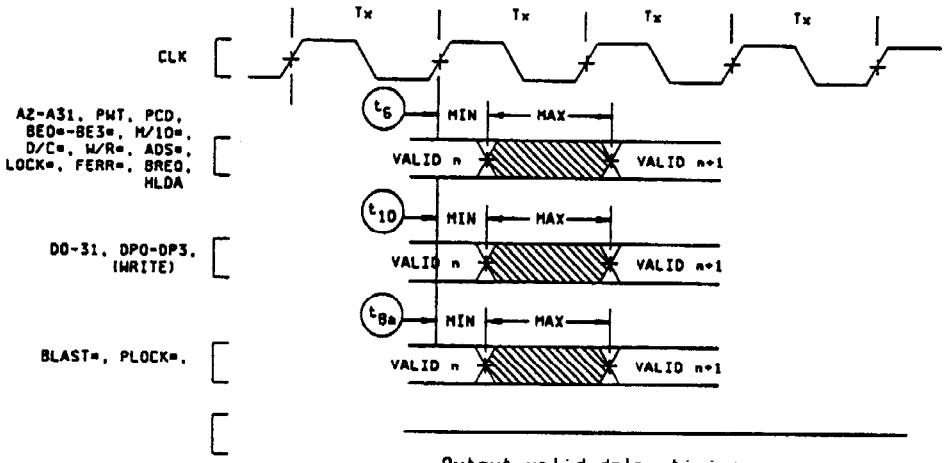


Input setup and hold timing

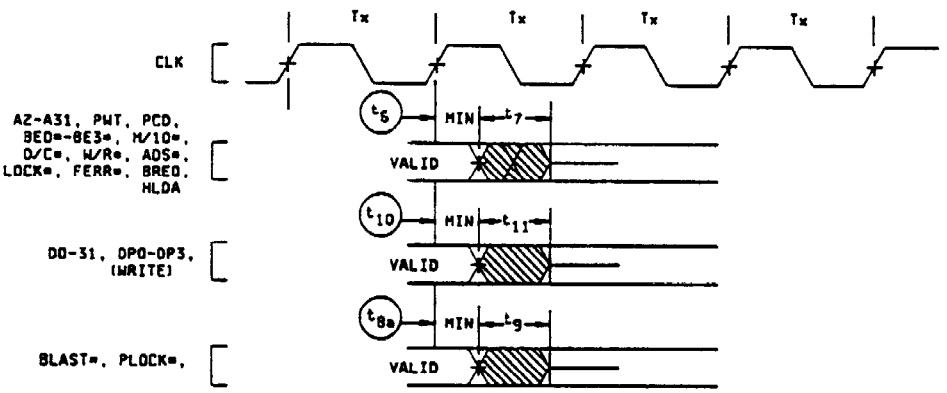
FIGURE 4. Switching waveforms.



PCHK= valid delay timing



Output valid delay timing



Maximum float delay timing

FIGURE 4. Switching waveforms - Continued

Instruction Codes	Instruction Name
0000	EXTEST
0001	SAMPLE
0010	ICODE
0011	PRIVATE
0100	PRIVATE
0101	PRIVATE
0110	PRIVATE
0111	PRIVATE
1000	RUNBIST
1001	PRIVATE
1010	PRIVATE
1011	PRIVATE
1100	PRIVATE
1101	PRIVATE
1110	PRIVATE
1111	BYPASS

FIGURE 5. Boundry scan instruction codes

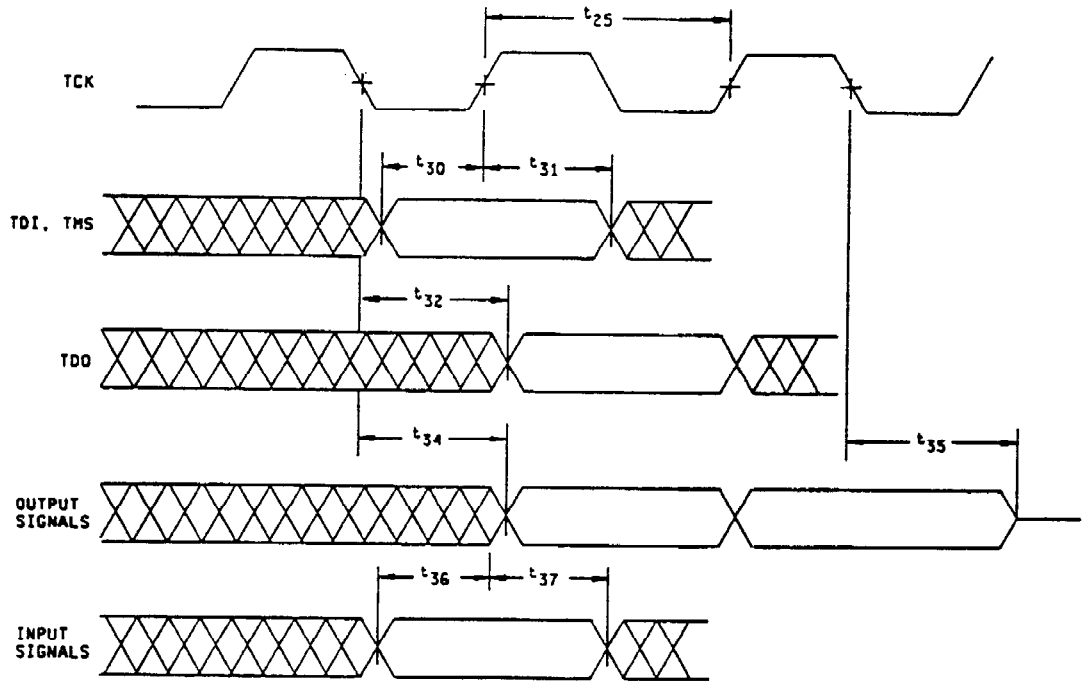


FIGURE 5. Boundry scan instruction codes - Continued

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-I-38535, table III)		
	Device class N	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - -		
Final electrical parameters (see 4.2)	1,2,3,7,8,9 1/ 10,11	1,2,3,7,8, 1/ 9,10,11	1,2,3,7,8, 2/ 9,10,11
Group A test requirements (see 4.4)	1,2,3,4,7,8,9, 10,11	1,2,3,4,7,8,9, 10,11	1,2,3,4,7,8, 9,10,11
Group C end-point electrical parameters (see 4.4)	2, 8a, 10	2, 8a, 10	2, 8a, 10
Group D end-point electrical parameters (see 4.4)	2, 8a, 10	2, 8a, 10	2, 8a, 10
Group E end-point electrical parameters (see 4.4)			

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4 Conformance inspection. Technology conformance inspection for classes N, Q, and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device classes N, Q, and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_{CLK}, C_{IN}, $C_{I/O}$ and C_O measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters for device classes N, Q, and V shall be as specified in table II herein.

4.4.2.1 Additional criteria. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters for device classes N, Q, and V shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes N, Q, and V shall be M, D, R, and H.

a. End-point electrical parameters shall be as specified in table II herein.

b. The devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging for device classes N, Q, and V shall be in accordance with MIL-I-38535.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331.

TABLE III. Pin descriptions.

Symbol	Type	Function
CLK	I	Clock provides the fundamental timing and the internal operating frequency for the device. All external timing parameters are specified with respect to the rising edge of CLK.
ADDRESS BUS		
A31-A4 A2-A3	I/O O	A31-A2 are the address lines of the microprocessor. A31-A2, together with the byte enables BE0#-BE3#, define the physical area of memory or input/output space accessed. Address lines A31-A4 are used to drive addresses into the microprocessor to perform cache line invalidations. Input signals must meet setup and hold times t_{22} and t_{23}. A31-A2 are not driven during bus or address hold.
BE0-3#	I/O	The byte enable signals indicate active bytes during read and write cycles. During the first cycle of a cache fill, the external system should assume that all byte enables are active. BE3# applies to D24-D31, BE2# applies to D16-D23, BE1# applies to D8-D15 and BE0# applied to D0-D7, BE0#-BE3# are active LOW and are not driven during bus hold.
DATA BUS		
D31-D0	I/O	These are the data lines for the device. Lines D0-D7 define the least significant byte of the data bus while lines D24-D31 define the most significant byte of the data bus. These signals must meet setup and hold times t_{22} and t_{23} for proper operation on reads. These pins are driven during the second and subsequent clocks of write cycles.
DATA PARITY		
DP0-DP3	I/O	There is one data parity pin for each byte of the data bus. Data parity is generated on all write data cycles with the same timing as the data driven by the device. Even parity information must be driven back into the microprocessor on the data parity pins with the same timing as read information to insure that the correct parity check status is indicated by the device. The signals read on these pins do not affect program execution. Input signals must meet setup and hold times t_{22} and t_{23}. DP0-DP3 should be connected to V_{CC} through a pullup resistor in systems which do not use parity. DP0-DP3 are active HIGH and are driven during the second and subsequent clocks of write cycles.
PCHK#	O	Parity status is driven on the PCHK# pin the clock after ready for read operations. The parity status is for data sampled at the end of the previous clock. A parity error is indicated by PCHK# being LOW. Parity status is only checked for enabled bytes as indicated by the byte enable and bus sized signals. PCHK# is valid only in the clock immediately after read data is returned to the microprocessor. At all other times PCHK# is inactive (HIGH). PCHK# is never floated.
BUS CYCLE DEFINITION		
M/IO# D/C# W/R#	O O O	The memory/input-output, data/control and write/read lines are the primary bus definition signals. These signals are driven valid as the ADS# signal is asserted. M/IO# D/C W/R BUS CYCLE INITIATED 0 0 0 Interrupt Acknowledge 0 0 1 Halt/Special Cycle 0 1 0 I/O Read 0 1 1 I/O Write 1 0 0 Code Read 1 0 1 Reserved 1 1 0 Memory Read 1 1 1 Memory Write The bus definition signals are not driven during bus hold and follow the timing of the address bus.

TABLE III. Pin descriptions - Continued.

Symbol	Type	Function
LOCK#	O	The bus lock pin indicates that the current bus cycle is locked. The device will not allow a bus hold when LOCK# is asserted (but address holds are allowed). LOCK# goes active in the first clock of the first locked bus cycle and goes inactive after the last clock of the last locked bus cycle. The last locked cycle ends when ready is returned. LOCK# is active LOW and is not driven during bus hold. Locked read cycles will not be transformed into cache fill cycles if KEN# is returned active.
PLOCK#	O	The Pseudo-lock pin indicates that the current bus transaction requires more than one bus cycle to complete. Examples of such operations are floating point long reads and writes (64 bits), segment table descriptor reads (64 bits), segment table descriptor reads (64 bits),in addition to cache line fills (128 bits). The device will drive PLOCK# active until the addresses for the last bus cycle of the transaction have been driven regardless of whether RDY# or BRDY# have been returned. Normally PLOCK# and BLAST# are inverse of each other. However, during the first bus cycle of a 64-bit floating point write, both PLOCK# and BLAST# will be asserted PLOCK# is a function of the BS8#, BS16#, and KEN# inputs. PLOCK# should be sampled only in the clock ready is returned. PLOCK# is active LOW and is not driven during bus hold.
BUS CONTROL		
ADS#	O	The address status output indicates that a valid bus cycle definition and address are available on the cycle definition lines and address bus. ADS# is driven active in the same clock as addresses are driven. ADS# is active LOW and is not driven during bus hold.
RDY#	I	The non-burst ready input indicates that the current bus cycle is complete. RDY# indicates that the external system has presented valid data on the data pins in response to a read or that the external system has accepted data from the device in response to a write, RDY# is ignored when the bus is idle and at the end of the first clock of the bus cycle. RDY# is active LOW, and is not provided with an internal pullup resistor. RDY# must satisfy setup and hold times t_{16} and t_{17} for proper chip operation. RDY# is active during address hold. Data can be returned to the processor while AHOLD is active.
BURST CONTROL		
BRDY#	I	The burst ready input performs the same function during a burst cycle that RDY# performs during a non-burst cycle. BRDY# is ignored when the bus is idle at the end of the first clock in a bus cycle. BRDY# is sampled in the second and subsequent clocks of a burst cycle. The data presented on the data bus will be strobed into the microprocessor when BRDY# is sampled active. If RDY# is returned simultaneously with BRDY#, BRDY# is ignored and the burst cycle is prematurely aborted. BRDY# is active LOW and is provided with a small pullup resistor. BRDY# must satisfy the setup and hold times t_{16} and $_{17}$.
BLAST#	O	The burst last signal indicates that the next time BRDY# is returned the burst bus cycle is complete. BLAST# is active for both burst and non-burst bus cycles. BLAST# is active LOW and is not driven during bus hold.
INTERRUPTS		
RESET	I	The reset input forces the device to begin execution at a known state. The microprocessor cannot begin execution of instructions until at least 1ms after V_{CC} and CLK have reached their proper DC and AC specifications. The RESET pin should remain active during this time to insure proper microprocessor operation. RESET is active HIGH. RESET is asynchronous but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.

TABLE III. Pin descriptions - Continued.

Symbol	Type	Function
INTR	I	The maskable interrupt indicates that an external interrupt has been generated. If the internal interrupt flag is set in EFLAGS, active interrupt processing will be initiated. The device will generate two locked interrupt acknowledge bus cycles in response to the INTR pin going active. INTR must remain active until the interrupt acknowledges have been performed to assure that the interrupt is recognized. INTR is active HIGH and is not provided with an internal pulldown resistor. INTR is asynchronous, but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.
NMI	I	The non-maskable interrupt request signal indicates that an external non-maskable interrupt has been generated. NMI is rising edge sensitive. NMI must be held LOW for at least four CLK periods before this rising edge. NMI is not provide with an internal pulldown resistor. NMI is asynchronous, but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.
BUS ARBITRATION		
BREQ	O	The internal cycle pending signal indicates that the device has internally generated a bus request. BREQ is generated whether or not the device is driving the bus. BREQ is active HIGH and is never floated.
HOLD	I	The bus hold request allows another bus master complete control of the device bus. In response to HOLD going active the device will float most of its output and input/output pins. HLDA will be asserted after completing the current bus cycle, burst cycle or sequence of locked cycles. The device will remain in this state until HOLD is deasserted. HOLD is active high and is not provided with an internal pulldown resistor. HOLD must satisfy setup and hold times $_{18}$ and $_{19}$ for proper operation.
HLDA	O	Hold acknowledge goes active in response to a hold request presented on the HOLD pin. HLDA indicates that the device has given the bus to another local bus master. HLDA is driven active in the same clock that the device floats its bus. HLDA is driven inactive when leaving bus hold. HLDA is active HIGH and remains driven during bus hold.
BOFF#	I	The backoff input forces the device to float its bus in the next clock. The microprocessor will float all pins normally floated during bus hold but HLDA will not be asserted in response to BOFF#. BOFF# has higher priority than RDY# or BRDY#; if both are returned in the same clock, BOFF# takes effect. The microprocessor remains in bus hold until BOFF# is negated. If a bus cycle was in progress when BOFF# was asserted the cycle will be restarted. BOFF# is active LOW and must meet setup and hold times t_{18} and t_{19} for proper operation.
CACHE INVALIDATION		
AHOLD	I	The address hold request allows another bus master access to the device address bus for a cache invalidation cycle. The device will stop driving its address bus in the clock following AHOLD going active. Only the address bus will be floated during address hold, the remainder of the bus will remain active. AHOLD is active HIGH and is provided with a small internal pulldown resistor. For proper operation AHOLD must meet setup and hold times t_{18} and t_{19}.
EADS#	I	This signal indicates that a valid external address has been driven onto the device microprocessor address pins. This address will be used to perform an internal cache invalidation cycle. EADS# is active LOW and is provided with an internal pullup resistor EADS# must satisfy setup and hold times t_{12} and t_{13} for proper operation.

TABLE III. Pin descriptions - Continued.

Symbol	Type	Function
CACHE CONTROL		
KEN#	I	The cache enable pin is used to determine whether the current cycle is cacheable. When the device generates a cycle that can be cached and KEN# is active, the cycle will become a cache line fill cycle. Returning KEN# active one clock before ready during the last read in the cache line fill will cause the line to be placed in the on-chip cache. KEN# is active LOW and is provided with a small internal pullup resistor. KEN# must satisfy setup and hold times t_{14} and t_{15} for operation.
FLUSH#	I	The cache flush input forces the device to flush its entire internal cache. FLUSH# is active low and need only be asserted for one clock. FLUSH# is asynchronous but setup and hold times t_{20} and t_{21} must be met before the falling edge of RESET caused the device to enter the tri-state test mode.
PAGE CACHEABILITY		
PWT PCD	O O	The page write-through and page cached disable pins reflect the state of the page attribute bits. PWT and PCD, in the page table entry or page directory entry. If paging is disabled or for cycles that are not paged, PWT and PCD reflect the state of the PWT and PCD bits in control register 3. PWT and PCD have the same timing as the cycle definition pins(M/IO#, D/C# and W/R#). PWT and PCD are active HIGH and are not driven during bus hold. PCD is masked by the cache disable bit (CD) in Control Register 0.
NUMERIC ERROR REPORTING		
FERR#	O	The floating point error pin is driven active when a floating point error occurs. FERR# is included for compatibility with systems using DOS type floating point error reporting. FERR# will not go active if FP errors are masked in FPU register. FERR# is active LOW, and is not floated during bus hold.
IGNNE#	I	When the ignore numeric error pin is asserted the device will ignore a numeric error and continue executing non-control floating point instructions, but FERR# will still be activated by the device. When IGNNE# is deasserted the device will freeze on a non-control floating point instruction, if a previous floating point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 is set. IGNNE# is active LOW and is provided with a small internal pullup resistor. IGNNE# is asynchronous but setup and hold times t_{20} and t_{21} must be met to insure recognition on any specific clock.
BUS SIZE CONTROL		
BS16# BS8#	I I	The bus size 16 and bus size 8 pins (bus sizing pins) cause the device to run multiple bus cycles to complete a request from devices that cannot provide or accept 32 bits of data in a single cycle. The bus sizing pins are sampled every clock. The state of these pins in the clock before ready is used by the device to determine the bus size. These signals are active LOW and are provided with internal pullup resistors. These inputs must satisfy setup and hold times t_{14} and t_{15} for proper operation.
SRESET	I	The soft reset pin duplicates all the functionality of the RESET pin with the following exception: 1. The SMBASE register will retain its previous value. For soft resets, SRESET should remain active for at least 15 CLK periods. SRESET is active HIGH, SRESET is asynchronous but must meet setup and hold times t_{20} and t_{21} for recognitions in any specific clock.
$\overline{\text{SMI}}$	I	The system management interrupt input is used to invoke the system management mode (SMM). SMI# is a falling edge triggered signal which forces the processor into SMM at the completion of the current instruction. SMI# is recognized on an instruction boundary and at each iteration for repeat string instructions. SMI# does not break LOCKed bys cycles and cannot interrupt a currently executing SMM. The processor will latch the falling edge of one pending SMI# signal while the processor is executing and existing SMI#. The nested SMI# will not be recognized until after the execution of a Resume (RSM) instruction.

SMIACT#	O	The system management interrupt active is an active low output, indicating that the processor is operating in SMM. It is asserted when the processor begins to execute the SMI state save sequence and will remain active LOW until the processor executes the last state restore cycle out of SMRAM.
STPCLK#	I	The stop clock request input signal indicates a request has been made to turn off the CLK input. When the processor recognizes a STPCLK#, the processor will stop execution on the next instruction boundary, unless superseded by a higher priority interrupt, empty all internal pipelines and the write buffers and generate a stop grant acknowledge bus cycle. STPCLK# is an asynchronous signal, but must remain active until the processor issurs the stop grant bus cycle. STPCLK# may be deasserted at any time after the processor has issued the stop grant bus cycle.
A20M#	I	When the address bit 20 mask pin is asserted, the device masks physical address bit 20 (A20) before performing a lookup to the internal cache or driving a memory cycle on the bus. A20M# emulates the address wraparound at one Mbyte, which occurs on the 8086 processor.. A20M# is active LOW and should be asserted only when the processor is in real mode. This pin is asynchronous but should beet setup and hold times t_{20} and t_{21} for recognition in any specific clock. For proper operation, A20M# should be sampled high at the falling edge of RESET.
TCK	I	Test clock is an input to the device and provides the clocking function required by the JTAG boundry scan feature. TCK is used to clock state information and data into component on the rising edge of TCK on TMS and TDI, respectively. Data is clocked out of the part on the falling edge of TCK and TDO. TCK is provided with an internal pull-up resistor.
TDI	I	Test data input is the serial input used to shift JTAG instructions and data into component. TDI is sampled on the rising edge of TCK, during the SHIFT-IR and SHIFT-DR TAP controller states. During all other tap controller states, TDI is a "don't care". TDI is provided with an internal pull-up resistor.
TDO	O	Test data output is the serial output used to shift JTAG instructions and data out of the component. TDO is driven on the falling edge of TCK during shift_IR and SHIFT-DR tap controller states. At all other times TDO is driven to the high impedance state.
TMS	I	Test select mode is decoded by JTAG TAP (test access port) to select the opoeration of the test logic. TMS is sampled on the rising edge of TCK. To guarantee deterministic behavior of the TAP controller TMS is provided with an internal pull-up resistor.
WB/WT#	I	The write back/write through pin enables enhanced bus mode (write-back cache). It also defines a cached line as write-through or write-back. For cache configuration, WB/WT# must be valid during RESET and be active for at least two clocks before and two clocks after RESET is de-asserted. To define write-back or write-through configuration of a line, WB/WT# is sampled in the same clock as the first RDY# or BRDY# is returned during a line fill (allocation) cycle.
CLKMUL	I	The clock multiplier input, defined during device RESET, defines the ratio of internal core frequency to external bus frequency. If sampled low, the core frequency operates at twice the external bus frequency(speed doubled mode). If driven high or left floating, speed triple mode is selected. CLKMUL has an internal pull-up speed to V_{CC} and may be left floating in designs that select speed tripled clock mode.
V_{CC5}	I	The 5v reference voltage input is the referenced voltage for the 5v-tolerant I/O buffers. This signal shoul be connected to +5V ±5% for use with 5 v logic. If all inputs are from 3V logic, this pin should be connected to 3.3V.
VOLDET	O	A voltage detect signal allows external system logic to distinguish between a 5v device and a 3v device. This signal is active low for a 3.3v device. This pin is available only on the PGA version of the device.
CACHE#	O	The cache# output indicates internally cacheable on read cycles and burst write-back on write cycles. CACHE# is asserted for cacheable reads, cacheable code fetches and write-backs. It is driven inactive for non-cacheable reads, I/O cycles, special cycles, and write-through cycles.

FLUSH#	I	Cache flush# is an existing pin that operates differently if the processor is configured as enhanced bus mode (write-back). Flush# will cause the processor to write-back all modified lines and flush (invalidate) the cache. FLUSH# is asynchronous, but must meet setup and hold times t_{20} and t_{21} for recognitions in any specific clock.
HITM#	O	The hit/miss to a modified line pin is a cache coherency protocol pin that is driven only in enhanced bus mode. When a snoop cycle is run, HITM# indicates that the processor contains the snooped line and that the line has been modified. Assertion of HITM# implies that the line will be written back in its entirety, unless the processor is already in the process of doing a replacement write-back of the same line.
INV	I	The invalidation request pin is a cache coherency protocol pin that is used only in the enhanced bus mode. It is sampled by the processor on EADS#-driven snoop cycles. It is necessary to assert this pin to get the effect of the processor invalidate cycle on write-through-only lines. INV invalidates the write-back lines. However, if the snooped line is modified the line will be written back and then invalidate. INV must satisfy setup and hold times t_{12} and t_{13} for proper operation.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(N, Q, or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply. Sources of supply for device classes N, Q, and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 95-11-22

Approved sources of supply for SMD 5962-95837 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standard microcircuit drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-9583701QXA	34369	MG80486DX4-75/Q
5962-9582701QYA	34369	MQ80486DX4-75/Q
5962-9583702QXA	34369	MG80486DX4-100/Q
5962-9583702QYA	34369	MQ80486DX4-100/Q
5962-9583703NXA	34369	VA80486DX4-75/Q
5962-9583703NYA	34369	VQ80486DX4-75/Q
5962-9583704NXA	34369	VA80486DX4-100/Q
5962-9583704NYA	34369	VQ80486DX4-100/Q
5962-9583705NXA	34369	TA80486DX4-75/Q
5962-9583705NYA	34369	TQ80486DX4-75/Q
5962-9583706NXA	34369	TA80486DX4-100/Q
5962-9583706NYA	34369	TQ80486DX4-100/Q

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34369	Intel Corportation 2200 Mission College Blvd. P.O. Box 58119 Santa Clara, CA 95052-8119 Point of Contact: 5000 W. Chandler Blvd Chandler, AZ 85226