NOTICE OF REVISION (NOR)

This revision described below has been authorized for the document listed.

1. DATE (YYMMDD): 95-02-10

Form Approved OMB No. 0704-0188

2. PROCURING ACTIVITY NO.

3. DODAAC

4. ORIGINATOR	b. ADDRESS (Street, City, State, Zip Code)	5. CAGE CODE	6. NOR NO.
a. TYPED NAME (First, Middle Initial, Last)	Defense Electronics Supply Center 1507 Wilmington Pike Dayton, OH 45444-5765	7. CAGE CODE 67268	8. DOCUMENT NO. **5962-90548**
		67268	5962-R069-95

9. TITLE OF DOCUMENT	10. REVISION LETTER		11. ECP NO.
MICROCIRCUIT, DIGITAL, CMOS, SCSI BUS CONTROLLER, MONOLITHIC SILICON	a. CURRENT Initial	b. NEW A	

12. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES

All

13. DESCRIPTION OF REVISION

Sheet 1: Revisions ltr column; add "A".
Revisions description column; add "Changes in accordance with NOR 5962-R069-95".
Revisions date column; add "95-02-10".
Revision level block; add "A".
Rev status of sheets; For sheets 1, 5, 6, 7, 8, 14 add "A".

Sheet 5: Change Supply currrent quiescent I_{CC} from: 1.0 mA to: 1.5 mA
Change status of revision level to "A"

Sheet 6: Change DACK false to ACK true (REQ true), t8, from: 140 ns to: 185 ns
Change status of revision level to "A"

Sheet 7: Change IOW false to ACK true (REQ true), t8, from: 140 ns to: 185 ns
Change status of revision level to "A"

Sheet 8: Change DACK false to REQ true (ACK false), t8, from: 140 ns to: 185 ns
Change IOW false to REQ true (ACK false), t8, from: 140 ns to: 185 ns
Change status of revision level to "A"

Sheet 14: Change note from: SCSI bus outputs to: SCSI bus and outputs
Change note from: Pin's 2-10 to: Pin's 2-10, 12-20
Change status of revision level to "A"

14. THIS SECTION FOR GOVERNMENT USE ONLY

a. (X one)		
	X	(1) Existing document supplemented by the NOR may be used in manufacture.
		(2) Revised document must be received before manufacturer may incorporate this change.
		(3) Custodian of master document shall make above revision and furnish revised document.

b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT	c. TYPED NAME (First, Middle Initial, Last)
DESC-ELDC	Monica L. Poelking

d. TITLE	e. SIGNATURE	f. DATE SIGNED (YYMMDD)
Chief, Custom Microelectronics Branch	Monica L. Poelking	95-02-10

15a. ACTIVITY ACCOMPLISHING REVISION	b. REVISION COMPLETED (Signature)	c. DATE SIGNED (YYMMDD)
DESC-ELDC	Thomas M. Hess	95-02-10

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25								

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Thomas M. Hess

CHECKED BY
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APPROVED BY
Tim H. Noh

DRAWING APPROVAL DATE
92-06-25

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS, SCSI
BUS CONTROLLER, MONOLITHIC SILICON

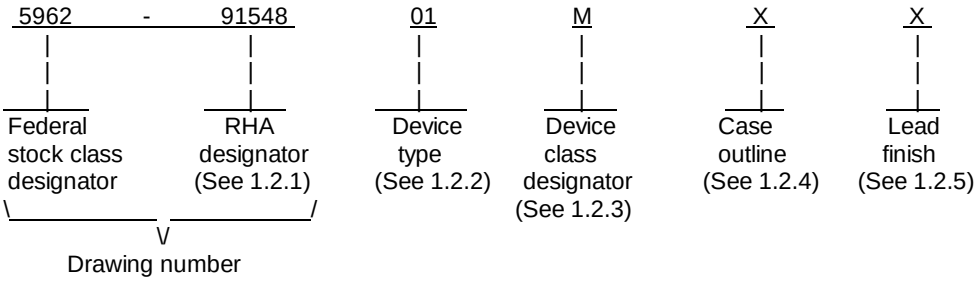
SIZE	CAGE CODE	
A	**67268**	**5962-90548**

SHEET 1 OF 25

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Frequency
01	L5380	SCSI Bus controller	2 MHz
02	L53C80	SCSI Bus controller	2 MHz

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). For device classes M, B, and S, case outline(s) shall meet the requirements in appendix C of MIL-M-38510 and as listed below. For device classes Q and V, case outline(s) shall meet the requirements of MIL-I-38535, appendix C of MIL-M-38510, and as listed below.

Outline letter	Case outline
Q	D-5 (40-Lead, 2.096" x .620" x .225") dual-in-line package
X	C-5 (44-terminal, .662" x .662" x .120") leadless chip carrier
Y	D-14 (48-Lead, 2.435" x .620" x .225") dual-in-line package

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Storage temperature	-65°C to +150°C
V_{CC} supply voltage respect to ground	-0.5 V to +7.0 V
Output voltage	0.0 to V_{CC}
Input voltage	0.0 to 5.5 V
I_{OL} Low level output current (SCSI bus)	48 mA
I_{OL} Low level output current (other pins)	8 mA
I_{OH} High level output current (other pins)	-4 mA
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-M-38510, appendix C
Power dissapation (P_D)	55 mW
Lead temperature (soldering, 10 seconds)	275°C

1.4 Recommended operating conditions.

Supply voltage	4.50 V $\leq$ V_{CC} $\leq$ 5.50 V
Case operating temperature	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 2/

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Values will be added when they become available.

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block or logic diagram. The block or logic diagram shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-ECC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Electrical characteristic							
Low level input voltage	V_{IL}		1, 2, 3	All	0.0	0.8	V
High level input voltage	V_{IH}		1, 2, 3	All	2.0	V_{CC}	V
Low level output voltage (SCSI bus)	V_{OL}	V_{CC} = Min, I_{OL} = 48 mA	1, 2, 3	All		0.5	V
Low level output voltage (other pins)	V_{OL}	V_{CC} = Min, I_{OL} = 8 ma	1, 2, 3	All		0.5	V
High level output voltage (other pins)	V_{OH}	V_{CC} = Min, I_{OH} = -4 mA	1, 2, 3	All	3.5		V
Input current	I_{IN}	V_{CC} = Max, V_{IN} = 0 -V_{CC} (SCSI bus) 3/	1, 2, 3	All		65	μA
Input current	I_{IN}	V_{CC} = Max, V_{in} = 0 - V_{CC} (other pins) 3/	1, 2, 3	All		20	μA
Supply current	I_{CC}	V_{CC} = Max, V_{IH} = 2.4 V_{IL} = 0.4, 4 MHz cycle, No load, No termination	1, 2, 3	All		20	mA
Supply current quiescent	I_{CC}	V_{CC} = Max, V_{IH} = 2.4 V_{IL} = 0.4, 4 MHz inputs stable	1, 2, 3	All		1.0	mA
Input capacitance	C_I	See 4.4.1.c	4	All		10	pF
Output capacitance	C_O	See 4.4.1.c	4	All		10	pF
Functional test		See 4.4.1.b V_{CC} = 4.5V, 5.5V	7, 8	All			
Switching characteristics aribitration timing							
BSY False duration to detect bus free condition	t1	V_{CC} = 4.5V See figure 3	9, 10, 11	All	0.4	1.2	μs
SCSI Bus clear (high Z) from BSY false	t2		9, 10, 11	All		1.2	μs
Arbitate (BSY and SCSI ID asserted) from BSY false (bus free detected)	t3		9, 10, 11	All	0.8	2.4	μs
SCSI Bus clear (high Z) from SEL true (lost arbiration)	t4		9, 10, 11	All		60	ns
CPU Write cycle timing							
Address setup to write enable	t1		9, 10, 11	All	10		ns
Address hold from end of write enable	t2		9, 10, 11	All	5		ns

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Width of write enable	t3	V_{CC} = 4.5 V See figure 3	9, 10, 11	All	40		ns
Data setup to end of write enable	t4		9, 10, 11	All	20		ns
Data hold from end of write enable	t5		9, 10, 11	All	10		ns
CPU Read cycle timing							
Address setup to read enable	t1		9, 10, 11	All	10		ns
Address hold from end of read enable	t2		9, 10, 11	All	5		ns
Data access time from read enable	t3		9, 10, 11	All		50	ns
DMA Write initiator send timing							
The following apply for all DMA mode							
DRQ False from write enable (concurrence of IOW and DACK	t1		9, 10, 11	All		60	ns
Width of write enable (concurrence of IOW and DACK	t2		9, 10, 11	All	60		ns
Data setup to end of write enable	t4		9, 10, 11	All	20		ns
Data hold from end of write enable	t5		9, 10, 11	All	15		ns
Concurrent width of EOP, IOW, and DACK	t6		9, 10, 11	All	50		ns
REQ False to ACK false	t9		9, 10, 11	All		90	ns
End of write enable to valid SCSI data	t13		9, 10, 11	All		65	ns
SCSI Data setup time to ACK true	t14		9, 10, 11	All	60		ns
The following apply for normal DMA mode only							
REQ False to DRQ true	t7		9, 10, 11	All		60	ns
DACK False to ACK true (REQ true)	t8		9, 10, 11	All		140	ns
REQ True to ACK true (DACK false)	t10		9, 10, 11	All		70	ns

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
The following apply for blockmode DMA only							
IOW Recovery time	t3	V_{CC} = 4.5 V See figure 3	9, 10, 11	All	40		ns
IOW False to ACK true (REQ true)	t8		9, 10, 11	All		140	ns
REQ True to ACK true (IOW false)	t10		9, 10, 11	All		70	ns
REQ False to read true	t11		9, 10, 11	All		60	ns
IOW False to ready false	t12		9, 10, 11	All		70	ns
DMA Read initiator receive timing							
The following apply for all DMA modes							
DRQ False from concurrence of IOR and DACK	t1		9, 10, 11	All		60	ns
Data access time from concurrence of IOR and DACK	t3		9, 10, 11	All		60	ns
Concurrent width of EOP,IOR, and DACK	t4		9, 10, 11	All	50		ns
REQ True to ACK true	t7		9, 10, 11	All		70	ns
SCSI Data setup time to REQ true	t12		9, 10, 11	All	20		ns
SCSI Data hold time from REQ true	t13		9, 10, 11	All	15		ns
The following apply for normal DMA mode only							
REQ True to DRQ true	t5		9, 10, 11	All		60	ns
DACK False to ACK false (REQ false)	t6		9, 10, 11	All		90	ns
REQ False to ACK false (DACK false)	t8		9, 10, 11	All		80	ns
The following apply for blockmode DMA only							
IOR Recovery time	t2		9, 10, 11	All	40		ns
IOR False to ACK false (REQ false)	t6		9, 10, 11	All		90	ns

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
REQ False to ACK false (IOR false)	t8	V_{CC} = 4.5 V See figure 3	9, 10, 11	All		80	ns
REQ True to ready true	t9		9, 10, 11	All		60	ns
Ready true to CPU data vaild	t10		9, 10, 11	All		15	ns
IOR False to ready false	t11		9, 10, 11	All		70	ns
DMA Write target send timing							
The following apply for all DMA modes							
DRQ False from write enable (concurrence of IOW and DACK)	t1		9, 10, 11	All		60	ns
Width of write enable (concurrence of IOW and DACK	t2		9, 10, 11	All	60		ns
Data setup to end of write enable	t4		9, 10, 11	All	20		ns
Data hold from end of write enable	t5		9, 10, 11	All	15		ns
Concurrent width of EOP, IOW, and DACK	t6		9, 10, 11	All	50		ns
ACK True to REQ false	t9		9, 10, 11	All		90	ns
End of write enable to valid SCSI data	t13		9, 10, 11	All		60	ns
SCSI Data setup time to REQ true	t14		9, 10, 11	All	60		ns
The following apply for normal DMA mode only							
ACK True to DRQ true	t7		9, 10, 11	All		60	ns
DACK False to REQ true (ACK false)	t8		9, 10, 11	All		140	ns
ACK False to REQ true (DACK false)	t10		9, 10, 11	All		70	ns
The following apply for blockmode DMA only							
IOW Recovery time	t3		9, 10, 11	All	40		ns
IOW False to REQ true (ACK false)	t8		9, 10, 11	All		140	ns

TABLE I. Electrical performace characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
ACK False to REQ true (IOW false)	t10	V_{CC} = 4.5 V See figure 3	9, 10, 11	All		70	ns
ACK True to ready true	t11		9, 10, 11	All		60	ns
IOW False to ready false	t12		9, 10, 11	All		70	ns
DMA Read target receive timing							
The folloeing apply for all DMA modes							
DRQ False from concurrence of IOR and DACK	t1		9, 10, 11	All		60	ns
Data access time from concurrence of IOR and DACK	t3		9, 10, 11	All		60	ns
Concurrent width of EOP,IOP, and DACK	t4		9, 10, 11	All	50		ns
ACK True to REQ false	t7		9, 10, 11	All		70	ns
SCSI Data setup time to ACK true	t12		9, 10, 11	All	20		ns
SCSI Data hold time from ACK true	t13		9, 10, 11	All	15		ns
The following apply for normal DMA mode only							
ACK True to DRQ true	t5		9, 10, 11	All		60	ns
DACK False to REQ true (ACK false)	t6		9, 10, 11	All		90	ns
ACK False to REQ true (DACK false)	t8		9, 10, 11	All		80	ns
The following apply for blockmode DMA only							
IOR Recovery time	t2		9, 10, 11	All	40		ns
IOR False to REQ true (ACK false)	t6		9, 10, 11	All		90	ns
ACK False to REQ true (IOR false)	t8		9, 10, 11	All		80	ns
ACK True to ready true	t9		9, 10, 11	All		60	ns

TABLE I. Electrical performace characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Read true to CPU data valid	t10	V_{CC} = 4.5 V See figure 3	9, 10, 11	All		15	ns
IOR false to ready false	t11		9, 10, 11	All		70	ns

1/ All testing to be performed using worst-case test conditions unless otherwise specified.
2/ The following pins are active low: BSY, IOW, REQ, SEL, DACK, ACK, IOR, EOP, IOP.
3/ Not tested at low temperature extreme.

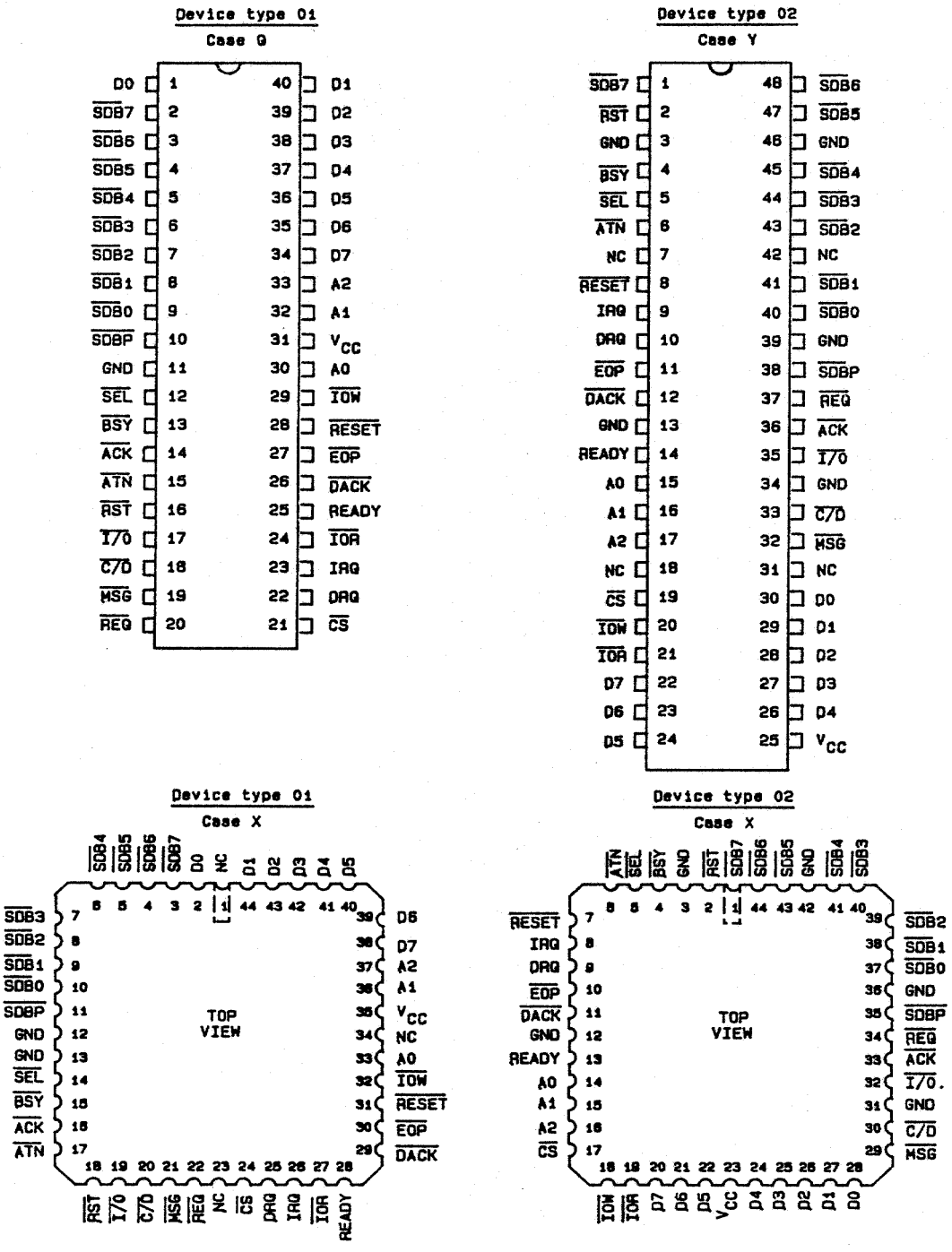


FIGURE 1. Terminal connections.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE **A**		**5962-90548**
		REVISION LEVEL	SHEET **11**

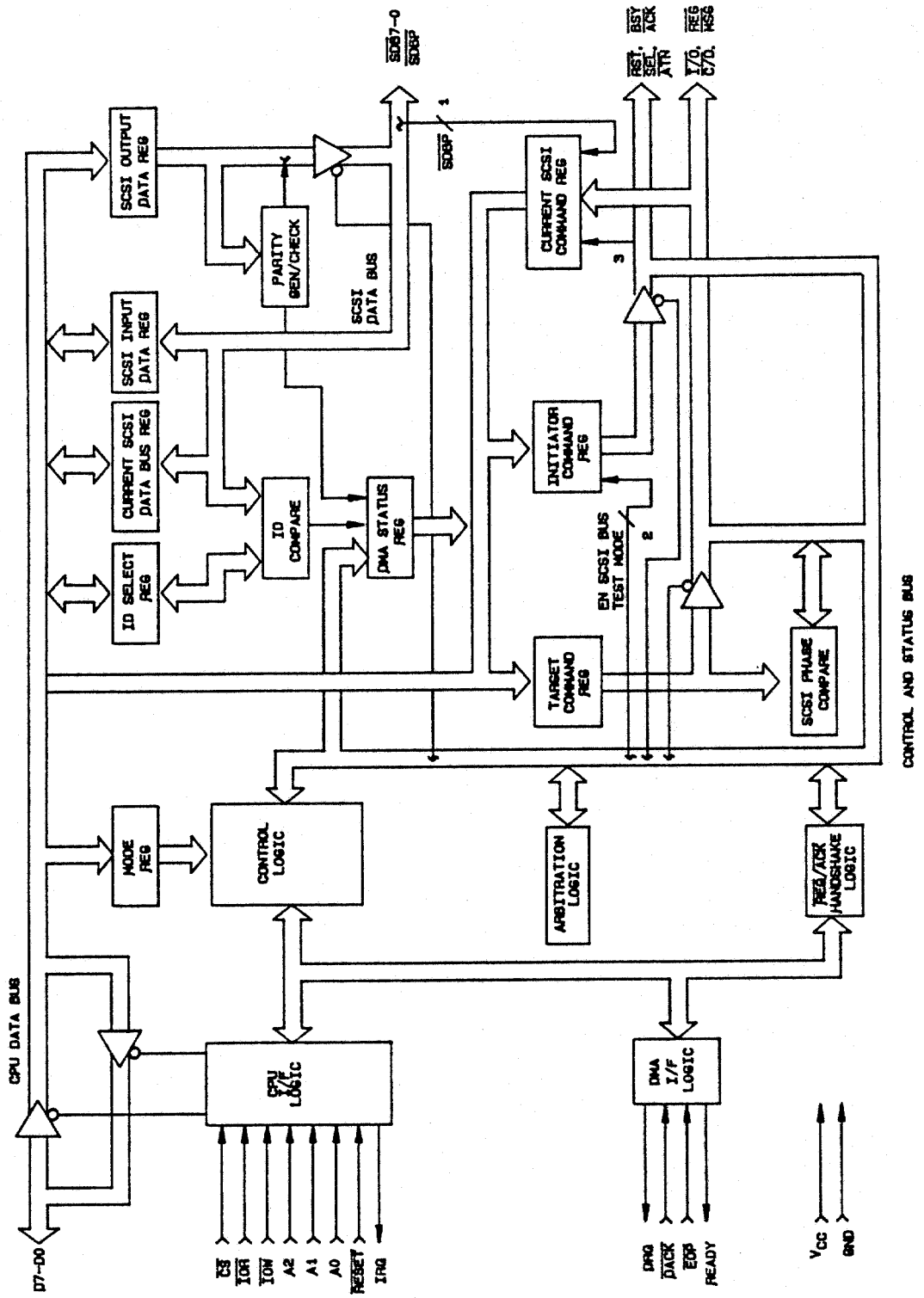
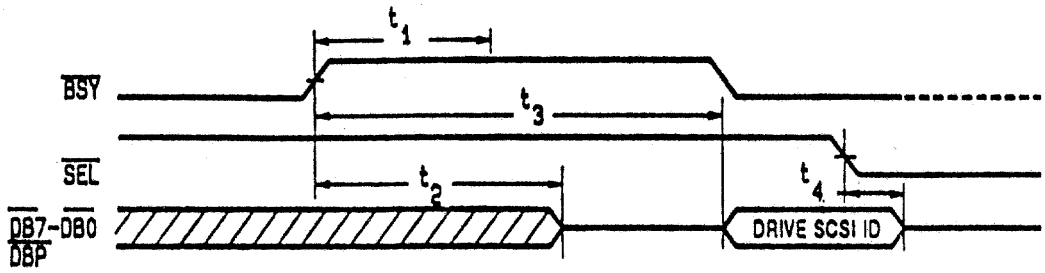


FIGURE 2. Block Diagram.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-90548
		REVISION LEVEL	SHEET 12

Arbitration timing



CPU write cycle timing

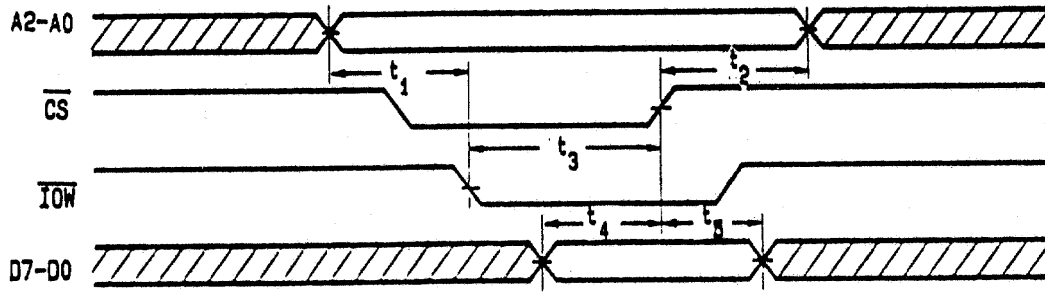
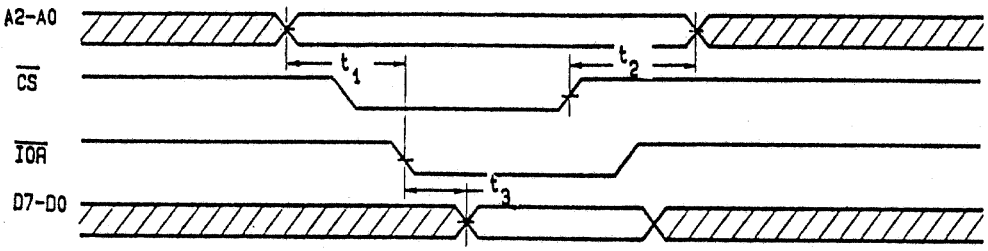
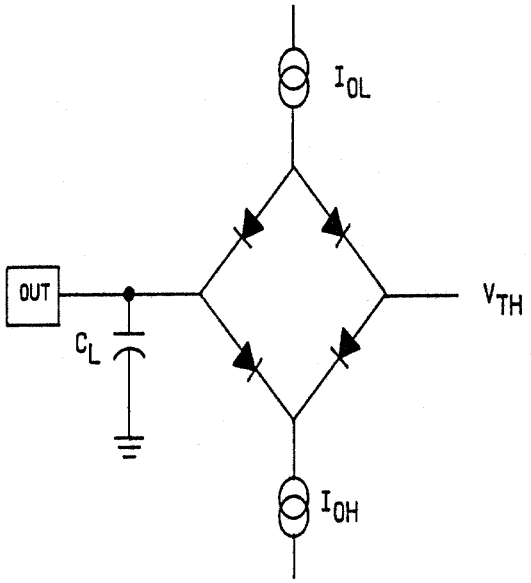


FIGURE 3. Timing waveforms.

CPU read cycle



Output load circuit



NOTE: AC test conditions are as follows:

CPU bus and outputs	Pin's 1,22,23,25,34-40	V_{TH} = 1.5 V	I_{OL} = 8 mA	I_{OH} = -4 mA	C_L = 30 pF
SCSI bus outputs	Pin's 2-10	V_{TH} = 2.5 V	I_{OL} = 24 mA	I_{OH} = 0 mA	C_L = 30 pF

FIGURE 3. Timing waveforms - Continued.

DMA write initiator send

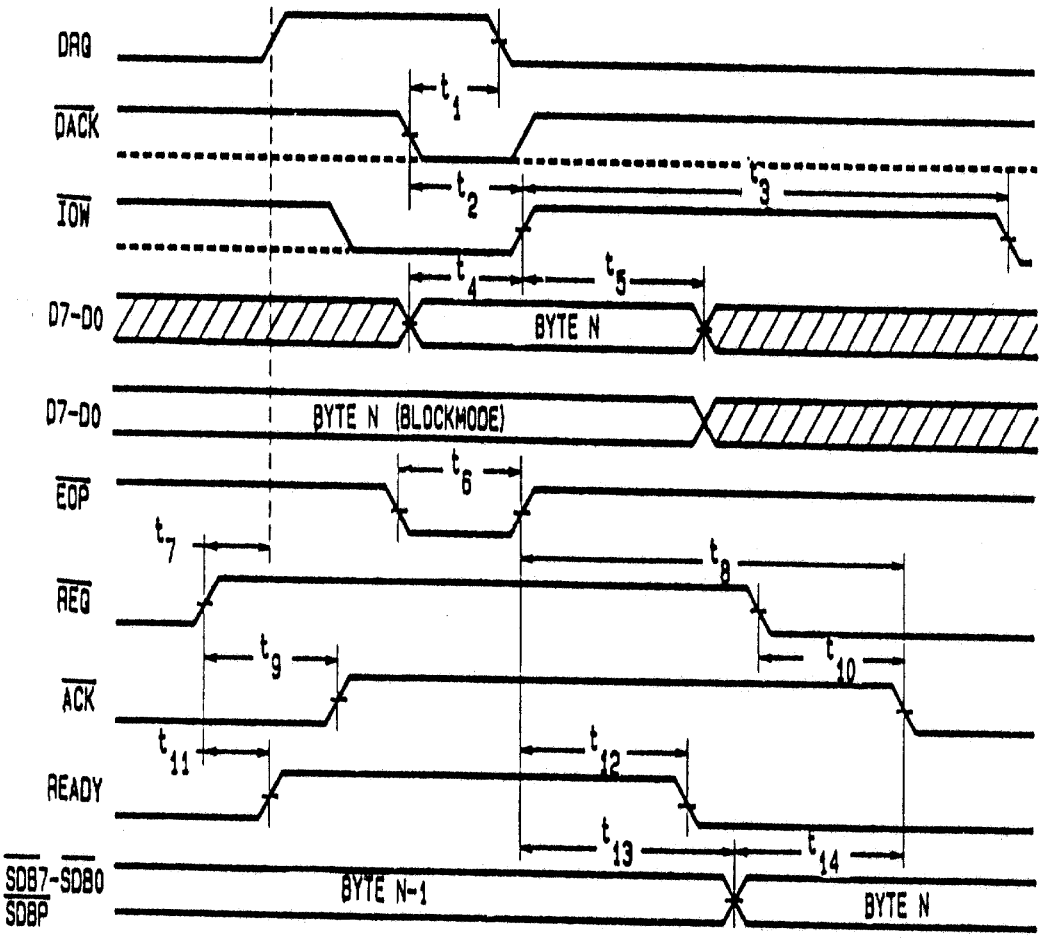


FIGURE 3. Timing waveforms - Continued.

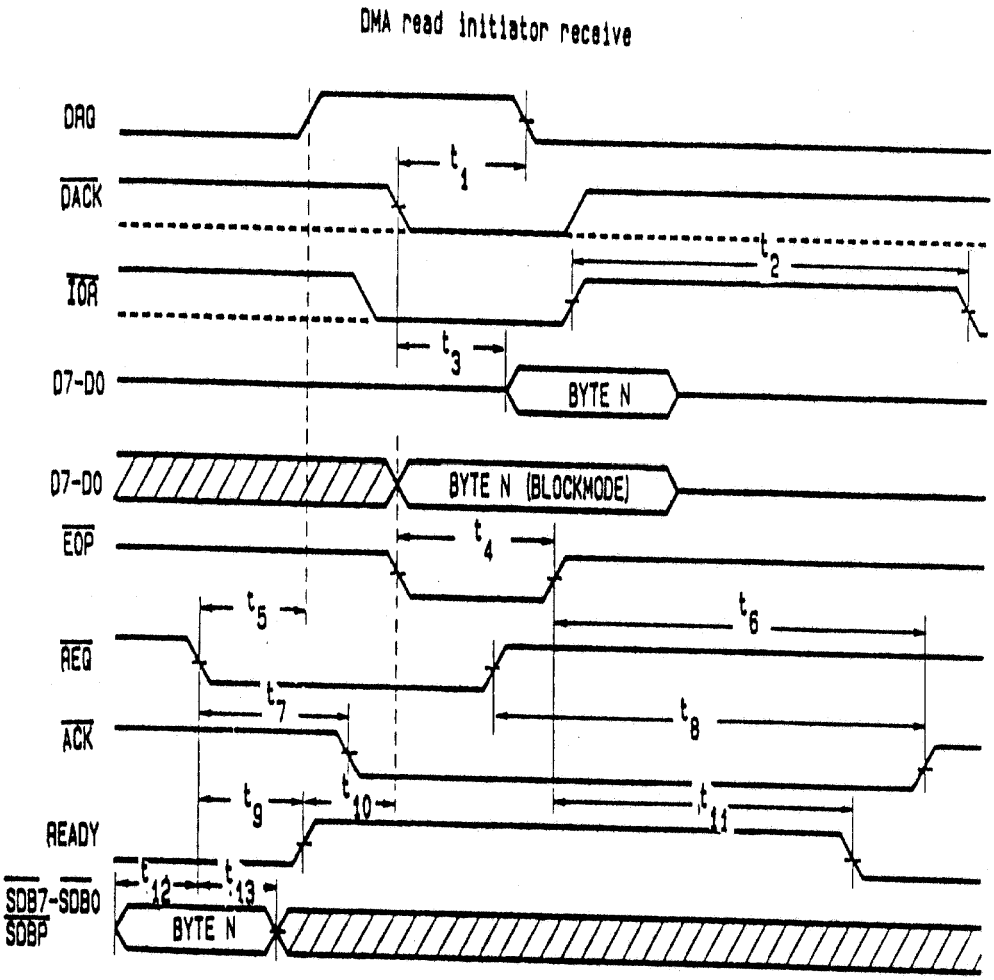


FIGURE 3. Timing waveforms - Continued.

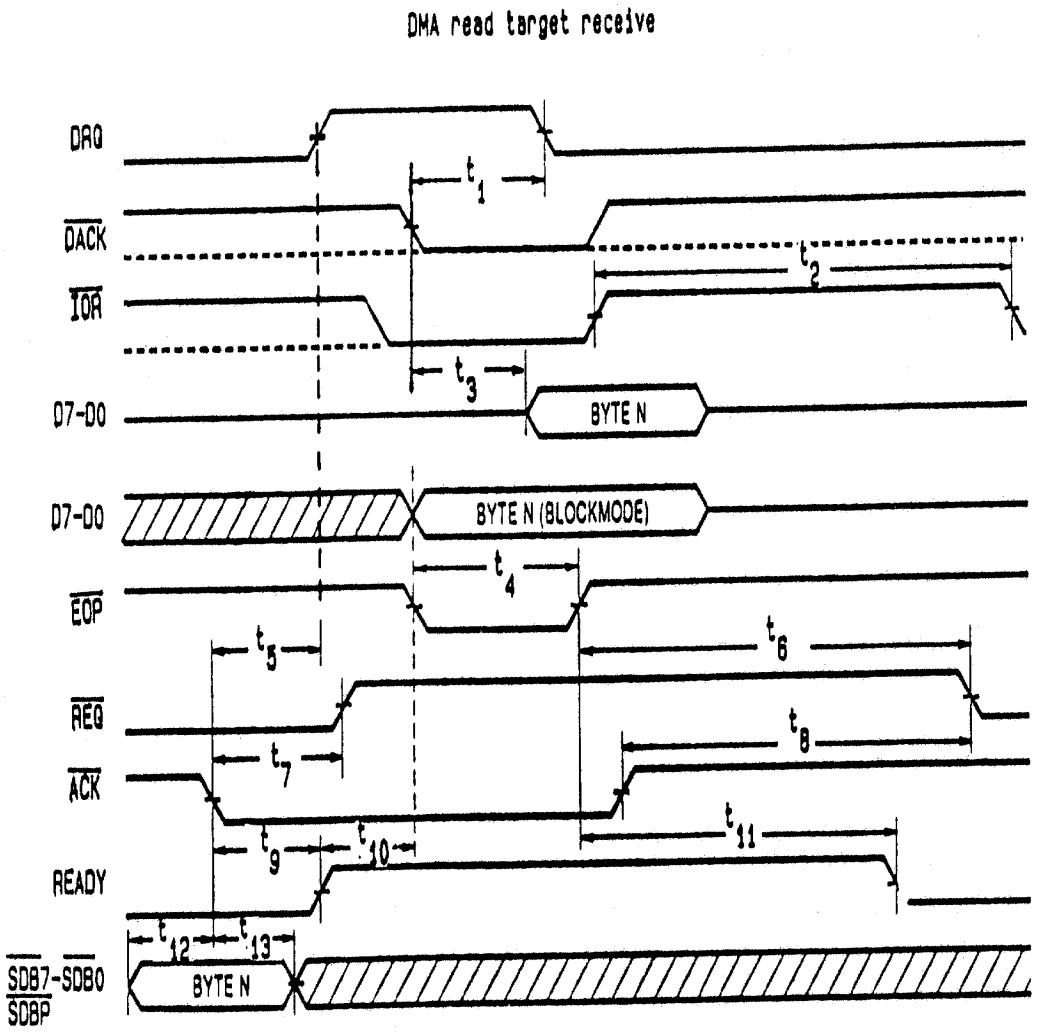


FIGURE 3. Timing waveforms - Continued.

DMA write target send

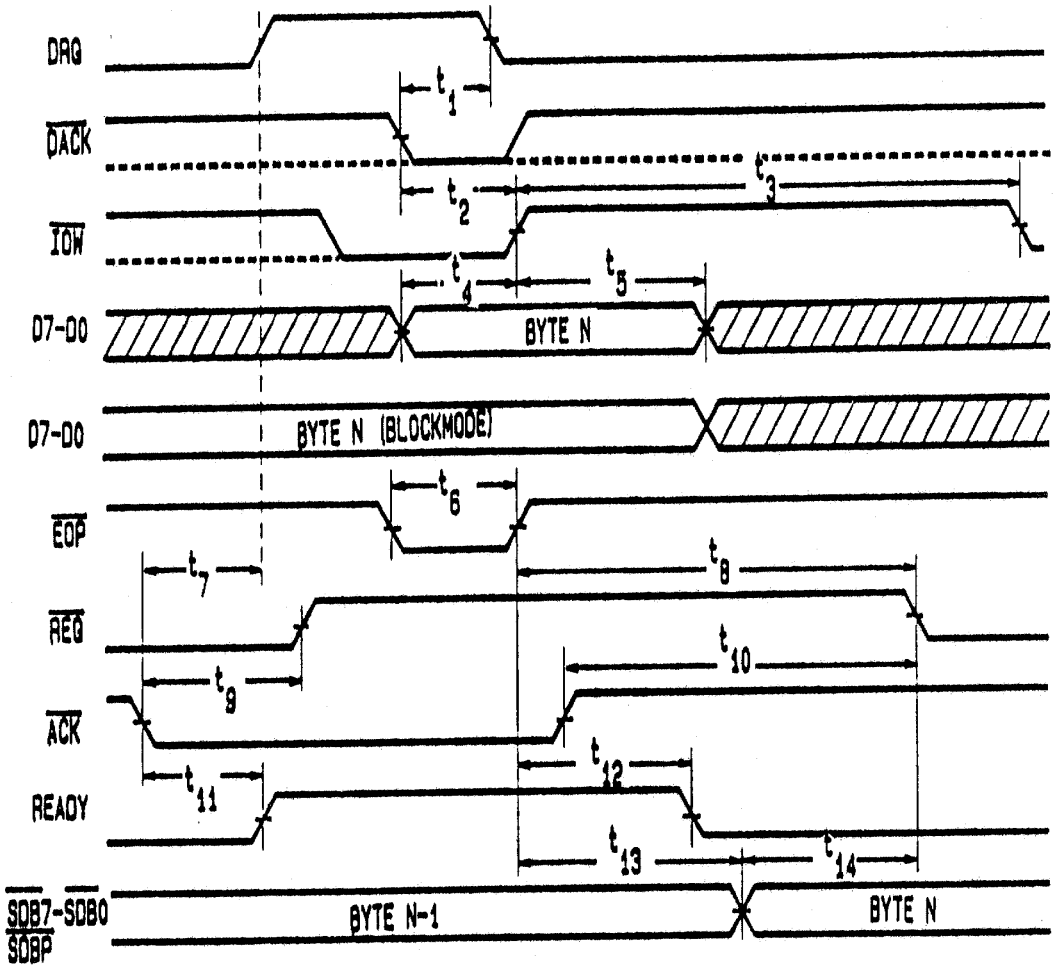


FIGURE 3. Timing waveforms - Continued.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 105 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A. For device class M, the test circuit shall be submitted to DESC-ECC for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be submitted to DESC-ECC with the certificate of compliance and shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535 and as detailed in table IIB herein.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes B and S, subgroups 7 and 8 tests shall be sufficient to verify the funcitionality of the device as approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_{IN} and C_O Measurements) shall be measured only for the initial test and after processor design changes which may affect the capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (per method 5005,table I)			Subgroups (per MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,7,9	1,7,9	1,7,9	1,7,9	1,7,9
Final electrical parameters (see 4.2)	1/ 1-3, 7-11	1/ 1-3, 7-11	2/ 1-3, 7-11	1/ 1-3, 7-11	2/ 1-3,7-11
Group A test requirements (see 4.4)	1-4, 7-11	1-4, 7-11	1-4, 7-11	1-4, 7-11	1-4, 7-11
Group B end-point electrical parameters (see 4.4)			1,7,9		
Group C end-point electrical parameters (see 4.4)	1,7,9	1,7,9		1,7,9	1,7,9
Group D end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9	1,7,9	1,7,9
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9	1,7,9	1,7,9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3.1 Additional criteria for device classes M, B, and S. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A. For device class M, the test circuit shall be submitted to DESC-ECC for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The steady-state life test circuit shall be submitted to DESC-ECC with the certificate of compliance and shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIB. Additional screening for device class V.

Test	MIL-STD-883, test method	Lot requirement
Particle impact noise detection	2020	100%
Internal visual	2010, condition A or approved alternate	100%
Nondestructive bond pull	2023 or approved alternate	100%
Reverse bias burn-in	1015	100%
Burn-in	1015, total of 240 hours at +125°C	100%
Radiographic	2012	100%

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

a. RHA tests for device classes B and S for levels M, D, R, and H or for device class M for levels M and D shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table IIA herein.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table IIA herein.

d. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at T_C = +25°C ±5 percent, after exposure.

e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.

f. For device classes M, B, and S, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-6022.

6.4 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8526.

6.5 Symbols, definitions, and functional descriptions.

A. SCSI Bus

SDB7–0 — SCSI DATA BUS 7–0:
Bidirectional/Active low. The 8-bit SCSI data bus is defined by these pins. SDB7 is the most significant bit. During arbitration phase, these lines contain the SCSI ID numbers of all initiators arbitrating for the SCSI bus; SDB7 represents the initiator with the highest priority. During the selection/reselection phase, these lines contain the ID number of the device that won the arbitration along with the ID number of the device to be selected/reselected.

SDBP — SCSI DATA BUS PARITY:
Bidirectional/Active low. SDBP is the parity bit of the SCSI data bus. Odd parity is used, meaning that the total number of ones on the bus, including the parity bit, is odd. Parity is always generated when sending information, however checking for parity errors when receiving information is a user option. Parity is not valid during arbitration phase.

SEL — SELECT:
Bidirectional/Active low. SEL is asserted by the initiator to select a target. It is also asserted by the target when reselecting it as an initiator.

BSY — BUSY:
Bidirectional/Active low. BSY is asserted to indicate that the SCSI bus is active.

ACK — ACKNOWLEDGE:
Bidirectional/Active low. ACK is asserted by the initiator, during any information transfer phase, in response to assertion of REQ by the target. Similarly, ACK is deasserted after REQ becomes inactive. These two signals form the data transfer handshake between the initiator and target. Data is latched by the target on the lowgoing edge of ACK for target receive operations.

ATN — ATTENTION:
Bidirectional/Active low. ATN is asserted by the initiator after successful selection of a target, to indicate an intention to send a message to the target. The target responds to ATN by entering the MESSAGE OUT phase.

RST — SCSI BUS RESET:
Bidirectional/Active low. RST when active indicates a SCSI bus reset condition.

I/O — INPUT/OUTPUT:
Bidirectional/Active low. I/O is controlled by the target and specifies the direction of information transfer. When I/O is asserted, the direction of transfer is to the initiator. I/O is also asserted by the target during RESELECTION phase to distinguish it from SELECTION phase.

C/D — CONTROL/DATA:
Bidirectional/Active low. C/D is controlled by the target and when asserted, indicates CONTROL (command or status) information is on the SCSI data bus. DATA is specified when C/D is deasserted.

MSG — MESSAGE:
Bidirectional/Active low. MSG is controlled by the target, and when asserted indicates MESSAGE phase.

REQ — REQUEST:
Bidirectional/Active low. REQ is asserted by the target to begin the handshake associated with transfer of a byte over the SCSI data bus. REQ is deasserted upon receipt of ACK from the initiator. Data is latched by the initiator on the lowgoing edge of REQ for initiator receive operations.

B. Microprocessor Bus

CS — CHIP SELECT:
Input/Active low. This signal enables reading or writing of the internal registers by the microprocessor, using memory mapped I/O. An alternate method for reading selected registers is available for DMA.

DRQ — DMA REQUEST:
Output/Active high. This signal is used to indicate that the L5380/L53C80 is ready to execute the next cycle of a DMA transfer on the microprocessor bus. For send operations, it indicates that the output data register is ready to receive the next byte from the DMA controller or CPU. For receive operations, it indicates that the input data register contains the next byte to be read by the DMA controller or CPU.

IRQ — INTERRUPT REQUEST: Output/Active high. The device asserts this signal to indicate to the microprocessor that one of the several interrupt conditions have been met. These include SCSI bus fault conditions as well as other events requiring microprocessor intervention. Most interrupt types are individually maskable.

IOR — I/O READ:
Input/Active low. IOR is used in conjunction with CS and A2–0 to execute a memory mapped read of a device internal register. It is also used in conjunction with DACK to execute a DMA read of the SCSI input data register.

READY — READY:
Output/Active high. Ready is used rather than DRQ as an alternate method for controlling DMA data transfer. This DMA type is termed blockmode DMA, and must be specifically enabled by the CPU. In blockmode DMA, data is throttled by treating the device as wait state memory. I/O (DMA) cycles are initiated at the maximum rate sustainable by the DMA controller/memory subsystem, but all cycles are extended (wait-states inserted) until READY is asserted by the device. This is generally the fastest DMA method since memory subsystem addressing can be overlapped with SCSI operations (flyby mode).

DACK — DMA ACKNOWLEDGE:
Input/Active low. DACK is used in conjunction with IOR or IOW to enable reading or writing the SCSI Input and Output Data Registers when in DMA mode. DACK resets DRQ and must not occur simultaneously with CS.

EOP — END OF PROCESS:
Input/Active low. This input is used to indicate to the device that a DMA transfer is to be concluded. The device can automatically generate an interrupt in response to receiving EOP from the DMA controller.

RESET — CPU BUS RESET:
Input/Active low. This input clears all internal registers and state machines. It does not result in assertion of the RST signal on the SCSI bus and therefore affects only the local device and not other devices on the bus.

IOW — I/O WRITE:
Input/Active low. IOW is used in conjunction with CS and A2–0 to execute a memory mapped write of a device internal register. It is also used in conjunction with DACK to execute a DMA write of the SCSI output data register.

A2, A1, A0 — ADDRESS 2,1,0:
Inputs/Active high. These signals, in conjunction with CS, IOR, and IOW, address the device internal registers for CPU read/write operations.

D7–0 — DATA 7–0:
Bidirectional/Active high. These signals are the microprocessor data bus. D7 is the most significant bit.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY (Part 1 or 2)	QPL-38510	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-ECC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 92-06-25

Approved sources of supply for SMD 5962-90548 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-ECC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-9054801MQX	65896	L5380DMB2
5962-9054801MXX	65896	L5380KMB2
5962-9054802MYX	65896	L53C80DMB2
5962-9054802MXX	65896	L53C80KMB2

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65896	Logic Devices Inc. 628 E. Evelyn Ave. Sunnyvale CA, 94086