REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	To update Skew between outputs (t_{SKEW}) and differential skew between outputs (t_{OST}) and footnotes 15 and 16 to table IA. Update radiation features in section 1.5 and table IB. Add equivalent test circuit and footnote 3 in figure 6. Delete class M requirements. - MAA	12-10-23	Thomas Hess

REV																				
SHEET																				
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A						
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28						

REV STATUS OF SHEETS																
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14		

PMIC N/A

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DRAWING APPROVAL DATE
07-03-23

REVISION LEVEL
A

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, RADIATION HARDENED, ADVANCED CMOS, SCHMITT 16-BIT BIDIRECTIONAL MULTI-PURPOSE REGISTERED TRANSCEIVER WITH THREE-STATE OUTPUTS, MONOLITHIC SILICON

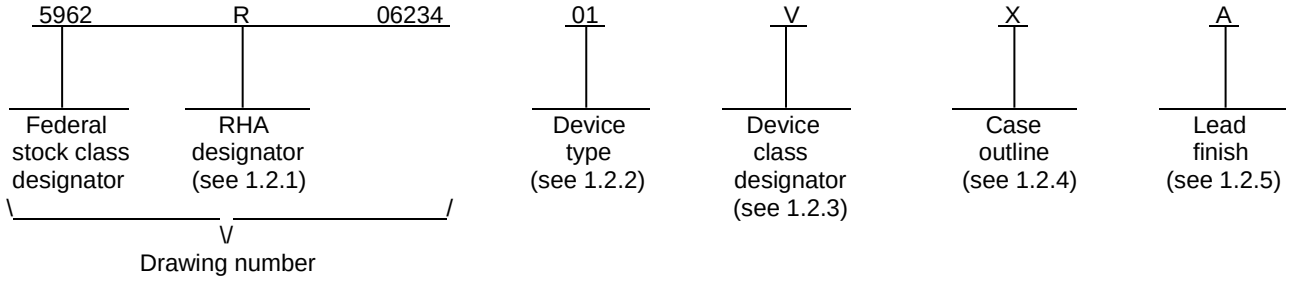
SIZE	CAGE CODE	
A	**67268**	**5962-06234**

SHEET 1 OF 28

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ACS164646S	Radiation hardened, Schmitt 16-bit bidirectional multi-purpose registered transceiver with three-state outputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	56	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{DDA}) ..... -0.3 V dc to +6.0 V dc
Supply voltage range (V_{DDB}) ..... -0.3 V dc to +6.0 V dc
DC input/output voltage range, port A ($V_{I/OA}$) ..... -0.3 V dc to V_{DDA} + 0.3 V dc 4/
DC input/output voltage range, port B ($V_{I/OB}$) ..... -0.3 V dc to V_{DDB} + 0.3 V dc 4/
DC input current, any one input (I_{IN})..... ±10 mA
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Lead temperature (soldering, 10 seconds) ..... +300°C
Thermal resistance, junction-to-case (θ_{JC})..... 20°C/W
Junction temperature (T_J) ..... +175°C
Maximum power dissipation (P_D) ..... 250 mW

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{DDA}) ..... +3.0 V dc to +3.6 V dc
or +4.5 V dc to +5.5 V dc 5/
Supply voltage range (V_{DDB}) ..... +3.0 V dc to +3.6 V dc
or +4.5 V dc to +5.5 V dc 5/
Input voltage range, port A (V_{INA})..... 0.0 V dc to V_{DDA}
Input voltage range, port B (V_{INB})..... 0.0 V dc to V_{DDB}
Case operating temperature range (T_C)..... -55°C to +125°C

1.5 Radiation features.

Maximum total dose available (Dose rate = 50 - 300 rads (Si)/s) ..... 100 Krad(Si)
Single event phenomenon (SEP):
No SEL occurs at effective LET (see 4.4.4.3)..... ≤ 110 MeV/(mg/cm^2) 6/
No SEU occurs at effective LET (see 4.4.4.3) .....≤ 75 MeV/(mg/cm^2) 6/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise specified, all voltages are referenced to V_{SS}.
3/ The limits for the parameters specified herein shall apply over the full specified V_{DD} range and case temperature range of -55°C to +125°C unless otherwise specified.
4/ For cold spare mode (V_{DDx} = V_{SS} ±0.3 V), $V_{I/Ox}$ may be -0.3 V to the maximum recommended operating V_{DDx} + 0.3 V.
5/ During normal operation, $V_{DDB} \geq V_{DDA}$.
6/ Limits are guaranteed by design or process but not production tested unless specified by the customer through the purchase order or contract.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation or contract.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications are available online at http://www.astm.org or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, west Conshohocken, PA 19428-2959)

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD20 Standard for Description of 54/74ACXXXX and 54/74ACTXXXX Advanced High-Speed CMOS devices.

JESD78 IC Latch-Up Test.

(Copies of these documents are available online at http://www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 and figure 1 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Power table. The power table shall be as specified on figure 4.

3.2.5 Logic diagram. The logic diagram shall be as specified on figure 5.

3.2.6 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 6.

3.2.7 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post irradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Test conditions 1/ 2/ $-55°C \le T_C \le +125°C$ for device 01 $+3.0\ V \le V_{DDx} \le +3.6\ V$ or $+4.5\ V \le V_{DDx} \le +5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits 3/		Unit
					Min	Max	
Schmitt trigger, positive going threshold	V_{T+}	V_{DDx} = 3.0 V and 5.5 V	All	1, 2, 3		$0.7V_{DDx}$	V
		M, D, P, L, R 4/		1		$0.7V_{DDx}$	
Schmitt trigger, negative going threshold	V_{T-}	V_{DDx} = 3.0 V and 5.5 V	All	1, 2, 3	$0.3V_{DDx}$		V
		M, D, P, L, R 4/		1	$0.3V_{DDx}$		
Schmitt trigger, range of hysteresis	V_{H1}	V_{DDx} = 4.5 V and 5.5 V	All	1, 2, 3	0.7		V
		M, D, P, L, R 4/		1	0.7		
	V_{H2}	V_{DDx} = 3.0 V and 3.6 V		1, 2, 3	0.5		
		M, D, P, L, R 4/		1	0.5		
Low level output voltage	V_{OL1}	V_{DDx} = 4.5 V, I_{OL} = 8 mA	All	1, 2, 3		0.4	V
		M, D, P, L, R 4/		1		0.4	
		V_{DDx} = 4.5 V, I_{OL} = 100 µA		1, 2, 3		0.2	
		M, D, P, L, R 4/		1		0.2	
	V_{OL2}	V_{DDx} = 4.5 V, I_{OL} = 12 mA		1, 3		0.4	
				2		0.55	
		M, D, P, L, R 4/		1		0.4	
	V_{OL3}	V_{DDx} = 3.0 V, I_{OL} = 8 mA		1, 2, 3		0.5	
		M, D, P, L, R 4/		1		0.5	
		V_{DDx} = 3.0 V, I_{OL} = 100 µA		1, 2, 3		0.2	
		M, D, P, L, R 4/		1		0.2	
	V_{OL4}	V_{DDx} = 3.0 V, I_{OL} = 12 mA		1, 3		0.5	
				2		0.6	
		M, D, P, L, R 4/		1		0.5	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ $-55°C \le T_C \le +125°C$ for device 01 $+3.0\ V \le V_{DDx} \le +3.6\ V$ or $+4.5\ V \le V_{DDx} \le +5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits 3/		Unit
					Min	Max	
High level output voltage	V_{OH1}	V_{DDx} = 4.5 V, I_{OH} = -8 mA	All	1, 2, 3	V_{DDx} - 0.5		V
		M, D, P, L, R 4/		1	V_{DDx} - 0.5		
		V_{DDx} = 4.5 V, I_{OH} = -100 µA		1, 2, 3	V_{DDx} - 0.2		
		M, D, P, L, R 4/		1	V_{DDx} - 0.2		
	V_{OH2}	V_{DDx} = 4.5 V, I_{OH} = -12 mA		1, 3	V_{DDx} - 0.6		
				2	V_{DDx} - 0.7		
		M, D, P, L, R 4/		1	V_{DDx} - 0.6		
	V_{OH3}	V_{DDx} = 3.0 V, I_{OH} = -8 mA		1, 2, 3	V_{DDx} - 0.6		
		M, D, P, L, R 4/		1	V_{DDx} - 0.6		
		V_{DDx} = 3.0 V, I_{OH} = -100 µA		1, 2, 3	V_{DDx} - 0.2		
		M, D, P, L, R 4/		1	V_{DDx} - 0.2		
	V_{OH4}	V_{DDx} = 3.0 V, I_{OH} = -12 mA		1, 3	V_{DDx} - 0.8		
				2	V_{DDx} - 0.95		
		M, D, P, L, R 4/		1	V_{DDx} - 0.8		
Input leakage current	I_{IN}	V_{DDx} = 3.6 V and 5.5 V $V_{IN} = V_{DDx}$ or V_{SS}	All	1, 2, 3	-1.0	1.0	µA
		M, D, P, L, R 4/		1	-1.0	1.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ $-55°C \le T_C \le +125°C$ for device 01 $+3.0\ V \le V_{DDx} \le +3.6\ V$ or $+4.5\ V \le V_{DDx} \le +5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits 3/		Unit
					Min	Max	
Three-state output leakage current	I_{OZ}	V_{DDx} = 3.6 V and 5.5 V $V_{IN} = V_{DDx}$ or V_{SS}	All	1, 2, 3	-1.0	1.0	µA
		M, D, P, L, R 4/		1	-1.0	1.0	
Cold sparing input leakage current (any pin) 5/	I_{CS}	$V_{DDA} = V_{DDB} = V_{SS}$ V_{IN} = 5.5 V	All	1, 2, 3	-5.0	7.0	µA
		M, D, P, L, R 4/		1	-5.0	7.0	
Warm sparing input leakage current (any pin) 5/	I_{WSA}	V_{DDB} = 3.0 V and 5.5 V $V_{DDA} = V_{SS}$ V_{IN} = 5.5 V	All	1, 2, 3	-3.0	3.0	µA
		M, D, P, L, R 4/		1	-3.0	3.0	
	I_{WSB}	V_{DDA} = 3.0 V and 5.5 V $V_{DDB} = V_{SS}$ V_{IN} = 5.5 V	All	1, 2, 3	-3.0	3.0	µA
		M, D, P, L, R 4/		1	-3.0	3.0	
Short-circuit output current 6/ 7/	I_{OS1}	V_{DDx} = 4.5 V and 5.5 V $V_O = V_{DDx}$ or V_{SS}	All	1, 2, 3	-200	200	mA
		M, D, P, L, R 4/		1	-200	200	
	I_{OS2}	V_{DDx} = 3.0 V and 3.6 V $V_O = V_{DDx}$ or V_{SS}		1, 2, 3	-100	100	
		M, D, P, L, R 4/		1	-100	100	
Standby supply current, V_{DDA} or V_{DDB}	I_{DDQ}	$V_{DDA} = V_{DDB}$ = 5.5 V $V_{IN} = V_{DDx}$ or V_{SS}	All	1		10	µA
		$\overline{xOE} = V_{DDA}$		2, 3		100	
		M, D, P, L, R 4/		1		100	
Power dissipation per switching output 8/ 9/	P_{total1}	$V_{DDA} = V_{DDB}$ = 4.5 V and 5.5 V C_L = 20 pF	All	4, 5, 6		2.0	mW/ MHz
		M, D, P, L, R 4/		4		2.0	
	P_{total2}	$V_{DDA} = V_{DDB}$ = 3.0 V and 3.6 V C_L = 20 pF		4, 5, 6		1.5	
		M, D, P, L, R 4/		4		1.5	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Test conditions 1/ 2/ $-55°C \le T_C \le +125°C$ for device 01 $+3.0\ V \le V_{DDx} \le +3.6\ V$ or $+4.5\ V \le V_{DDx} \le +5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits 3/		Unit
					Min	Max	
Input capacitance	C_{IN}	V_{DDx} = 3.0 V and 5.5 V f = 1 MHz See 4.4.1c	All	4		15	pF
Output capacitance	C_{OUT}	V_{DDx} = 3.0 V and 5.5 V f = 1 MHz See 4.4.1c	All	4		15	pF
Functional test 10/		$V_{IH} = 0.7V_{DDx}$, $V_{IL} = 0.3V_{DDx}$ See 4.4.1b	All	7, 8	L	H	
		M, D, P, L, R 4/		7	L	H	
xCLKAB or xCLKBA frequency 11/	f_{CLOCK}	V_{DDA} = 3.0 V, V_{DDB} = 4.5 V C_L = 40 pF, See figure 6	All	9, 10, 11	0	90	MHz
		M, D, P, L, R 4/		9	0	90	
Clock period	t_p	V_{DDA} = 3.0 V, V_{DDB} = 4.5 V C_L = 40 pF, See figure 6	All	9, 10, 11	11.1		ns
		M, D, P, L, R 4/		9	11.1		
Setup time, xAn high before xCLKAB↑ or xBn high before xCLKBA↑	t_{s1}	V_{DDA} = 3.0 V, V_{DDB} = 4.5 V C_L = 40 pF, See figure 6	All	9, 10, 11	3.0		ns
		M, D, P, L, R 4/		9	3.0		
Setup time, xAn low before xCLKAB↑ or xBn low before xCLKBA↑	t_{s2}	V_{DDA} = 3.0 V, V_{DDB} = 4.5 V C_L = 40 pF, See figure 6	All	9, 10, 11	2.0		ns
		M, D, P, L, R 4/		9	2.0		
Hold time, xAn high or low after xCLKAB↑ or xBn high or low after xCLKBA↑	t_h	V_{DDA} = 3.0 V, V_{DDB} = 4.5 V C_L = 40 pF, See figure 6	All	9, 10, 11	1.5		ns
		M, D, P, L, R 4/		9	1.5		
xCLKAB or xCLKBA pulse duration, high or low	t_w	V_{DDA} = 3.0 V, V_{DDB} = 4.5 V C_L = 40 pF, See figure 6	All	9, 10, 11	5.0		ns
		M, D, P, L, R 4/		9	5.0		
Input rise or fall time 8/	t_r, t_f	$V_{DDA} = V_{DDB}$ = 3.0 V and 5.5 V C_L = 40 pF, See figure 6	All	9, 10, 11		100.0	ms
		M, D, P, L, R 4/		9		100.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ $-55°C \le T_C \le +125°C$ for device 01 $+3.0\ V \le V_{DDx} \le +3.6\ V$ or $+4.5\ V \le V_{DDx} \le +5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits 3/		Unit
					Min	Max	
Port A = 3.3 V, Port B = 5.0 V							
Propagation delay time, xAn to xBn or xBn to xAn 12/	t_{PLH1}, t_{PHL1}	V_{DDA} = 3.0 V and 3.6 V V_{DDB} = 4.5 V and 5.5 V C_L = 40 pF, See figure 6	All	9, 10, 11	3.5	9.0	ns
		M, D, P, L, R 4/		9	3.5	9.0	
Propagation delay time, xCLKAB↑ to xBn or xCLKBA↑ to xAn 12/	t_{PLH2}, t_{PHL2}	V_{DDA} = 3.0 V and 3.6 V V_{DDB} = 4.5 V and 5.5 V C_L = 40 pF, See figure 6	All	9, 10, 11	4.5	10.5	ns
		M, D, P, L, R 4/		9	4.5	10.5	
Propagation delay time, xSAB↑ to xBn or xSBA↑ to xAn 12/ 13/	t_{PLH3}, t_{PHL3}	V_{DDA} = 3.0 V and 3.6 V V_{DDB} = 4.5 V and 5.5 V C_L = 40 pF, See figure 6	All	9, 10, 11	4.0	10.5	ns
		M, D, P, L, R 4/		9	4.0	10.5	
Propagation delay time, xSAB↓ to xBn or xSBA↓ to xAn (with xAn or xBn high) 12/ 13/	t_{PLH4}, t_{PHL4}	V_{DDA} = 3.0 V and 3.6 V V_{DDB} = 4.5 V and 5.5 V C_L = 40 pF, See figure 6	All	9, 10, 11	4.0	10.5	ns
		M, D, P, L, R 4/		9	4.0	10.5	
Propagation delay time, output enable, $\overline{xOE}$ to xAn or xBn 12/	t_{PZH1}, t_{PZL1}	V_{DDA} = 3.0 V and 3.6 V V_{DDB} = 4.5 V and 5.5 V C_L = 40 pF, See figure 6	All	9, 10, 11	4.0	10.0	ns
		M, D, P, L, R 4/		9	4.0	10.0	
Propagation delay time, output disable, $\overline{xOE}$ to xAn or xBn 12/	t_{PHZ1}, t_{PLZ1}	V_{DDA} = 3.0 V and 3.6 V V_{DDB} = 4.5 V and 5.5 V C_L = 40 pF, See figure 6	All	9, 10, 11	3.0	10.0	ns
		M, D, P, L, R 4/		9	3.0	10.0	
Propagation delay time, output enable, xDIR to xAn or xBn 14/	t_{PZH2}, t_{PZL2}	V_{DDA} = 3.0 V and 3.6 V V_{DDB} = 4.5 V and 5.5 V C_L = 40 pF, See figure 6	All	9, 10, 11	3.0	12.0	ns
		M, D, P, L, R 4/		9	3.0	12.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ $-55°C \le T_C \le +125°C$ for device 01 $+3.0\ V \le V_{DDx} \le +3.6\ V$ or $+4.5\ V \le V_{DDx} \le +5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits 3/		Unit
					Min	Max	
Port A = 3.3 V, Port B = 5.0 V - Continued							
Propagation delay time, output disable, xDIR to xAn or xBn 14/	t_{PHZ2}, t_{PLZ2}	V_{DDA} = 3.0 V and 3.6 V V_{DDB} = 4.5 V and 5.5 V C_L = 40 pF, See figure 6	All	9, 10, 11	3.0	12.0	ns
		M, D, P, L, R 4/		9	3.0	12.0	
Skew between outputs 15/	t_{SKEW}	V_{DDA} = 3.0 V and 3.6 V V_{DDB} = 4.5 V and 5.5 V C_L = 40 pF	All	9, 10, 11	0.0	800.0	ps
		M, D, P, L, R 4/		9	0.0	800.0	
Differential skew between outputs 16/	t_{OST}	V_{DDA} = 3.0 V and 3.6 V V_{DDB} = 4.5 V and 5.5 V C_L = 40 pF	All	9, 10, 11	0.0	1500.0	ps
		M, D, P, L, R 4/		9	0.0	1500.0	
Part to part skew 8/	t_{PART}	V_{DDA} = 3.0 V and 3.6 V V_{DDB} = 4.5 V and 5.5 V C_L = 40 pF	All	9, 10, 11	0.0	500.0	ps
		M, D, P, L, R 4/		9	0.0	500.0	
Port A = Port B = 5.0 V							
xCLKAB or xCLKBA frequency 11/	f_{CLOCK}	$V_{DDA} = V_{DDB}$ = 4.5 V C_L = 40 pF, See figure 6	All	9, 10, 11	0	100	MHz
		M, D, P, L, R 4/		9	0	100	
Clock period	t_p	$V_{DDA} = V_{DDB}$ = 4.5 V C_L = 40 pF, See figure 6	All	9, 10, 11	10		ns
		M, D, P, L, R 4/		9	10		
Setup time, xAn high before xCLKAB↑ or xBn high before xCLKBA↑	t_{s1}	$V_{DDA} = V_{DDB}$ = 4.5 V C_L = 40 pF, See figure 6	All	9, 10, 11	2.0		ns
		M, D, P, L, R 4/		9	2.0		
Setup time, xAn low before xCLKAB↑ or xBn low before xCLKBA↑	t_{s2}	$V_{DDA} = V_{DDB}$ = 4.5 V C_L = 40 pF, See figure 6	All	9, 10, 11	1.0		ns
		M, D, P, L, R 4/		9	1.0		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ $-55°C \le T_C \le +125°C$ for device 01 $+3.0\ V \le V_{DDx} \le +3.6\ V$ or $+4.5\ V \le V_{DDx} \le +5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits 3/		Unit
					Min	Max	
Port A = Port B = 5.0 V - Continued							
Hold time, xAn high or low after xCLKAB↑ or xBn high or low after xCLKBA↑	t_h	$V_{DDA} = V_{DDB} = 4.5\ V$ $C_L = 40\ pF$, See figure 6	All	9, 10, 11	1.5		ns
		M, D, P, L, R 4/		9	1.5		
xCLKAB or xCLKBA pulse duration, high or low	t_w	$V_{DDA} = V_{DDB} = 4.5\ V$ $C_L = 40\ pF$, See figure 6	All	9, 10, 11	3.5		ns
		M, D, P, L, R 4/		9	3.5		
Propagation delay time, xAn to xBn or xBn to xAn 12/	t_{PLH1}, t_{PHL1}	$V_{DDA} = V_{DDB} = 4.5\ V$ and $5.5\ V$ $C_L = 40\ pF$, See figure 6	All	9, 10, 11	3.5	7.5	ns
		M, D, P, L, R 4/		9	3.5	7.5	
Propagation delay time, xCLKAB↑ to xBn or xCLKBA↑ to xAn 12/	t_{PLH2}, t_{PHL2}	$V_{DDA} = V_{DDB} = 4.5\ V$ and $5.5\ V$ $C_L = 40\ pF$, See figure 6	All	9, 10, 11	4.0	9.0	ns
		M, D, P, L, R 4/		9	4.0	9.0	
Propagation delay time, xSAB↑ to xBn or xSBA↑ to xAn (with xAn or xBn high) 12/ 13/	t_{PLH3}, t_{PHL3}	$V_{DDA} = V_{DDB} = 4.5\ V$ and $5.5\ V$ $C_L = 40\ pF$, See figure 6	All	9, 10, 11	3.0	8.0	ns
		M, D, P, L, R 4/		9	3.0	8.0	
Propagation delay time, xSAB↓ to xBn or xSBA↓ to xAn (with xAn or xBn high) 12/ 13/	t_{PLH4}, t_{PHL4}	$V_{DDA} = V_{DDB} = 4.5\ V$ and $5.5\ V$ $C_L = 40\ pF$, See figure 6	All	9, 10, 11	3.0	8.0	ns
		M, D, P, L, R 4/		9	3.0	8.0	
Propagation delay time, output enable, $\overline{xOE}$ to xAn or xBn 12/	t_{PZH1}, t_{PZL1}	$V_{DDA} = V_{DDB} = 4.5\ V$ and $5.5\ V$ $C_L = 40\ pF$, See figure 6	All	9, 10, 11	3.5	9.0	ns
		M, D, P, L, R 4/		9	3.5	9.0	
Propagation delay time, output disable, $\overline{xOE}$ to xAn or xBn 12/	t_{PHZ1}, t_{PLZ1}	$V_{DDA} = V_{DDB} = 4.5\ V$ and $5.5\ V$ $C_L = 40\ pF$, See figure 6	All	9, 10, 11	3.0	8.0	ns
		M, D, P, L, R 4/		9	3.0	8.0	
Propagation delay time, output enable, xDIR to xAn or xBn 14/	t_{PZH2}, t_{PZL2}	$V_{DDA} = V_{DDB} = 4.5\ V$ and $5.5\ V$ $C_L = 40\ pF$, See figure 6	All	9, 10, 11	3.0	11.0	ns
		M, D, P, L, R 4/		9	3.0	11.0	
Propagation delay time, output disable, xDIR to xAn or xBn 14/	t_{PHZ2}, t_{PLZ2}	$V_{DDA} = V_{DDB} = 4.5\ V$ and $5.5\ V$ $C_L = 40\ pF$, See figure 6	All	9, 10, 11	3.0	11.0	ns
		M, D, P, L, R 4/		9	3.0	11.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ $-55°C \le T_C \le +125°C$ for device 01 $-40°C \le T_C \le +125°C$ for device 02 $+3.0\ V \le V_{DDx} \le +3.6\ V$ or $+4.5\ V \le V_{DDx} \le +5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits 3/		Unit
					Min	Max	
Port A = Port B = 5.0 V - Continued							
Skew between outputs 15/	t_{SKEW}	$V_{DDA} = V_{DDB} = 4.5\ V$ and $5.5\ V$ $C_L = 40\ pF$	All	9, 10, 11	0.0	600.0	ps
		M, D, P, L, R 4/		9	0.0	600.0	
Differential skew between outputs 16/	t_{OST}	$V_{DDA} = V_{DDB} = 4.5\ V$ and $5.5\ V$ $C_L = 40\ pF$	All	9, 10, 11	0.0	1500.0	ps
		M, D, P, L, R 4/		9	0.0	1500.0	
Part to part skew 8/	t_{PART}	$V_{DDA} = V_{DDB} = 4.5\ V$ and $5.5\ V$ $C_L = 40\ pF$	All	9, 10, 11	0.0	500.0	ps
		M, D, P, L, R 4/		9	0.0	500.0	
Port A = Port B = 3.3 V							
xCLKAB or xCLKBA frequency 11/	f_{CLOCK}	$V_{DDA} = V_{DDB} = 3.0\ V$ $C_L = 40\ pF$, See figure 6	All	9, 10, 11	0	80	MHz
		M, D, P, L, R 4/		9	0	80	
Clock period	t_p	$V_{DDA} = V_{DDB} = 3.0\ V$ $C_L = 40\ pF$, See figure 6	All	9, 10, 11	12.5		ns
		M, D, P, L, R 4/		9	12.5		
Setup time, xAn high before xCLKAB↑ or xBn high before xCLKBA↑	t_{s1}	$V_{DDA} = V_{DDB} = 3.0\ V$ $C_L = 40\ pF$, See figure 6	All	9, 10, 11	3.0		ns
		M, D, P, L, R 4/		9	3.0		
Setup time, xAn low before xCLKAB↑ or xBn low before xCLKBA↑	t_{s2}	$V_{DDA} = V_{DDB} = 3.0\ V$ $C_L = 40\ pF$, See figure 6	All	9, 10, 11	2.0		ns
		M, D, P, L, R 4/		9	2.0		
Hold time, xAn high or low after xCLKAB↑ or xBn high or low after xCLKBA↑	t_h	$V_{DDA} = V_{DDB} = 3.0\ V$ $C_L = 40\ pF$, See figure 6	All	9, 10, 11	1.5		ns
		M, D, P, L, R 4/		9	1.5		
xCLKAB or xCLKBA pulse duration, high or low	t_w	$V_{DDA} = V_{DDB} = 3.0\ V$ $C_L = 40\ pF$, See figure 6	All	9, 10, 11	5.0		ns
		M, D, P, L, R 4/		9	5.0		
Propagation delay time, xAn to xBn or xBn to xAn 12/	t_{PLH1}, t_{PHL1}	$V_{DDA} = V_{DDB} = 3.0\ V$ and $3.6\ V$ $C_L = 40\ pF$, See figure 6	All	9, 10, 11	4.0	10.0	ns
		M, D, P, L, R 4/		9	4.0	10.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ $-55°C \le T_C \le +125°C$ for device 01 $+3.0\ V \le V_{DDx} \le +3.6\ V$ or $+4.5\ V \le V_{DDx} \le +5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits 3/		Unit
					Min	Max	
Port A = Port B = 3.3 V - Continued							
Propagation delay time, xCLKAB↑ to xBn or xCLKBA↑ to xAn 12/	t_{PLH2}, t_{PHL2}	$V_{DDA} = V_{DDB} = 3.0\ V$ and $3.6\ V$ $C_L = 40\ pF$, See figure 6	All	9, 10, 11	4.5	12.5	ns
		M, D, P, L, R 4/		9	4.5	12.5	
Propagation delay time, xSAB↑ to xBn or xSBA↑ to xAn (with xAn or xBn high) 12/ 13/	t_{PLH3}, t_{PHL3}	$V_{DDA} = V_{DDB} = 3.0\ V$ and $3.6\ V$ $C_L = 40\ pF$, See figure 6	All	9, 10, 11	4.5	11.0	ns
		M, D, P, L, R 4/		9	4.5	11.0	
Propagation delay time, xSAB↓ to xBn or xSBA↓ to xAn (with xAn or xBn high) 12/ 13/	t_{PLH4}, t_{PHL4}	$V_{DDA} = V_{DDB} = 3.0\ V$ and $3.6\ V$ $C_L = 40\ pF$, See figure 6	All	9, 10, 11	4.5	11.0	ns
		M, D, P, L, R 4/		9	4.5	11.0	
Propagation delay time, output enable, $\overline{xOE}$ to xAn or xBn 12/	t_{PZH1}, t_{PZL1}	$V_{DDA} = V_{DDB} = 3.0\ V$ and $3.6\ V$ $C_L = 40\ pF$, See figure 6	All	9, 10, 11	4.0	11.0	ns
		M, D, P, L, R 4/		9	4.0	11.0	
Propagation delay time, output disable, $\overline{xOE}$ to xAn or xBn 12/	t_{PHZ1}, t_{PLZ1}	$V_{DDA} = V_{DDB} = 3.0\ V$ and $3.6\ V$ $C_L = 40\ pF$, See figure 6	All	9, 10, 11	4.0	10.0	ns
		M, D, P, L, R 4/		9	4.0	10.0	
Propagation delay time, output enable, xDIR to xAn or xBn 14/	t_{PZH2}, t_{PZL2}	$V_{DDA} = V_{DDB} = 3.0\ V$ and $3.6\ V$ $C_L = 40\ pF$, See figure 6	All	9, 10, 11	3.0	13.0	ns
		M, D, P, L, R 4/		9	3.0	13.0	
Propagation delay time, output disable, xDIR to xAn or xBn 14/	t_{PHZ2}, t_{PLZ2}	$V_{DDA} = V_{DDB} = 3.0\ V$ and $3.6\ V$ $C_L = 40\ pF$, See figure 6	All	9, 10, 11	3.0	13.0	ns
		M, D, P, L, R 4/		9	3.0	13.0	
Skew between outputs 15/	t_{SKEW}	$V_{DDA} = V_{DDB} = 3.0\ V$ and $3.6\ V$ $C_L = 40\ pF$	All	9, 10, 11	0.0	700.0	ps
		M, D, P, L, R 4/		9	0.0	700.0	
Differential skew between outputs 16/	t_{OST}	$V_{DDA} = V_{DDB} = 3.0\ V$ and $3.6\ V$ $C_L = 40\ pF$	All	9, 10, 11	0.0	1500.0	ps
		M, D, P, L, R 4/		9	0.0	1500.0	
Part to part skew 8/	t_{PART}	$V_{DDA} = V_{DDB} = 3.0\ V$ and $3.6\ V$ $C_L = 40\ pF$	All	9, 10, 11	0.0	500.0	ps
		M, D, P, L, R 4/		9	0.0	500.0	

See footnotes on next sheet.

TABLE IA. Electrical performance characteristics - Continued.

1/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table IA herein. Output terminals not designated shall be high level logic, low level logic, or open, except for all I_{DD} test, where the output terminals shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.

2/ This device requires both V_{DDA} and V_{DDB} power supplies for operation. The power supply will be indicated followed by the voltage to which the power supply is set to for the given test.

3/ For negative and positive voltage and current values, the sign designates the potential difference in reference to V_{SS} and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

4/ RHA devices supplied to this drawing have been characterized through all levels M, D, P, L, and R of irradiation. However, this device is only tested at the "R" level. Pre and post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

5/ This parameter is unaffected by the state of $\overline{xOE}$ and xDIR.

6/ Not more than one output should be shorted at a time for a maximum duration of one second.

7/ This parameter is supplied as design limit but not guaranteed or tested.

8/ This parameter is guaranteed based on characterization data but not tested.

9/ Power does not include power contribution of any CMOS output sink current.

10/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 3 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}(min) + 20\%, - 0\%$; $V_{IL} = V_{IL}(max) + 0\%, - 50\%$, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH}(min)$ and $V_{IL}(max)$.

11/ Guaranteed by functional test.

12/ For propagation delay tests, all paths must be tested.

13/ These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

14/ This parameter is guaranteed by design but not tested.

15/ For device type 01, Output skew is defined as a comparison of any two output transitions of the same type at the same temperature and voltage for the same port within the byte:1A1 through 1A8 are compared high-to-low versus high-to-low and low-to-high versus low-to-high; similarly 1B1through 1B8 are compared, 2A1 through 2A8 are compared and 2B1 through 2B8 are compared.

16/ For device type 01, differential output skew is defined as the comparison of any two outputs transitioning of opposite types at the same temperature and voltage for the same port within the byte:1A1 through 1A8 are compared high-to-low versus high-to-low; similarly 1B1through 1B8 are compared, 2A1 through 2A8 are compared and 2B1 through 2B8 are compared.

TABLE IB. SEP test limits. 1/ 2/

Device type	T_A = Temperature ±10°C	Single event upsets(SEU) Bias V_{DDx} = 3.0 V		Single event latch-up(SEL) Bias V_{DDx} = 5.5 V
		Effective LET No upsets [MeV/(mg/cm^2)]	Maximum device cross section	Effective LET No latch-up [MeV/(mg/cm^2)]
All	3/	75	2.5 x 10^{-7} cm^2	110

1/ Devices that contain cross-coupled resistance must be tested at the maximum T_A. For SEP test conditions, see 4.4.4.3 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Worst case temperature for latch-up test is T_A = +125°C. Test temperature for SEU test is TA = +25°C.

Case outline X

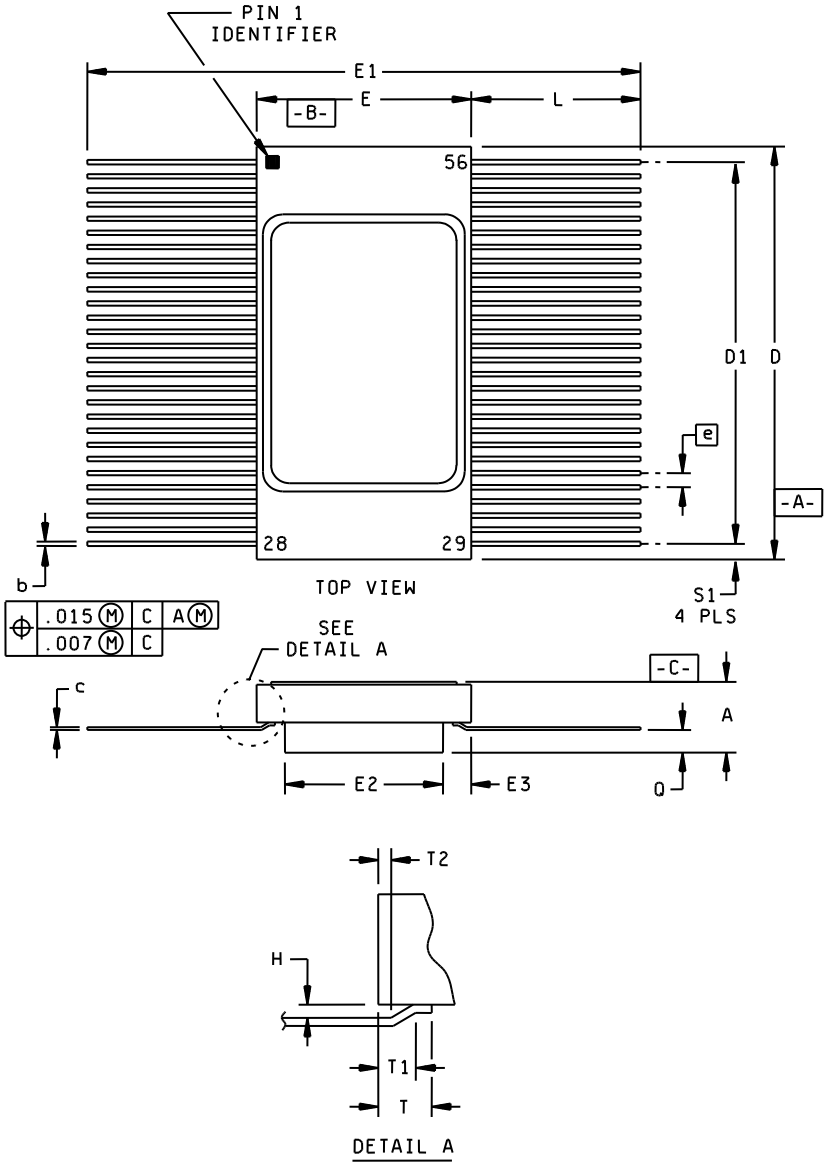


FIGURE 1. Case outline.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-06234
		REVISION LEVEL A	SHEET 17

Case outline X				
Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A		.125		3.175
b	.006	.01	0.152	0.254
c	.005 TYP		0.127 TYP	
D	.722	.738	18.339	18.745
D1	.675 TYP		17.145 TYP	
E	.374	.386	9.500	9.804
E1	1.100 TYP		27.940 TYP	
E2	.274	.286	6.960	7.264
E3	.030		0.762	
e	.025 BSC		.635 BSC	
H	.002	.014	0.051	0.356
L	.300		7.620	
Q	.040 REF		1.016 REF	
S1	.005		0.127	
T	.033 REF		0.838 REF	
T1	.018 REF		0.457 REF	
T2	.000		0.000	
N	56		56	

NOTES:
1. All exposed metallized areas are gold plated 100 micro-inches over electroplated nickel underplating 100 micro-inches thick per MIL-PRF-38535.
2. Lead finishes are in accordance with MIL-PRF-38535.
3. Seal ring is electrically connected to V_{SS}.
4. Letter designations are to cross-reference to MIL-STD-1835.
5. Lead true position tolerance and coplanarity are not measured.

FIGURE 1. Case outline - Continued.

Device type	All				
Case outline	X				
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	1DIR	20	2B5	39	V_{SS}
2	1CLKBA	21	2B6	40	2A3
3	1SBA	22	V_{DDB}	41	2A2
4	V_{SS}	23	2B7	42	2A1
5	1B1	24	2B8	43	1A8
6	1B2	25	V_{SS}	44	1A7
7	V_{DDB}	26	2SBA	45	1A6
8	1B3	27	2CLKBA	46	V_{SS}
9	1B4	28	2DIR	47	1A5
10	1B5	29	$\overline{2OE}$	48	1A4
11	V_{SS}	30	2CLKAB	49	1A3
12	1B6	31	2SAB	50	V_{DDA}
13	1B7	32	V_{SS}	51	1A2
14	1B8	33	2A8	52	1A1
15	2B1	34	2A7	53	V_{SS}
16	2B2	35	V_{DDA}	54	1SAB
17	2B3	36	2A6	55	1CLKAB
18	V_{SS}	37	2A5	56	$\overline{1OE}$
19	2B4	38	2A4		

Terminal description	
Terminal symbol	Description
$\overline{xOE}$ (x = 1, 2)	Output enable inputs (active low)
xDIR (x = 1, 2)	Direction-control inputs
xAn (x = 1, 2; n = 1 - 8)	Side A inputs or three-state outputs
xBn (x = 1, 2; n = 1 - 8)	Side B inputs or three-state outputs
xSAB (x = 1, 2)	Select real-time or stored A bus data to B bus
xSBA (x = 1, 2)	Select real-time or stored B bus data to A bus
xCLKAB (x = 1, 2)	Clock inputs, store A bus data
xCLKBA (x = 1, 2)	Clock inputs, store B bus data

FIGURE 2. Terminal connections.

Inputs						Data I/O 1/		Operation or function
$\overline{xOE}$	xDIR	xCLKAB	xCLKBA	xSAB	xSBA	xA1 - xA8	xB1 - xB8	
X	X	↑	X	X	X	Input	Unspecified	Store A, B unspecified 1/
X	X	X	↑	X	X	Unspecified	Input	Store B, A unspecified 1/
H	X	↑	↑	X	X	Input	Input	Store A and B data 1/
H	X	H or L	H or L	X	X	Input	Input	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

H = High voltage level
L = Low voltage level
X = Irrelevant
↑ = Low-to-high transition of the clock

1/ The data output functions may be enabled or disabled by various signals at the $\overline{xOE}$ or xDIR. Data-input functions are always enabled, i.e., data at the bus terminals will be stored on every low-to-high transition of the clock inputs.

FIGURE 3. Truth table.

Port B	Port A	Operation
5 Volts	3.3 Volts	Voltage translator
5 Volts	5 Volts	Non translating
3.3 Volts	3.3 Volts	Non translating
V_{SS}	V_{SS}	Cold spare
V_{SS}	3.3 Volts or 5 Volts	Port A warm spare
3.3 Volts or 5 Volts	V_{SS}	Port B warm spare

NOTES:

I/O guidelines

Control dignals xDIR, $\overline{\text{xOE}}$, xSAB, xSBA, xCLKAB, and xCLKBA ar 5-volt tolerant inputs powered by V_{DDA}. Therefore, when V_{DDA} is at 3.3 volts, either 3.3-volt or 5-volt CMOS logic levels may be applied to all control inputs. Additionally, it is recommended that all unused inputs be tied to V_{SS} through a 1 KΩ resistor. Input signal transition should be driven into the device with a rise and fall time that is ≤ 100 ms.

Power application guidelines

For proper operation, connect power to all V_{DDx} and ground all V_{SS} pins (i.e., no floating V_{DDx} or V_{SS} input pins). By virtue of the device warm-spare feature, power supplies V_{DDB} and V_{DDA} may be applied to the device in any order. To ensure the device is in cold-spare, both supplies, V_{DDB} and V_{DDA}, must be equal to V_{SS} ±0.3 V. Warm-spare operation is in effect when on power supply is > 1 V and the other power supply is equal to V_{SS} ±0.3 V. If V_{DDB} has a power-on ramp rate longer than 1 second, then V_{DDA} should power-on first to ensure proper control of xDIR and $\overline{\text{xOE}}$. During normal operation of the part, after power-up, ensure $V_{DDB} \geq V_{DDA}$.

By definition, warm sparing occurs when half of the chip receives its normal V_{DD} supply value while the V_{DD} supplying the other half of the chip is set to 0.0 V. When the chip is “warm spared”, the side that has its V_{DD} set to a normal operational value is “actively” three-stated because the chip’s internal OE signal is forced low. The side of the chip that has V_{DD} set to 0.0 V is “passively” three-stated by the cold spare circuitry.

In order to minimize transients and current consumption, the user is encouraged to first apply a high level to the xOE pins and then power down the appropriate supply.

FIGURE 4. Power table.

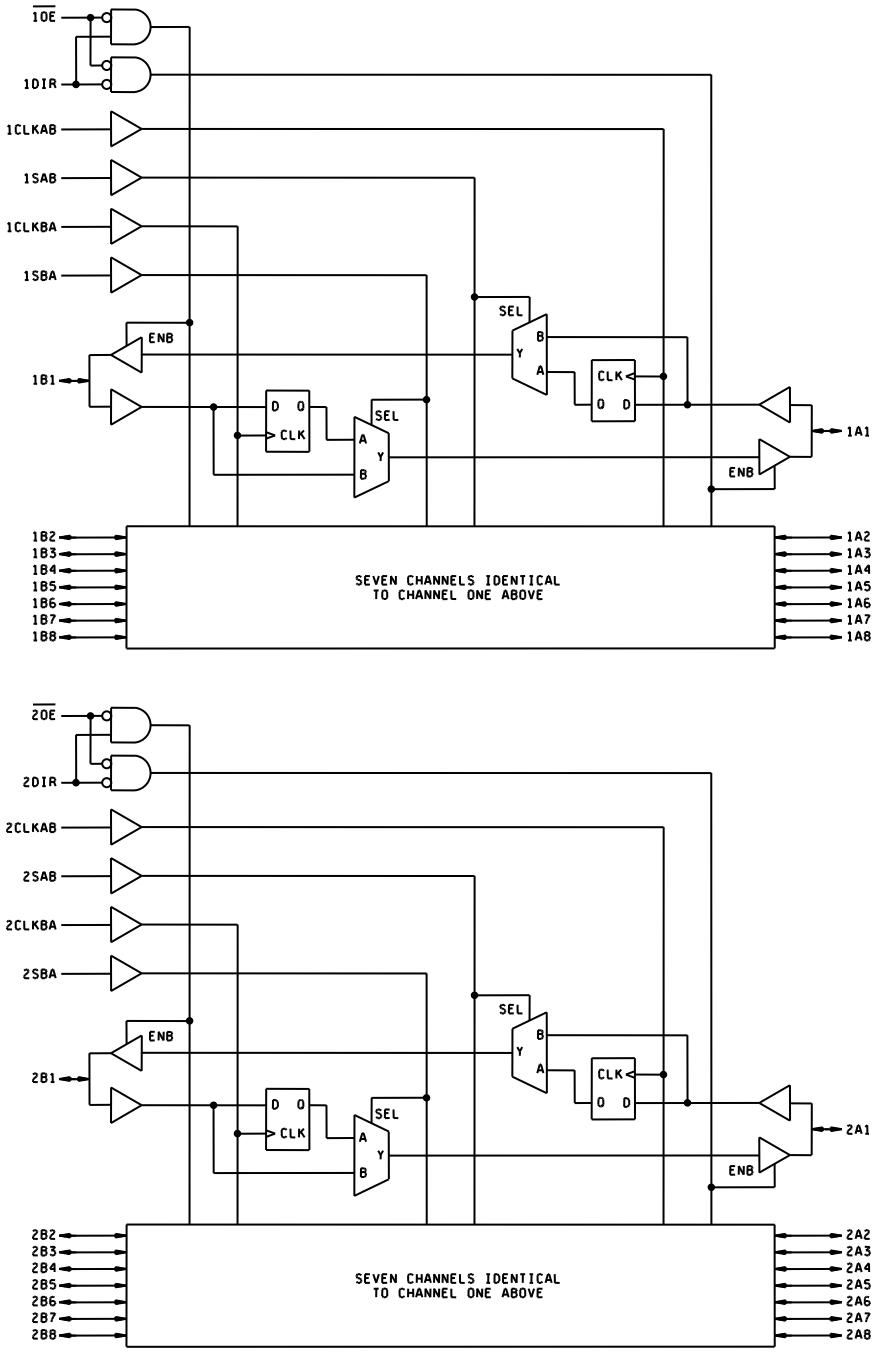


FIGURE 5. Logic diagram.

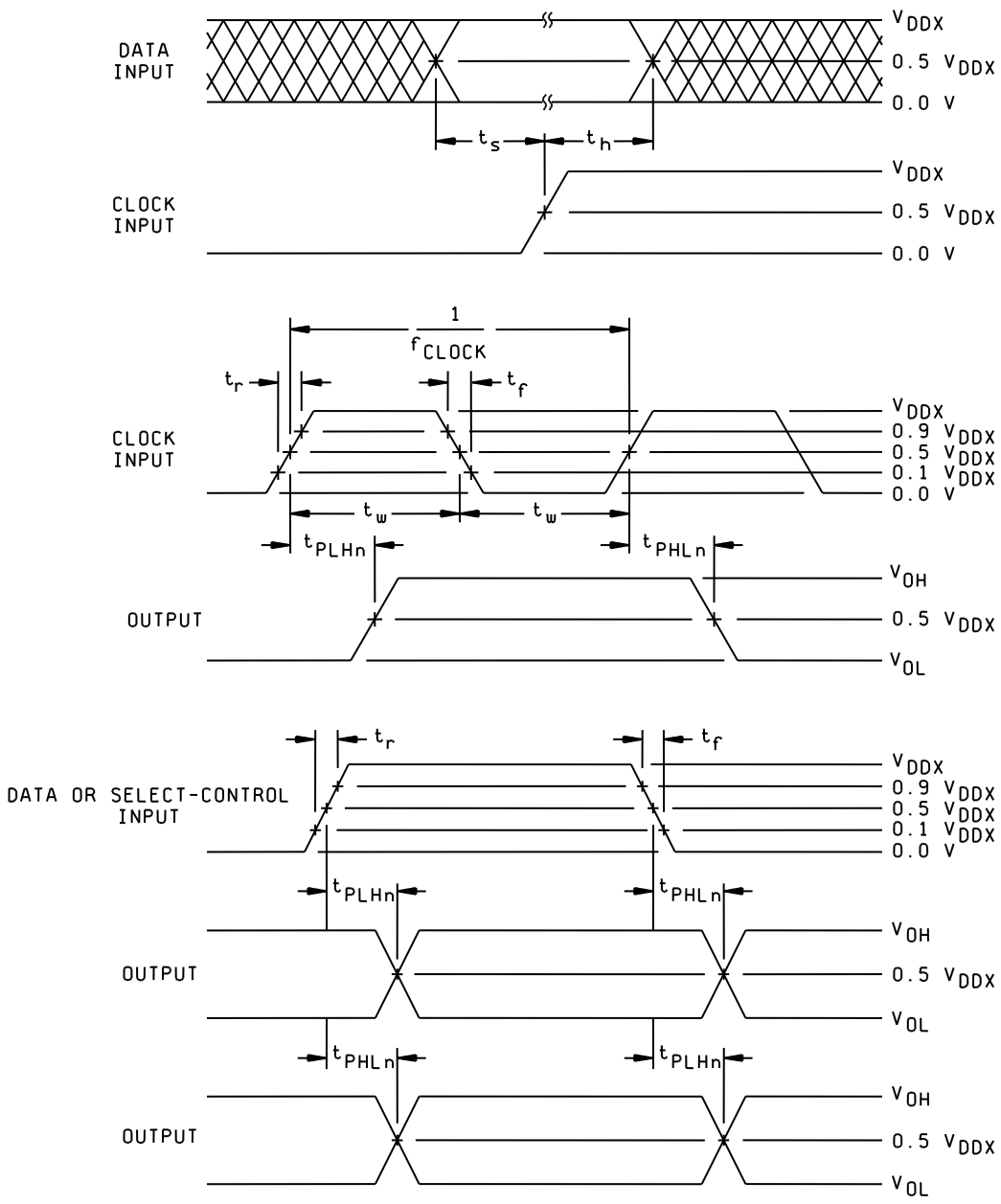
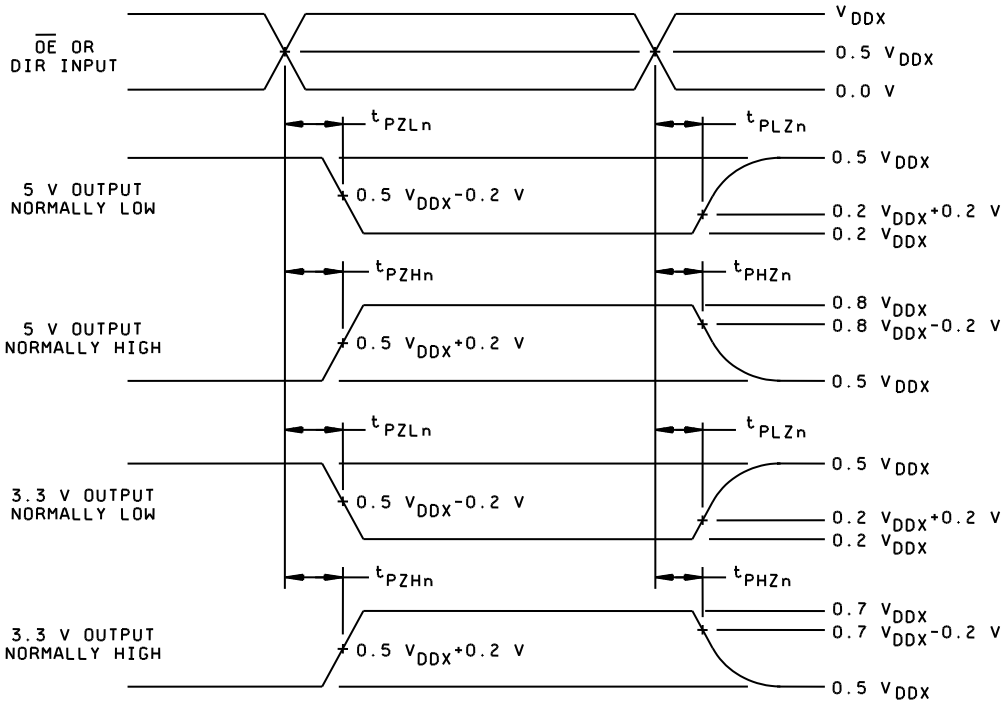
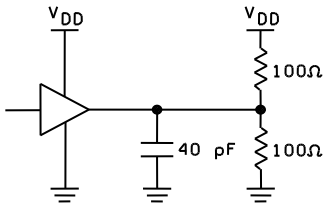


FIGURE 6. Switching waveforms and test circuit.





TEST CIRCUIT A or EQUIVALENT

NOTES:

1. C_L includes test jig and probe capacitance.
2. Input signal from pulse generator: V_{IN} = 0.0 V to V_{DDx}; f ≤ 10 MHz; t_r = 1.0 ns/V ±0.3 ns/V; t_f = 1.0 ns/V ±0.3 ns/V; t_r and t_f shall be measured from 0.1 V_{DDx} to 0.9 V_{DDx} and from 0.9 V_{DDx} to 0.1 V_{DDx}, respectively.
3. Equivalent test circuit means that DUT performance will be correlated and remain guaranteed to the applicable test circuit, above, whenever a test platform change necessitates a deviation from the applicable test circuit.

FIGURE 6. Switching waveforms and test circuit - Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B or as modified in the device manufacturer's Quality Management plan.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. C_{IN} and C_{OUT} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} and C_{OUT} shall be measured between the designated terminal and V_{SS} at a frequency of 1 MHz. For C_{IN} and C_{OUT}, test all applicable pins on five devices with zero failures.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/ 3/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11 3/
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 2, 3, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ PDA applies to subgroups 1 and 7.
2/ PDA applies to subgroups 1, 7, and deltas.
3/ Delta limits, as specified in table IIB, shall be required where specified, and the delta values shall be completed with reference to the zero hour electrical parameters.

TABLE IIB. Burn-in delta parameters (+25°C).

Parameter	Symbol	Condition	Delta limit
Standby supply current	I_{DDQ}	T_A = 25°C	±10% of measured value or 35 μA whichever is greater

NOTE: If device is tested at or below 35 μA, no deltas are required. Deltas are performed at room temperature.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019, condition A, and as specified herein.

4.4.4.1.1 Accelerated annealing tests. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limits at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. When required by the customer, dose rate induced latchup testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.3 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or $\geq 10^7$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be +25°C for the upset measurements and the maximum rated operating temperature ±10°C for the latchup measurements.

f. Bias conditions shall be defined by the manufacturer for the latchup measurements.

g. For SEP test limits, see table IB herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit V_{SS} terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.7 Additional information. A copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA Test conditions (SEP).

b. Number of upsets (SEU).

c. Occurrence of latchup (SEL).

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 12-10-23

Approved sources of supply for SMD 5962-06234 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R0623401QXA	65342	UT54ACS164646SUCA
5962R0623401QXC	65342	UT54ACS164646SUCC
5962R0623401VXA	65342	UT54ACS164646SUCA
5962R0623401VXC	65342	UT54ACS164646SUCC

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65342	Aeroflex Colorado Springs Inc. 4350 Centennial Boulevard Colorado Springs, CO 80907-3486