REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
D	Add vendor CAGE 27014. Remove vendor CAGE 07263. Device 01FX inactive for new design. Convert to military drawing format. Editorial changes throughout.	86-03-28	M. A. Frye
E	Technical changes in table I, table II, and 1.4. Change CAGE code to 67268. Delete vendor CAGE 31019. Change vendor CAGE 27014 part number from MM4640BJ/883B to CD4040BMJ/883. Editorial changes throughout.	89-02-09	M. A. Frye
F	Update boilerplate to MIL-PRF-38535 requirements. Editorial changes throughout.- LTG	03-08-19	Thomas M. Hess

CURRENT CAGE CODE 67268

REV																				
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REV STATUS				REV			F	F	F	F	F	F	F	F	F					
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9					

PMIC N/A

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DRAWING APPROVAL DATE
78-02-24

REVISION LEVEL
F

DEFENSE SUPPLY CENTER COLUMBUS

COLUMBUS, OHIO 43216
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, CMOS, 12-BIT BINARY COUNTER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**14933**	**77058**

SHEET 1 OF 9

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

77058	01	E	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	4040B	CMOS, 12-bit binary counter

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line package
F	GDFP2-F16 or CDFP3-F16	16	Flat pack

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range ..... -0.5 V dc to +18 V dc
Input voltage range ..... -0.5 V dc to V_{DD} + 0.5 V dc
Storage temperature range ..... -65°C to +150°C
Maximum power dissipation (P_D) ..... 500 mW 1/
Lead temperature (soldering, 10 seconds) ..... +300°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Junction temperature (T_J) ..... +175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) ..... +3.0 V dc to +15 V dc
Case operating temperature range (T_C) ..... -55°C to +125°C
Minimum CP width, low or high (t_W):
  T_C = +25°C ..... 335 ns
  T_C = -55°C, T_C = +125°C ..... 503 ns
Minimum reset pulse width (t_{WR}):
  T_C = +25°C ..... 640 ns
  T_C = -55°C, T_C = +125°C ..... 950 ns

1/ For T_C = +100°C to +125°C, derate linearly at 12 mW/°C to 200 mW.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Quiescent device current	I_{DD}	V_{DD} = 15 V V_{IN} = 0.0 V or V_{DD}	1	All		100	µA
			2			600	
			3			80	
Low level output voltage	V_{OL}	V_{DD} = 15 V V_{IN} = 0.0 V or V_{DD}	1, 2, 3	All		.05	V
High level output voltage	V_{OH}	V_{DD} = 15 V V_{IN} = 0.0 V or V_{DD}	1, 2, 3	All	14.95		V
Low level input voltage	V_{IL}	V_{DD} = 5.0 V V_O = 0.5 V or 4.5 V	1, 2, 3	All		1.5	V
		V_{DD} = 15.0 V V_O = 1.5 V or 13.5 V	1, 2, 3	All		4.0	V
High level input voltage	V_{IH}	V_{DD} = 5.0 V V_O = 0.5 V or 4.5 V	1, 2, 3	All	3.5		V
		V_{DD} = 15.0 V V_O = 1.5 V or 13.5 V	1, 2, 3	All	11		V
Low level output current	I_{OL}	V_{DD} = 5 V V_O = 0.4 V	1	All	.51		mA
			2	All	.36		
			3	All	.64		
		V_{DD} = 15 V V_O = 1.5 V	1	All	3.4		
			2	All	2.4		
			3	All	4.2		
High level output current	I_{OH}	V_{DD} = 5 V V_O = 4.6 V	1	All	-.20		mA
			2	All	-.14		
			3	All	-.25		
		V_{DD} = 15 V V_O = 13.5 V	1	All	-1.5		mA
			2	All	-1.1		
			3	All	-1.8		
Input current	I_{IN}	V_{DD} = 15 V V_{IN} = 0.0 V or V_{DD}	1, 3	All		±0.1	µA
			2			±1.0	
Input capacitance	C_{IN}	V_{IN} = 0.0 V T_C = +25°C See 4.3.1c	4	All		7.5	pF
Functional test		See 4.3.1d	7	All			

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Minimum clock frequency	f_{MAX}	V_{DD} = 5.0 V C_L = 50 pF ±10% R_L = 200 kΩ $t_r = t_f$ = 20 ns	T_C = +25°C	9	All	1.5		MHz
			T_C = -55°C, T_C = +125°C	10, 11		1.0		MHz
Transition time	t_{THL}, t_{TLH}		T_C = +25°C	9	All	2.0	350	ns
			T_C = -55°C, T_C = +125°C	10, 11		2.0	525	ns
Propagation delay time, RESET to Q_n	t_{PLH1}. t_{PHL1}		T_C = +25°C	9	All	2.0	1080	ns
			T_C = -55°C, T_C = +125°C	10, 11		2.0	1620	ns
Interstage propagation delay time Q_n to Q_{n+1}	t_{PLH2}. t_{PHL2}		T_C = +25°C	9	All	2.0	700	ns
			T_C = -55°C, T_C = +125°C	10, 11		2.0	1050	ns

Device type	All
Case outlines	E and F
Terminal number	Terminal symbol
1	Q_{12}
2	Q_6
3	Q_5
4	Q_7
5	Q_4
6	Q_3
7	Q_2
8	V_{SS}
9	Q_1
10	CP
11	RESET
12	Q_9
13	Q_8
14	Q_{10}
15	Q_{11}
16	V_{DD}

FIGURE 1. Terminal connections.

CP	RESET	Output state
↑	0	No change
↓	0	Advanced to next state
X	1	All outputs are low

↑ = Low to high transition
↓ = High to low transition
X = Irrelevant

FIGURE 2. Truth table.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	----
Final electrical test parameters (method 5004)	1*, 2, 3, 9
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5, 6, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. Test all applicable pins on five devices with zero failures.

d. Subgroup 7 tests shall include verification of the truth table as specified in figure 2 herein.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 03-08-19

Approved sources of supply for SMD 77058 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
7705801EA	27014	CD4040BMJ/883
7705801FA	3/	BCL4040BF

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
27014	National Semiconductor P. O. Box 58090 Santa Clara, CA 95052-8090