

82S100/82S101 Field Programmable Logic Array (16 × 48 × 8)

**Military
Customer Specific Products**

Product Specification

DESCRIPTION

The 82S100 (3-State) and 82S101 (Open-Collector) are bipolar, Fuse Programmable Logic Arrays (FPLAs). Each device utilizes the standard AND/OR invert architecture to directly implement custom sum of product logic equations.

Each device consists of 16 dedicated inputs and 8 dedicated outputs. Each output is capable of being actively controlled by any or all of the 48 product terms. The True, Complement, or Don't Care condition of each of the 16 inputs ANDed together comprise one P-term. All 48 P-terms are selectively ORed to each output. The user must then only select which P-term will activate an output by disconnecting terms which do not affect the output. In addition, each output can be fused as active-HIGH (H) or active-LOW (L).

The 82S100 and 82S101 are fully TTL compatible, and include chip enable control for expansion of input variables and output inhibit. They feature either Open-Collector or 3-State outputs for ease of expansion of product terms and application in bus-organized systems.

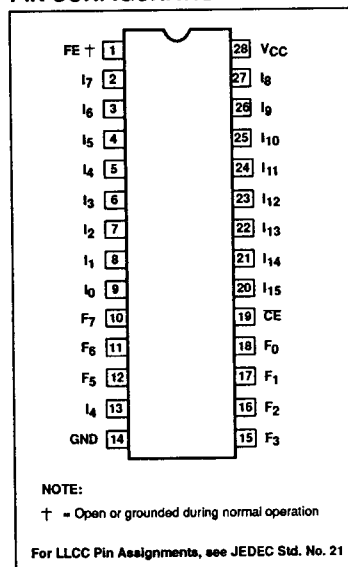
FEATURES

- Field-programmable (Ni-Cr link)
- Input variables: 16
- Output functions: 8
- Product terms: 48
- I/O propagation delay: 80ns max
- Power dissipation: 600mW typ
- Input loading: -150µA max
- Chip enable input
- Output option:
 - 82S100: 3-State
 - 82S101: Open-Collector
- Output disable function;
 - 3-State: HI-Z
 - Open-Collector: HI
- Separate I/O architecture

APPLICATION

- CRT display systems
- Code conversion
- Peripheral controllers
- Function generators
- Look-up and decision tables
- Microprogramming
- Address mapping
- Character generators
- Data security encoders
- Fault detectors
- Frequency synthesizers
- 16-bit to 8-bit bus interface
- Random logic replacement

PIN CONFIGURATION



LOGIC FUNCTION

TYPICAL PRODUCT TERM:

$$P_n = A \bullet B \bullet C \bullet D$$

TYPICAL LOGIC FUNCTION:

$$\text{AT OUTPUT POLARITY = H} \\ Z = P_0 + P_1 + P_2 \dots$$

AT OUTPUT POLARITY = L

$$Z = P_0 + P_1 + P_2 \dots \\ Z = P_0 \bullet P_1 \bullet P_2 \dots$$

NOTES:

1. For each of the 8 outputs, either function Z (active-High) or Z (active-Low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.

2. Z, A, B, C etc. are user defined connections to fixed inputs (I) and output pins (O).

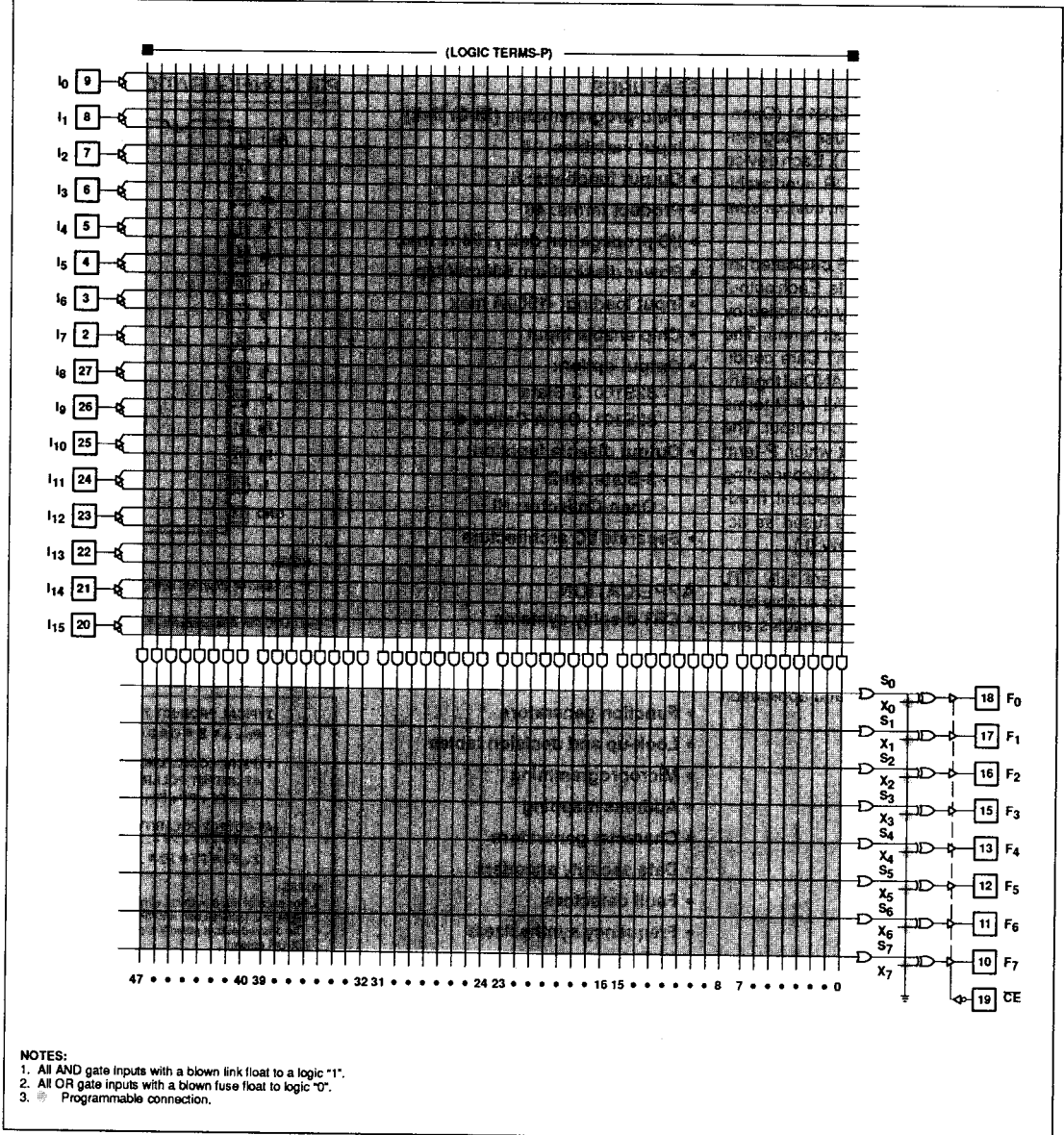
ORDERING INFORMATION

DESCRIPTION	3-STATE	OPEN-COLLECTOR
28-pin Ceramic DIP 600mil-wide	82S100/BXA	82S101/BXA
28-pin Ceramic Flat Pack	82S100/BYA	82S101/BYA
28-pin Ceramic LLCC	82S100/B3A	82S101/B3A

Field Programmable Logic Array (16 × 48 × 8)

82S100/101

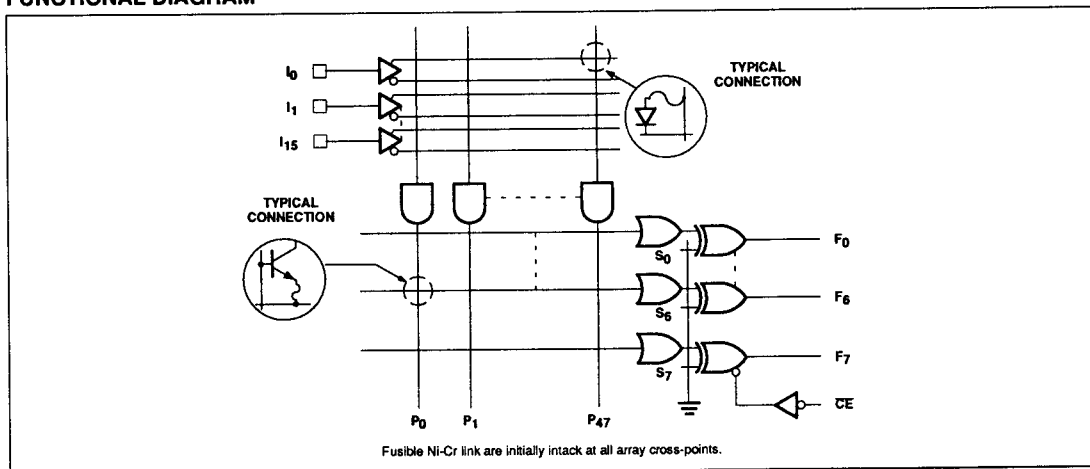
FPLA LOGIC DIAGRAM



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82S100/101

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Power supply voltage	+7	V _{DC}
V _I	Input voltage	+10.0	V _{DC}
V _O	Output voltage	+5.5	V _{DC}
I _I	Input currents	-30 to +30	mA
I _O	Output currents	+100	mA
T _A	Operating Temperature range	-55 to +125	°C
T _{STG}	Storage Temperature range	-65 to +150	°C

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82S100/101

DC ELECTRICAL CHARACTERISTICS $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$

SYMBOL	PARAMETER	TEST CONDITIONS ³	LIMITS			UNIT
			Min	Typ ⁵	Max	
Input Voltage						
V _{IH}	High	V _{CC} = 5.5V	2.0			V
V _{IL}	Low	V _{CC} = 4.5V			0.8	V
V _{IK}	Clamp ⁴	V _{CC} = 4.5V, I _I = -18mA		-0.8	-1.2	V
Output Voltage						
V _{OH}	High (82S100) ^{5, 10}	V _{CC} = 4.5V	2.4			V
V _{OL}	Low ⁶	I _{OH} = -2mA		0.35	0.5	V
		I _{OL} = 9.6mA				V
Input Current						
I _{IH}	High	V _{CC} = 5.5V		<1	50	μA
I _{IL}	Low	V _I = 5.5V		-10	-150	μA
		V _I = 0.45V				μA
Output Current						
I _{O(OFF)}	Hi-Z State	CE = HIGH, V _{CC} = Max		1	60	μA
	(82S100)	V _O = 5.5V		-1	-60	μA
I _{OS}	Short circuit (82S100) ^{4, 7, 10}	V _O = 0.45V	-15		-85	mA
I _{CC}	V _{CC} supply current ⁸	CE = LOW, V _O = 0V		120	180	mA
		V _{CC} = 5.5V				mA
Capacitance⁹						
C _{IN}	Input	CE = HIGH		8	13	pF
C _{OUT}	Output	V _{CC} = 5.0V		17	22	pF
		V _I = 2.0V				
		V _O = 2.0V				

AC ELECTRICAL CHARACTERISTICS $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ ⁵	Max	
Propagation Delay							
T _{PD}	Input ¹¹	Output	Input	35	80		ns
T _{CE}	Chip enable	Output	Chip enable	15	40		ns
Disable Time							
T _{CD}	Chip disable	Output	Chip enable	15	40		ns

NOTES:

- Stresses above those listed under Absolute Maximum Ratings may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- All voltage values are with respect to network ground terminal.
- Test one pin at a time.
- Measured with V_{IL} applied to CE and a logic high stored.
- Measured with a programmed logic condition for which the output test is at a low logic level. Output sink current is applied through a resistor to V_{CC}.
- Duration of short circuit should not exceed 1 second.
- I_{CC} is measured with the chip enable input at a logic high, 1₁-1₁₅ = GND.
- Guaranteed, but not tested.
- On unprogrammed device apply 10V - 1₁-1₁₅.
- Not testable on unprogrammed device.

Field Programmable Logic Array (16 × 48 × 8)

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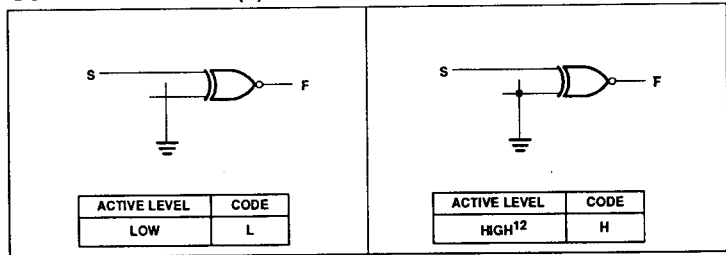
LOGIC PROGRAMMING

The FPLA can be programmed by means of Logic programming equipment.

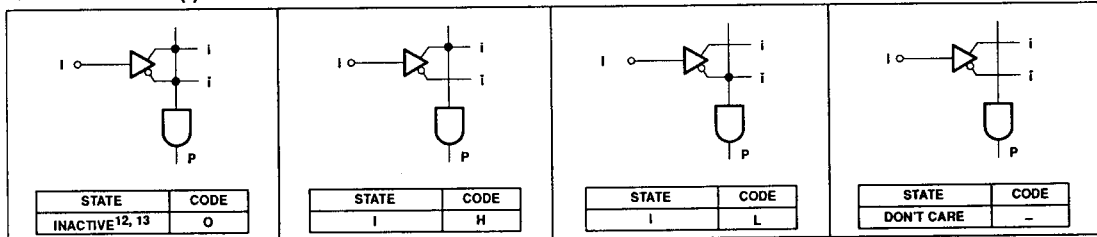
With Logic programming, the AND/OR/EX-OR gate input connections necessary to implement the desired logic function are coded directly from logic equations using the Program Table.

In this Table, the logic state or action of variables I, P and F, associated with each Sum Term S_n , is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

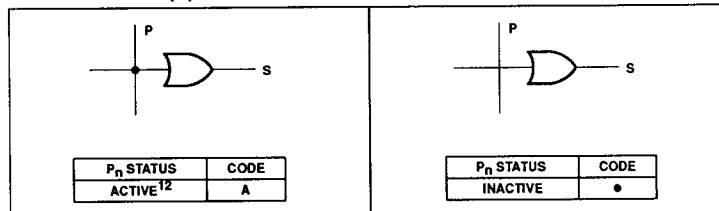
OUTPUT POLARITY - (F)



"AND" ARRAY - (I)



"OR" ARRAY - (F)



NOTES:

- 12. This is the initial unprogrammed state of all links.
- 13. Any gate P_n will be unconditionally inhibited if any one of its (I) link pairs is left intact.

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82S100/101

TIMING DEFINITIONS

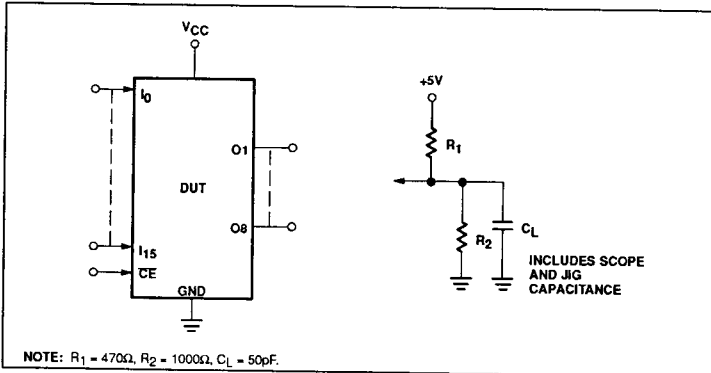
SYMBOL	PARAMETER
t_{CE}	Delay between beginning of Chip Enable Low (with input valid) and when Data Output becomes valid.
T_{CD}	Delay between when Chip Enable becomes High and Data Output is in Off-state (Hi-Z or High).
T_{PD}	Delay between beginning of valid input (with Chip Enable Low) and when Data Output becomes valid.

VIRGIN STATE

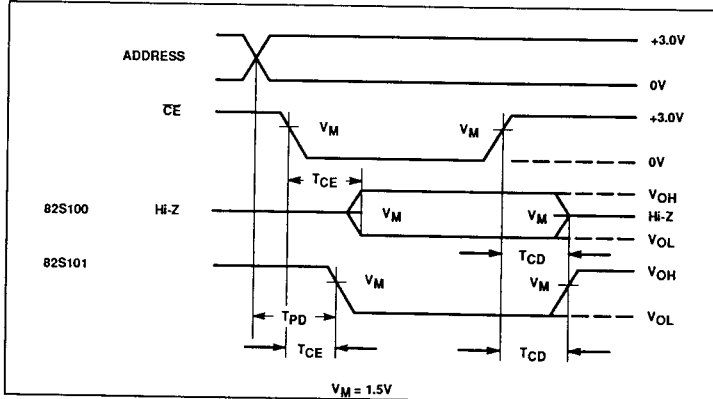
The 82S100/101 virgin devices are factory shipped in an unprogrammed state, characterized by:

1. All internal Ni-Cr links are intact.
2. Each product term (P-term) contains both True and Complement values of every input variable I (P-terms always logically "false").
3. The "OR" Matrix contains all 48 P-terms.
4. The polarity of each output is set to active-High (Fp function).
5. All outputs are at a Low logic level.

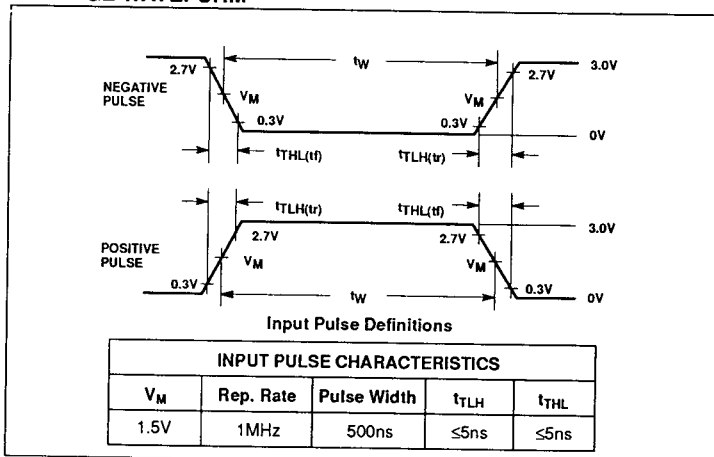
TEST LOAD CIRCUITS



TIMING DIAGRAM



VOLTAGE WAVEFORM



Signetics

Packaging Information

T.90-20

Military Products

SIGNETICS STANDARD PACKAGE DESCRIPTIONS

All Military package case outlines and physical dimensions conform with the current revision MIL-M-38510, Appendix C, except for package types which are not included in that specification.

The physical dimensions for standard package types which are not included in Appendix C are included herein in Appendix C format. Case outline letters are assigned to these packages according to JEDEC Publication 101 as follows:

- U: Leadless chip carriers
- X: Dual-in-line packages
- Y: Flat packages
- Z: All other configurations

A case outline suffix number is assigned herein for identification purposes only, and is not marked on the product.

Signetics Military products are offered in a wide range of package configurations to optimally fit our customer needs.

- Dual-in-line Packages; Frit glass sealed CERDIP (F package family) with 8-40 leads, and side-brazed ceramic (I package family) with 48-64 leads.
- Flat Packages; Frit glass sealed alumina CERPAC (W package family) with 14-28 leads, and brazed leaded ceramic (Q package family) with 52 leads.

- Ceramic Chip Carriers; triple laminated, metal-lidded LCC (G package family) with 20-68 terminals.
- Pin Grid Array; metal-lidded ceramic pin grid (P package family) with 68-100 leads.
- Shown in Table 1 are the case outline letters assigned according to Appendix C of MIL-M-38510 and JEDEC publication 101. Unless otherwise noted, all package types are Configuration 1 and all lead finishes are hot solder dip Finish "A".

Table 1.

Package Description	Type Designation	Case Outline	Theta-JC °C/Watt ⁴
8DIP3	D-4	P	28
14DIP3	D-1	C	28
16DIP3	D-2	E	28
18DIP3	D-6	V	28
20DIP3	D-8	R	28
22DIP4	D-7	W	28
24DIP3	D-9	L	28
24DIP4	D-11	X ²	28
24DIP6	D-3	J	28
28DIP6	D-10	X ²	28
40DIP6	D-5	Q	28
48DIP6	D-14 ¹	X ²	28
50DIP9	D-12 ¹	X ²	28
64DIP9	D-13 ¹	X ²	28
14FLAT	F-2	D	22
16FLAT	F-5	F	22
18FLAT	F-10	Y ²	22
20FLAT	F-9	S	22
24FLAT	F-6	K	22
28FLAT	F-11	Y ²	22
52FLAT	Y-1 ¹	Y ²	22
18LLCC	C-9	U ²	20
20LLCC	C-2 ³	2	20
28LLCC	C-4 ³	3	20
32LLCC	C-12	U ²	20
44LLCC	C-5	U ²	20
68LLCC	C-7	U ²	20
68PGA	P-AB	Z ²	20
84PGA	P-AB	Z ²	20

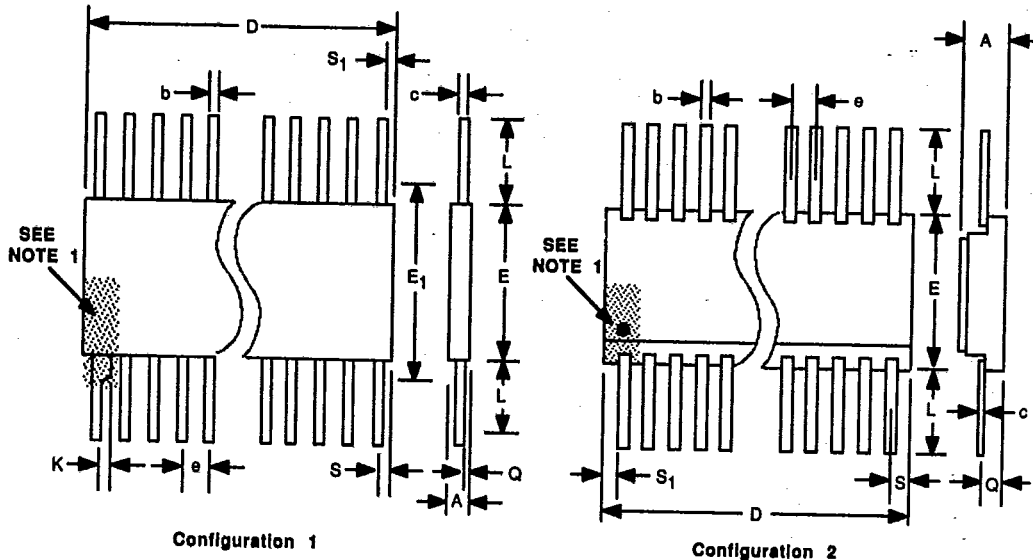
NOTES:

1. Configuration 2.
2. Per JEDEC publication 101.
3. Dimension A (LLCC thickness) is 75mils maximum.
4. See RADC test report RADC-TR-86-97 for thermal resistance confidence and derating.

Packaging Information

T-90-20

CASE OUTLINES Y (FLAT PACKAGES)



NOTES:

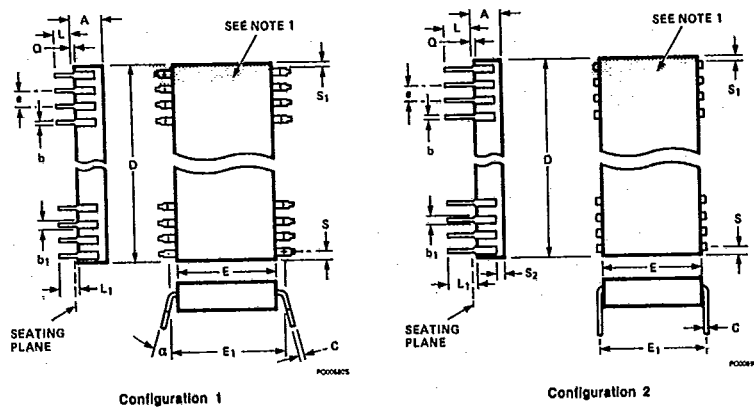
1. A lead tab (enlargement) or index dot is located within the shaded area shown at Pin 1. Other pin numbers proceed sequentially from Pin 1 counterclockwise (as viewed from the top of the device).
2. This dimension allows for off-center lid, meniscus, and glass overrun.
3. The reference pin spacing is 0.050 between centerlines. Each pin centerline is located within ± 0.005 of its longitudinal position relative to the first and last pin numbers.
4. This dimension is measured at the point of exit of the lead body.
5. This dimension applied to all four corner pins.
6. Lead dimensions include 0.003 inch allowance for hot solder dip lead finish.

OUTLINE	Y1		NOTES
CONFIGURATION	2		
NO. LEADS	52		
SIG. PKG.	QP		
SYMBOL	INCHES		
	Min	Max	
A	0.045	0.100	6
b	0.015	0.026	
c	0.008	0.015	
D	-	1.330	2
E	0.620	0.660	3
e	0.050 BSC		
L	0.250	0.370	4
Q	0.054	0.0666	
S	-	0.045	5
S1	0.005	-	5

T-90-20

Packaging Information

CASE OUTLINES X (DUAL IN-LINE PACKAGES)

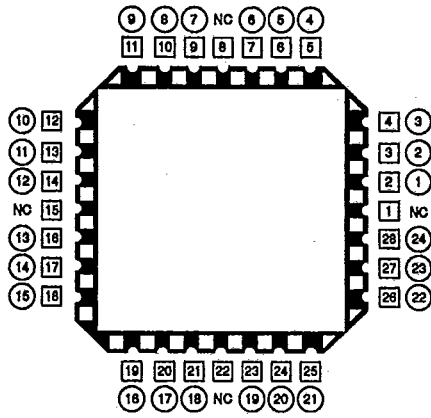


1. An index notch is located within the shaded area shown. Pin 1 is adjacent to the notch to the immediate left (as viewed from the top of the device) and other pin numbers proceed sequentially from Pin 1 counterclockwise.
2. The minimum limit for Dimension b1 is 0.023 inches for all four corner pins.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. This dimension is measured at the centerline of the leads for Configuration 2.
5. The reference pin spacing is 0.100 between centerlines. Each pin centerline is located within ± 0.010 of its longitudinal position relative to the first and last pin numbers.
6. This dimension is measured from the seating plane to the base plane.
7. This dimension applies to all four corner pins.
8. Lead dimensions include 0.003 inch allowance for hot solder dip lead finish.

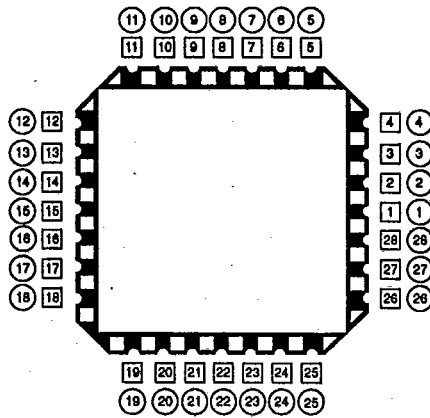
Packaging Information

T-90-20

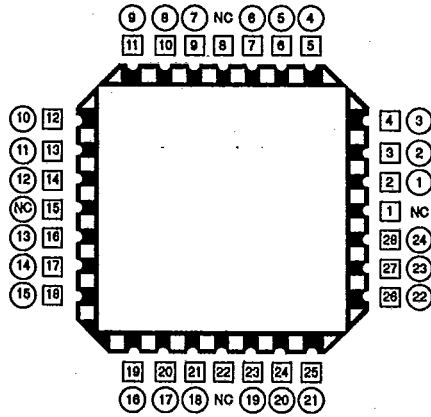
LEADLESS CHIP CARRIER (LLCC) PINOUTS



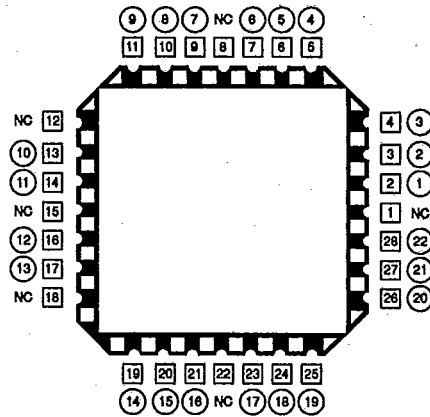
24-Lead Logic Pinout for 28 Terminal Chip Carrier



28-Lead Pinout for 28 Terminal Chip Carrier for all Device Types



24-Lead Memory Pinout for 28 Terminal Chip Carrier



22-Lead Memory Pinout for 28 Terminal Chip Carrier

□ = Chip Carrier Terminal Number
 ○ = Dual In-Line Lead Number
 NC = No Connect