

# 350MHZ, CRYSTAL-TO-LVCMOS/LVTTL FREQUENCY SYNTHESIZER

# ICS8402I

## General Description

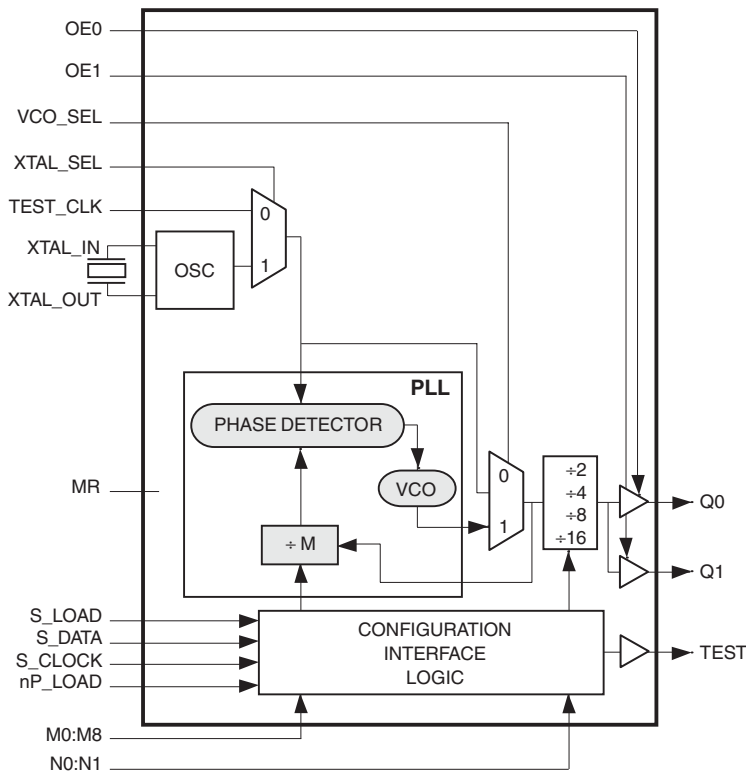


The ICS8402I is a general purpose, Crystal-to-LVCMOS/LVTTL High Frequency Synthesizer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS8402I has a selectable TEST\_CLK or crystal inputs. The VCO operates at a frequency range of 250MHz to 700MHz. The VCO frequency is programmed in steps equal to the value of the input reference or crystal frequency. The VCO and output frequency can be programmed using the serial or parallel interfaces to the configuration logic. The low phase noise characteristics of the ICS8402I make it an ideal clock source for Gigabit Ethernet and SONET applications.

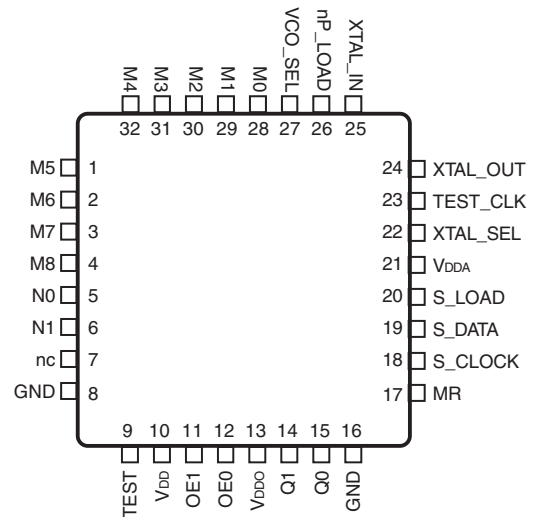
## Features

- Two LVCMOS/LVTTL outputs
- Selectable crystal oscillator interface or LVCMOS/LVTTL TEST\_CLK
- Output frequency range: 15.625MHz to 350MHz
- Crystal input frequency range: 12MHz to 40MHz
- VCO range: 250MHz to 700MHz
- Parallel or serial interface for programming counter and output dividers
- RMS period jitter: 30ps (maximum)
- Cycle-to-cycle jitter: 100ps (maximum)
- Full 3.3V or mixed 3.3V core/2.5V output supply
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

## Block Diagram



## Pin Assignment



**ICS8402I**  
**32 Lead LQFP**  
 7mm x 7mm x 1.4mm package body  
**Y Package**  
 Top View

**32 Lead VFQFN**  
 5mm x 5mm x 0.925mm package body  
**K Package**  
 Top View

## Functional Description

NOTE: The functional description that follows describes operation using a 25MHz crystal. Valid PLL loop divider values for different crystal or input frequencies are defined in the Input Frequency Characteristics, Table 5, NOTE 1.

The ICS8402I features a fully integrated PLL and therefore requires no external components for setting the loop bandwidth. A fundamental crystal is used as the input to the on-chip oscillator. The output of the oscillator is fed into the phase detector. A 25MHz crystal provides a 25MHz phase detector reference frequency. The VCO of the PLL operates over a range of 250MHz to 700MHz. The output of the M divider is also applied to the phase detector.

The phase detector and the M divider force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low), the PLL will not achieve lock. The output of the VCO is scaled by a divider prior to being sent to each of the LVCMOS output buffers. The divider provides a 50% output duty cycle.

The programmable features of the ICS8402I support two input modes to program the M divider and N output divider. The two input operational modes are parallel and serial. *Figure 1* shows the timing diagram for each mode. In parallel mode, the nP\_LOAD input is initially LOW. The data on inputs M0 through M8 and N0 and N1 is passed directly to the M divider and N output divider. On the LOW-to-HIGH transition of the nP\_LOAD input, the data is latched and the M divider remains loaded until the next LOW transition on nP\_LOAD or until a serial event occurs. As a result, the M and N bits can be hardwired to set the M divider and N output divider to a specific default state that will automatically occur

during power-up. The TEST output is LOW when operating in the parallel input mode. The relationship between the VCO frequency, the crystal frequency and the M divider is defined as follows:  

$$f_{VCO} = f_{XTAL} \times M$$

The M value and the required values of M0 through M8 are shown in Table 3B, Programmable VCO Frequency Function Table. Valid M values for which the PLL will achieve lock for a 25MHz reference are defined as  $10 \leq M \leq 28$ . The frequency out is defined as follows:  

$$f_{out} = \frac{f_{VCO}}{N} = \frac{f_{XTAL} \times M}{N}$$

Serial operation occurs when nP\_LOAD is HIGH and S\_LOAD is LOW. The shift register is loaded by sampling the S\_DATA bits with the rising edge of S\_CLOCK. The contents of the shift register are loaded into the M divider and N output divider when S\_LOAD transitions from LOW-to-HIGH. The M divide and N output divide values are latched on the HIGH-to-LOW transition of S\_LOAD. If S\_LOAD is held HIGH, data at the S\_DATA input is passed directly to the M divider and N output divider on each rising edge of S\_CLOCK. The serial mode can be used to program the M and N bits and test bits T1 and T0. The internal registers T0 and T1 determine the state of the TEST output as follows:

T1	T0	TEST Output
0	0	LOW
0	1	Shift Register Output
1	0	Output of M Divider
1	1	CMOS fOUT

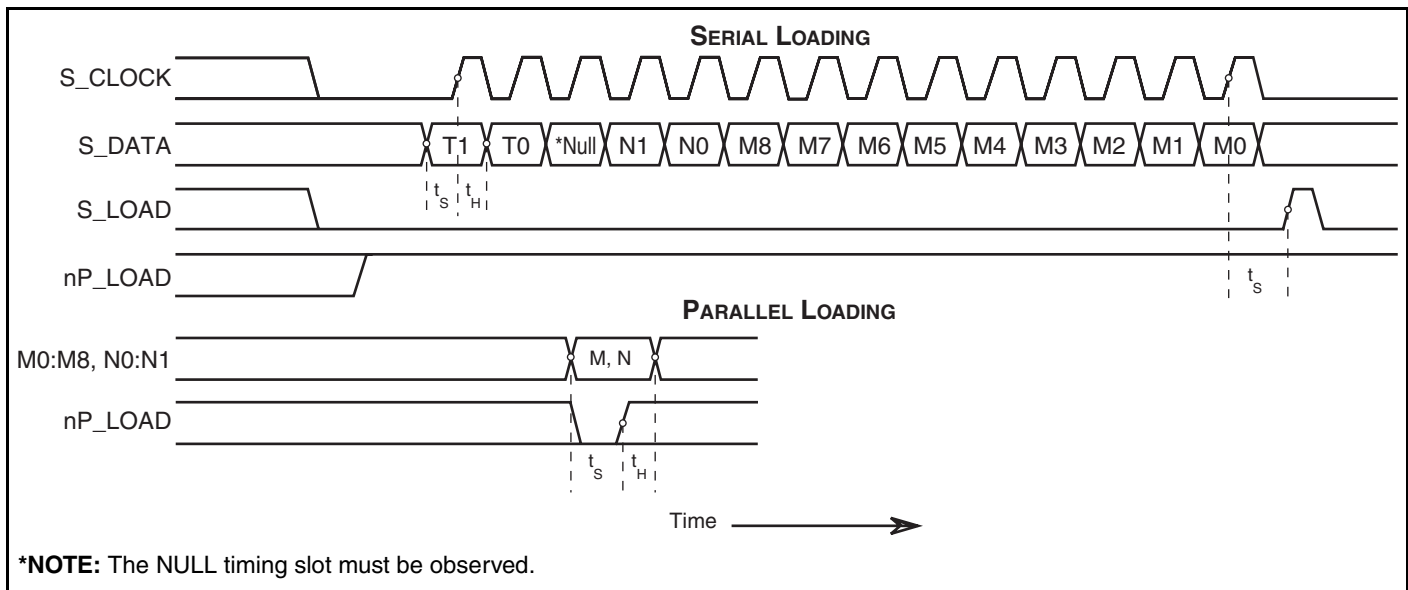


Figure 1. Parallel & Serial Load Operations

**Table 1. Pin Descriptions**

Number	Name	Type		Description
1	M5	Input	Pullup	M divider inputs. Data latched on LOW-to-HIGH transition of nP_LOAD input. LVCMOS/LVTTL interface levels.
2, 3, 4, 28, 29, 30, 31, 32	M6, M7, M8, M0, M1, M2, M3, M4	Input	Pulldown	
5, 6	N0, N1	Input	Pulldown	Determines output divider value as defined in Table 3C, Function Table. LVCMOS/LVTTL interface levels.
7	nc	Unused		
8, 16	GND	Power		No connect.
9	TEST	Output		Test output which is ACTIVE in the serial mode of operation. Output driven LOW in parallel mode. LVCMOS/LVTTL interface levels.
10	V <sub>DD</sub>	Power		Core supply pin.
11, 12	OE1, OE0	Input	Pullup	Output enable. When logic HIGH, the outputs are enabled (default). When logic LOW, the outputs are in Tri-State. See Table 3D, OE Function Table. LVCMOS / LVTTL interface levels.
13	V <sub>DDO</sub>	Power		Output supply pin.
14, 15	Q1, Q0	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels.
17	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the outputs to go low. When Logic LOW, the internal dividers and the outputs are enabled. Assertion of MR does not affect loaded M, N, and T values. LVCMOS/LVTTL interface levels.
18	S_CLOCK	Input	Pulldown	Clocks in serial data present at S_DATA input into the shift register on the rising edge of S_CLOCK. LVCMOS/LVTTL interface levels.
19	S_DATA	Input	Pulldown	Shift register serial input. Data sampled on the rising edge of S_CLOCK. LVCMOS/LVTTL interface levels.
20	S_LOAD	Input	Pulldown	Controls transition of data from shift register into the dividers. LVCMOS/LVTTL interface levels.
21	V <sub>DDA</sub>	Power		Analog supply pin.
22	XTAL_SEL	Input	Pullup	Selects between crystal oscillator or test inputs as the PLL reference source. Selects XTAL inputs when HIGH. Selects TEST_CLK when LOW. LVCMOS/LVTTL interface levels.
23	TEST_CLK	Input	Pulldown	Test clock input. LVCMOS/LVTTL interface levels.
24, 25	XTAL_OUT XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
26	nP_LOAD	Input	Pulldown	Parallel load input. Determines when data present at M8:M0 is loaded into M divider, and when data present at N1:N0 sets the N output divider value. LVCMOS/LVTTL interface levels.
27	VCO_SEL	Input	Pullup	Determines whether synthesizer is in PLL or bypass mode. LVCMOS/LVTTL interface levels.

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
C <sub>PD</sub>	Power Dissipation Capacitance (per output)	V <sub>DD</sub> , V <sub>DDO</sub> = 3.465V		13		pF
		V <sub>DD</sub> = 3.465V, V <sub>DDO</sub> = 2.625V		11		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ
R <sub>OUT</sub>	Output Impedance	V <sub>DDO</sub> = 3.465V	5	7	12	Ω
		V <sub>DDO</sub> = 2.625V		7		Ω

**Function Tables****Table 3A. Parallel and Serial Mode Function Table**

Inputs							Conditions
MR	nP_LOAD	M	N	S_LOAD	S_CLOCK	S_DATA	
H	X	X	X	X	X	X	Reset. Forces outputs LOW.
L	L	Data	Data	X	X	X	Data on M and N inputs passed directly to the M divider and N output divider. TEST output forced LOW.
L	↑	Data	Data	L	X	X	Data is latched into input registers and remains loaded until next LOW transition or until a serial event occurs.
L	H	X	X	L	↑	Data	Serial input mode. Shift register is loaded with data on S_DATA on each rising edge of S_CLOCK.
L	H	X	X	↑	L	Data	Contents of the shift register are passed to the M divider and N output divider.
L	H	X	X	↓	L	Data	M divider and N output divider values are latched.
L	H	X	X	L	X	X	Parallel or serial input do not affect shift registers.
L	H	X	X	H	↑	Data	S_DATA passed directly to M divider as it is clocked.

NOTE: L = LOW  
H = HIGH  
X = Don't care  
↑ = Rising edge transition  
↓ = Falling edge transition

Table 3B. Programmable VCO Frequency Function Table

VCO Frequency (MHz)	M Divide	256	128	64	32	16	8	4	2	1
		M8	M7	M6	M5	M4	M3	M2	M1	M0
250	10	0	0	0	0	0	1	0	1	0
275	11	0	0	0	0	0	1	0	1	1
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
650	26	0	0	0	0	1	1	0	1	0
675	27	0	0	0	0	1	1	0	1	1
700	28	0	0	0	0	1	1	1	0	0

NOTE 1: These M divide values and the resulting frequencies correspond to a TEST\_CLK or crystal frequency of 25MHz.

Table 3C. Programmable Output Divider Function Table

Inputs		N Divider Value	Output Frequency (MHz)	
N1	N0		Minimum	Maximum
0	0	2	125	350
0	1	4	62.5	175
1	0	8	31.25	87.5
1	1	16	15.625	43.75

Table 3D. OE Function Table

Inputs		Output	
OE0	OE1	Q0	Q1
0	0	Hi-Z	Hi-Z
0	1	Hi-Z	Enabled
1	0	Enabled	Hi-Z
1	1	Enabled	Enabled

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{CC}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $I_O$ (LVCMOS)	-0.5V to $V_{DDO} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$ 32 LQFP Package 32 VFQFN Package	47.9°C/W (0 lfpn) 37°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDA}$	Analog Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
$I_{DD}$	Power Supply Current				125	mA
$I_{DDA}$	Analog Supply Current				18	mA
$I_{DDO}$	Output Supply Current				10	mA

**Table 4B. LVCMOS/LVTTL DC Characteristics,  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		2		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage	OE0, OE1, MR, M0:M8, N0, N1, S_CLOCK, S_DATA, S_LOAD, nP_LOAD, VCO_SEL, XTAL_SEL	-0.3		0.8	V
		TEST_CLOCK	-0.3		1.3	V
$I_{IH}$	Input High Current	TEST_CLOCK, MR, M0:M4, M6:M8, N0, N1, S_CLOCK, S_DATA, S_LOAD, nP_LOAD	$V_{DD} = V_{IN} = 3.465\text{V}$		150	$\mu\text{A}$
		M5, XTAL_SEL, VCO_SEL, OE0, OE1	$V_{DD} = V_{IN} = 3.465\text{V}$		5	$\mu\text{A}$
$I_{IL}$	Input Low Current	TEST_CLOCK, MR, M0:M4, M6:M8, N0, N1, S_CLOCK, S_DATA, S_LOAD, nP_LOAD	$V_{DD} = 3.465\text{V}, V_{IN} = 0\text{V}$	-5		$\mu\text{A}$
		M5, XTAL_SEL, VCO_SEL, OE0, OE1	$V_{DD} = 3.465\text{V}, V_{IN} = 0\text{V}$	-150		$\mu\text{A}$
$V_{OH}$	Output High Voltage	TEST; NOTE 1	$V_{DDO} = 3.465\text{V}$	2.6		V
			$V_{DDO} = 2.625\text{V}$	1.8		V
$V_{OL}$	Output Low Voltage	TEST; NOTE 1	$V_{DDO} = 3.465$ or $2.625\text{V}$		0.5	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{DDO}/2$ . See Parameter Measurement Information section. *Load Test Circuit diagrams.*

**Table 5. Input Frequency Characteristics,  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{IN}$	Input Frequency	TEST_CLK; NOTE 1	12		40	MHz
		XTAL_IN, XTAL_OUT; NOTE 1	12		40	MHz
		S_CLOCK			50	MHz

NOTE 1: For the input crystal and TEST\_CLK frequency range, the M value must be set for the VCO to operate within the 250MHz to 700MHz range. Using the minimum input frequency of 12MHz, valid values of M are  $21 \leq M \leq 58$ . Using the maximum input frequency of 40MHz, valid values of M are  $7 \leq M \leq 17$ .

Table 6. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		12		40	MHz
Equivalent Series Resistance (ESR)				50	$\Omega$
Shunt Capacitance				7	pF

## AC Electrical Characteristics

Table 7A. AC Characteristics,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ 

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency		15.625		350	MHz
$f_{jit(cc)}$	Cycle-to-Cycle Jitter; NOTE 1, 3			40	100	ps
$f_{jit(per)}$	Period Jitter, RMS; NOTE 1			8	30	ps
$t_{sk(o)}$	Output Skew; NOTE 2, 3				80	ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	0.25		1.1	ns
$t_S$	Setup Time	M, N to nP_LOAD	5			ns
		S_DATA to S_CLOCK	5			ns
		S_CLOCK to S_LOAD	5			ns
$t_H$	Hold Time	M, N to nP_LOAD	5			ns
		S_DATA to S_CLOCK	5			ns
		S_CLOCK to S_LOAD	5			ns
odc	Output Duty Cycle	$f \leq 300\text{MHz}$	40		60	%
$t_{LOCK}$	PLL Lock Time				1	ms

See Parameter Measurement Information section.

NOTE 1: Jitter performance using XTAL inputs.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDO}/2$ .

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.



**Table 7B. AC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency		15.625		350	MHz
$f_{jit(cc)}$	Cycle-to-Cycle Jitter; NOTE 1, 3			40	100	ps
$f_{jit(per)}$	Period Jitter, RMS; NOTE 1				30	ps
$t_{sk(o)}$	Output Skew; NOTE 2, 3				60	ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	0.25		1.0	ns
$t_S$	Setup Time	M, N to nP_LOAD	5			ns
		S_DATA to S_CLOCK	5			ns
		S_CLOCK to S_LOAD	5			ns
$t_H$	Hold Time	M, N to nP_LOAD	5			ns
		S_DATA to S_CLOCK	5			ns
		S_CLOCK to S_LOAD	5			ns
odc	Output Duty Cycle	$f \leq 300\text{MHz}$	40		60	%
$t_{LOCK}$	PLL Lock Time				1	ms

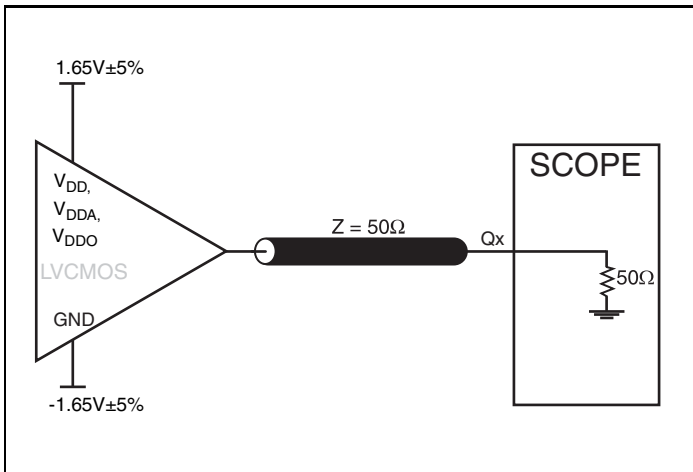
See Parameter Measurement Information section.

NOTE 1: Jitter performance using XTAL inputs.

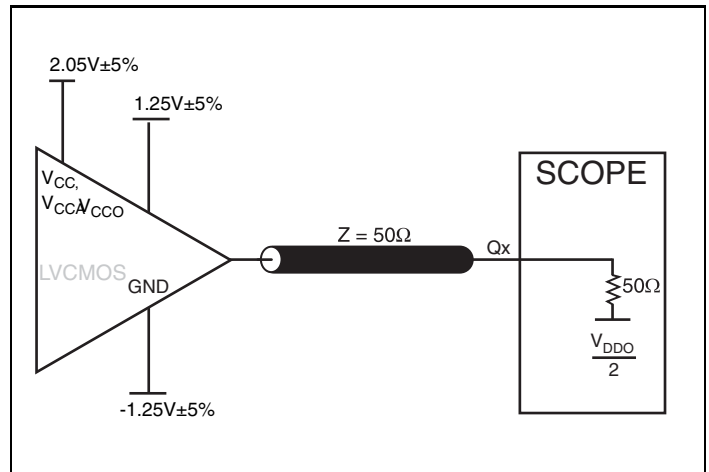
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDO}/2$ .

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

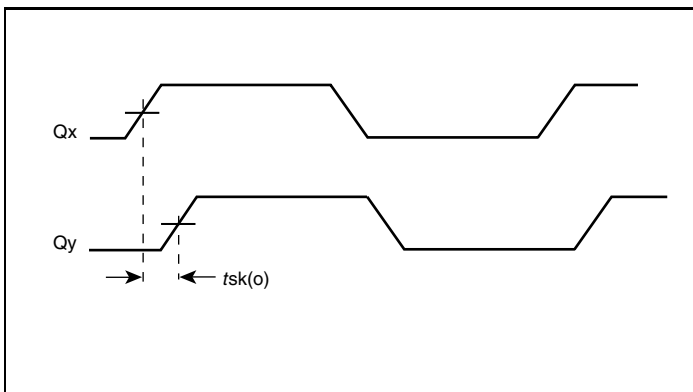
### Parameter Measurement Information



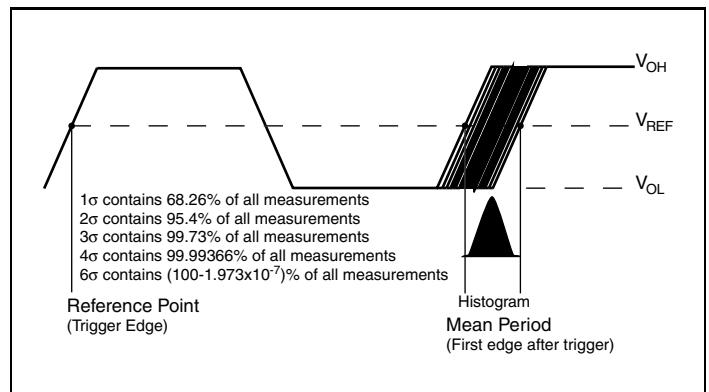
3.3/3.3V LVPECL Output Load AC Test Circuit



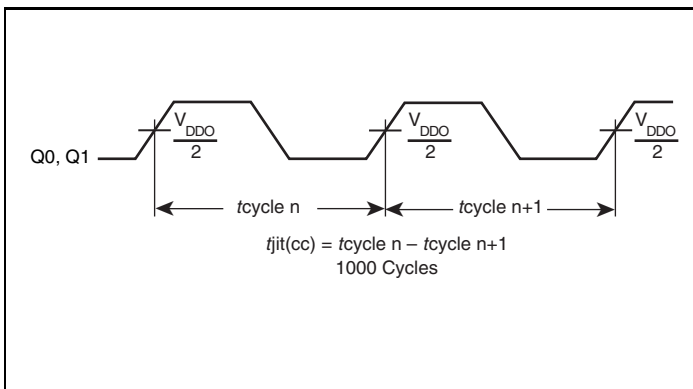
3.3V/2.5V LVPECL Output Load AC Test Circuit



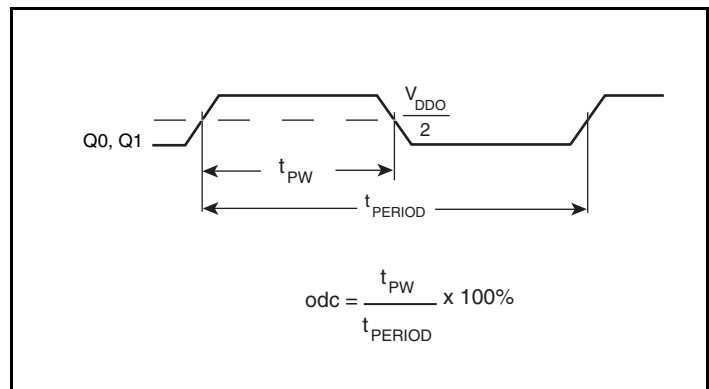
Output Skew



Period Jitter

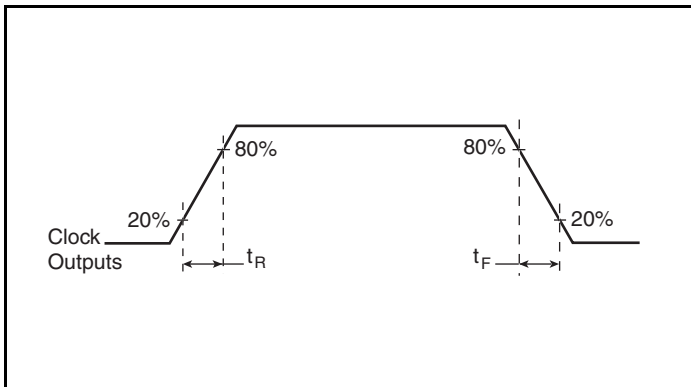


Cycle-to-Cycle Jitter



Output Duty Cycle/Pulse Width/Period

## Parameter Measurement Information, continued



Output Rise/Fall Time

## Application Information

### Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS84021 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{DD}$ ,  $V_{DDA}$  and  $V_{DDO}$  should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 2* illustrates how a  $10\Omega$  resistor along with a  $10\mu\text{F}$  and a  $0.01\mu\text{F}$  bypass capacitor should be connected to each  $V_{DDA}$  pin.

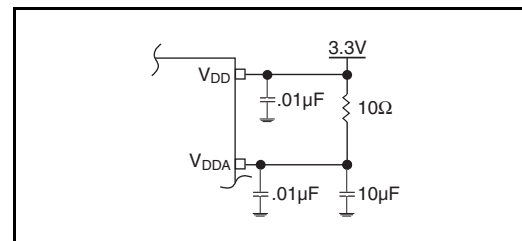
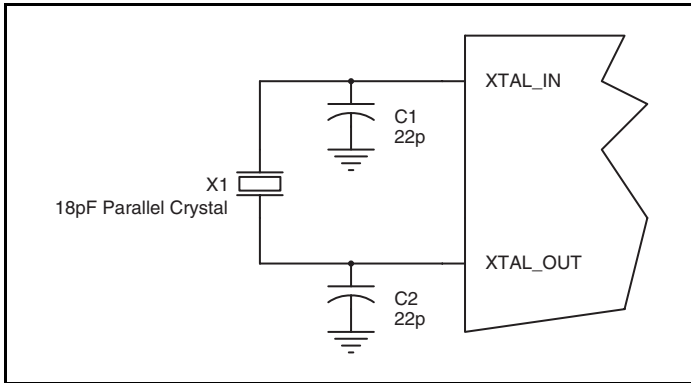


Figure 2. Power Supply Filtering

## Crystal Input Interface

The ICS8402I has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 3* below were determined using a 25MHz, 18pF parallel resonant crystal

and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

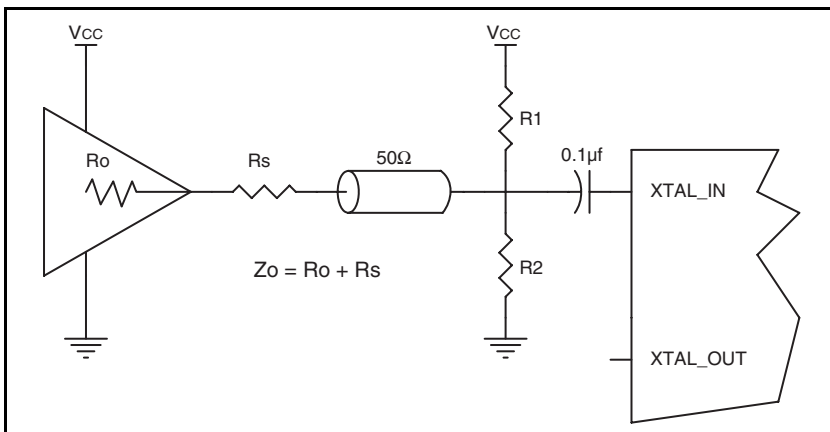


**Figure 3. Crystal Input Interface**

## LVCMOS to XTAL Interface

The XTAL\_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 4*. The XTAL\_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output

impedance of the driver ( $R_o$ ) plus the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50 $\Omega$  applications, R1 and R2 can be 100 $\Omega$ . This can also be accomplished by removing R1 and making R2 50 $\Omega$ .



**Figure 4. General Diagram for LVCMOS Driver to XTAL Input Interface**

## Recommendations for Unused Input and Output Pins

### Inputs:

#### Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL\_IN and XTAL\_OUT can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from XTAL\_IN to ground.

#### TEST\_CLK Input

For applications not requiring the use of the test clock, it can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from the TEST\_CLK to ground.

#### LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

### Outputs:

#### LVCMOS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100 $\Omega$  across. If they are left floating, we recommend that there is no trace attached.

## VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 5*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are

application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

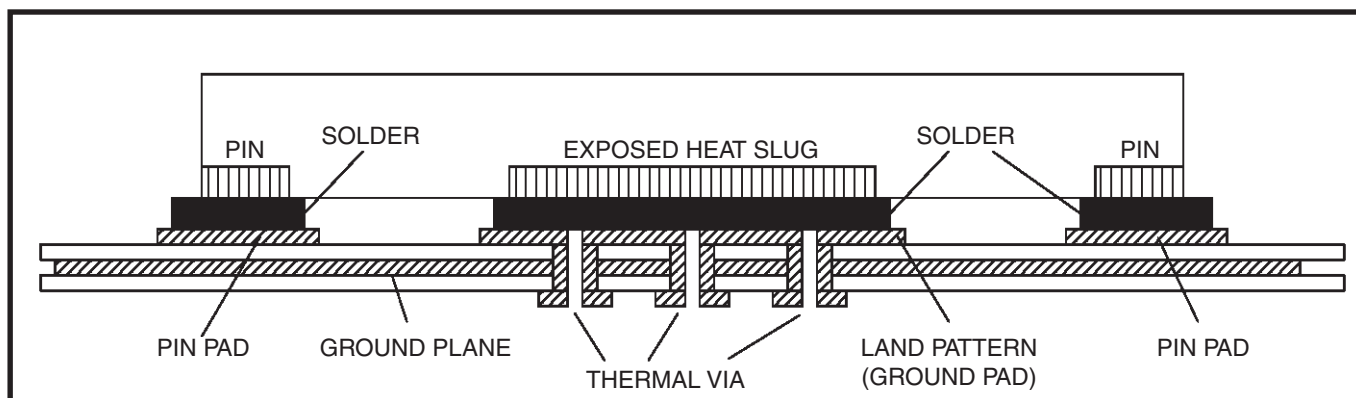


Figure 5. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

## Reliability Information

**Table 8A.  $\theta_{JA}$  vs. Air Flow Table for a 32 Lead LQFP**

$\theta_{JA}$ vs. Air Flow			
Linear Feet per Minute	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

**Table 8B.  $\theta_{JA}$  vs. Air Flow Table for a 32 Lead VFQFN**

$\theta_{JA}$ vs. Air Flow			
Linear Feet per Minute	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	37°C/W	32.4°C/W	29.0°C/W

## Transistor Count

The transistor count for ICS8402I is: 3784

## Package Outline and Package Dimension

### Package Outline - Y Suffix for 32 Lead LQFP

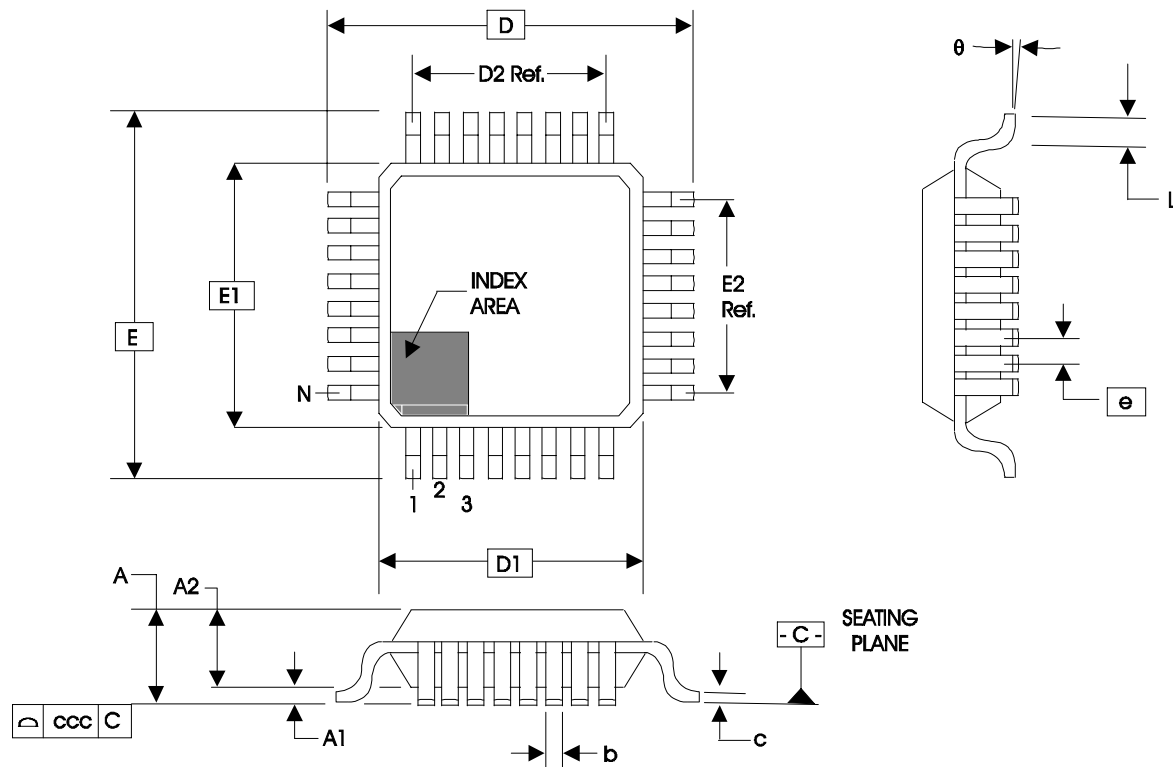
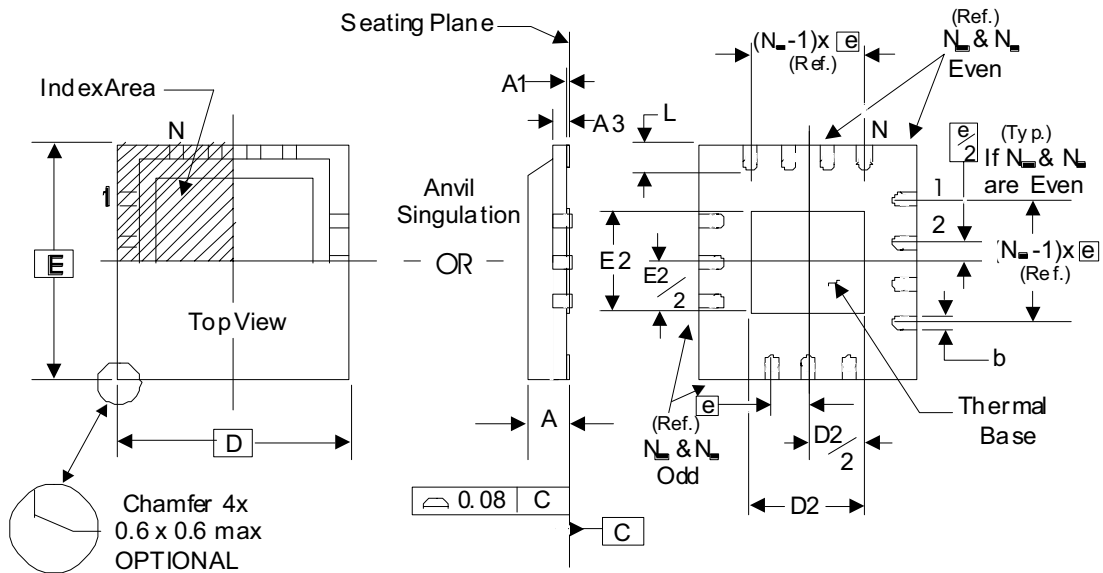


Table 9A. Package Dimensions for 32 Lead LQFP

JEDEC Variation: BBC - HD All Dimensions in Millimeters			
Symbol	Minimum	Nominal	Maximum
N	32		
A			1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09		0.20
D & E	9.00 Basic		
D1 & E1	7.00 Basic		
D2 & E2	5.60 Ref.		
e	0.80 Basic		
L	0.45	0.60	0.75
$\theta$	0°		7°
ccc			0.10

Reference Document: JEDEC Publication 95, MS-026

## Package Outline - K Suffix for 32 Lead VFQFN



**NOTE:** The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 8 below.

Table 9B. Package Dimensions for 32 Lead VFQFN

JEDEC Variation: VHHD-2/-4 All Dimensions in Millimeters			
Symbol	Minimum	Nominal	Maximum
N	32		
A	0.80		1.00
A1	0		0.05
A3	0.25 Ref.		
b	0.18	0.25	0.30
$N_D$ & $N_E$			8
D & E	5.00 Basic		
D2 & E2	3.0		3.3
e	0.50 Basic		
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220



## Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8402AYI	ICS8402AYI	32 Lead LQFP	Tray	-40°C to 85°C
8402AYIT	ICS8402AYI	32 Lead LQFP	1000 Tape & Reel	-40°C to 85°C
8402AYILF	ICS8402AYILF	"Lead-Free" 32 Lead LQFP	Tray	-40°C to 85°C
8402AYILFT	ICS8402AYILF	"Lead-Free" 32 Lead LQFP	1000 Tape & Reel	-40°C to 85°C
8402AKI	ICS8402AKI	32 Lead VFQFN	Tray	-40°C to 85°C
8402AKIT	ICS8402AKI	32 Lead VFQFN	2500 Tape & Reel	-40°C to 85°C
8402AKILF	ICS8402AKIL	"Lead-Free" 32 Lead VFQFN	Tray	-40°C to 85°C
8402AKILFT	ICS8402AKI	"Lead-Free" 32 Lead VFQFN	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial and industrial applications. Any other applications, such as those requiring high reliability or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

## Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		1	Pin Assignment - added 32 Lead VFQFN information.	10/10/07
		6	Absolute Maximum Ratings - added 32 Lead VFQFN package thermal impedance.	
		12	Added <i>LVCMOS to XTAL Interface</i> section.	
		13	Added <i>Recommendations for Unused Input/Output Pins</i> section.	
		13	Added <i>VFQFN EPAD Thermal Release Path</i> section.	
		14	Added 32 Lead VFQFN Reliability Information.	
		16	Added 32 Lead VFQFN Package Dimensions Table and Package Outline	
	T10	17	Ordering Information Table - added 32 Lead VFQFN ordering information.	

ICS8402I

350MHZ, CRYSTAL-TO-LVCMOS/LVTTL FREQUENCY SYNTHESIZER

Innovate with IDT and accelerate your future networks. Contact:

**www.IDT.com**

**For Sales**

800-345-7015  
408-284-8200  
Fax: 408-284-2775

**For Tech Support**

netcom@idt.com  
480-763-2056

---

**Corporate Headquarters**

Integrated Device Technology, Inc.  
6024 Silver Creek Valley Road  
San Jose, CA 95138  
United States  
800 345 7015  
+408 284 8200 (outside U.S.)

**Asia Pacific and Japan**

Integrated Device Technology  
Singapore (1997) Pte. Ltd.  
Reg. No. 199707558G  
435 Orchard Road  
#20-03 Wisma Atria  
Singapore 238877  
+65 6 887 5505

**Europe**

IDT Europe, Limited  
321 Kingston Road  
Leatherhead, Surrey  
KT22 7TU  
England  
+44 (0) 1372 363 339  
Fax: +44 (0) 1372 378851

