THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED
CURRENT CAGE CODE 67268

REV																					
SHEET																					
REV	H	H	H	H	H	H	H	H													
SHEET	15	16	17	18	19	20	21	22													
REV STATUS		REV	H	H	H	H	H	H	H	H	H	H	H	H	H	H
OF SHEETS		SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Roger Mell	**DLA LAND AMD MARITIME COLUMBUS, OHIO 43218-3990** http://www.dscc.dla.mil
STANDARD MICROCIRCUIT DRAWING	CHECKED BY D. A. DiCenzo	
	APPROVED BY Nelson A. Hauck	MICROCIRCUITS, MEMORY, DIGITAL, CMOS, 16K (2048 X 8) BIT STATIC RAM, MONOLITHIC SILICON
THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	DRAWING APPROVAL DATE 84 – 08 - 24	
AMSC N/A	REVISION LEVEL H	SIZE A / CAGE CODE **14933** / **84036**
		SHEET 1 OF 22

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

84036	01	J	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)
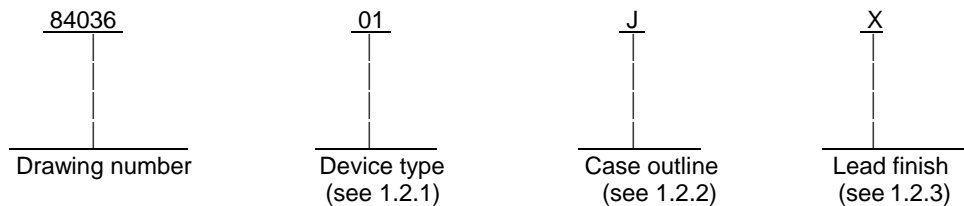
1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number 1/	Supply voltage variation	Address access time
01		10%	200 ns (synchronous)
02		10%	90 ns
03		10%	90 ns
04		10%	150 ns
05		10%	200 ns
06		10%	70 ns
07		10%	120 ns (synchronous)
08		10%	45 ns
09		10%	45 ns
10		10%	55 ns
11		10%	55 ns
12		10%	70 ns
13		10%	70 ns
14		10%	35 ns
15		10%	120 ns
16		10%	90 ns

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
J	CDIP2-T24 or GDIP1-T24	24	dual-in-line package
K	CDFP3-F24 or GDFP2-F24	24	flat package
L	CDIP4-T24 or GDIP3-T24	24	dual-in-line package
X	CQCC1-N32	32	rectangular chip carrier package
Y	See Figure 1	24	rectangular chip carrier package
Z	CQCC1-N32	32	rectangular chip carrier package with castellated instead of chamfered corners and extended pad metallization at terminal number 1.
3	CQCC1-N28	28	square chip carrier package

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1/ Generic numbers are listed on the standardized military drawing source approval bulletin at the end of this Standard Microcircuit Drawing and will also be listed in MIL-HDBK-103.

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1.3 <u>Absolute maximum ratings</u>.
 Supply voltage range (V_{CC})--------------------------------- -0.3 V dc to +7.0 V dc <u>2</u>/
 Temperature under bias------------------------------------- -55°C to +125°C
 Storage temperature range-------------------------------- -55°C to +150°C
 Maximum power dissipation (P_D) ------------------------- 1.0 W
 Lead temperature (soldering, 5 seconds)---------------- +275°C
 Thermal resistance, junction-to-case (θ_{JC}):-------------- See MIL-STD-1835
  Case Y-- 30°C/W
 Junction temperature (T_J)----------------------------------- +150°C <u>3</u>/
 All input or output voltages with respect to ground ---- -0.3 V dc to V_{CC} +0.3 V dc <u>4</u>/

1.4 <u>Recommended operating conditions</u>.
 Case operating temperature range (T_C) --------------------55°C to +125°C
 Input low voltage (V_{IL}):
  Device types 01 through 16 ---------------------------------0.3 V dc to 0.8 V dc <u>2</u>/
 Input high voltage (V_{IH}):
  Device types 01, 07--2.4 V dc to VCC +0.3 V dc <u>2</u>/
  Device types 02 through 06, 08 through 16 -----------2.2 V dc to VCC +0.3 V dc <u>2</u>/
 Supply voltage range (V_{CC}): -------------------------------4.5 V dc to 5.5 V dc <u>2</u>/
 Minimum chip enable low time -----------------------------40 ns <u>5</u>/
 Minimum chip enable high time-----------------------------40 ns <u>5</u>/
 Maximum input rise time ------------------------------------40 ns
 Maximum input fall time -------------------------------------40 ns

2. APPLICABLE DOCUMENTS

2.1 <u>Government specification, standards, and handbooks</u>. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

 DEPARTMENT OF DEFENSE SPECIFICATION

  MIL-PRF-38535   - Integrated Circuits, Manufacturing, General Specification for.

 DEPARTMENT OF DEFENSE STANDARDS

  MIL-STD-883   -   Test Method Standard Microcircuits.
  MIL-STD-1835   -   Interface Standard Electronic Component Case Outlines.

 DEPARTMENT OF DEFENSE HANDBOOKS

  MIL-HDBK-103 -   List of Standard Microcircuit Drawings.
  MIL-HDBK-780 -   Standard Microcircuit Drawings.

 (Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 <u>Order of precedence</u>. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

<u>2</u>/ All voltages referenced to V_{SS}.

<u>3</u>/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

<u>4</u>/ Negative undershoots to a minimum of -3.0 V are allowed with a maximum of 20 ns pulse width.

<u>5</u>/ For device types 02, 03, and 06 only.

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3. REQUIREMENTS

3.1 <u>Item requirements</u>. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used. This drawing has been modified to allow the manufacturer to use the alternate die/fabrication requirements of paragraph A.3.2.2 of MIL-PRF-38535 or alternative approved by the Qualifying Activity.

3.2 <u>Design, construction, and physical dimensions</u>. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 <u>Case outline(s)</u>. The case outline(s) shall be in accordance with 1.2.2 herein and figure 1.

3.2.2 <u>Terminal connections</u>. The terminal connections shall be as specified on figure 2.

3.2.3 <u>Truth table(s)</u>. The truth table(s) shall be as specified on figure 3.

3.2.4 <u>Logic diagram(s)</u>. The logic diagram(s) shall be as specified on figure 4.

3.2.5 <u>Die overcoat</u>. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection only. Each coated microcircuit inspection lot (see inspection lot as defined in MIL-PRF-38535) shall be subjected to and pass the internal moisture content test at 5000 ppm (see method 1018 of MIL-STD-883). The frequency of the internal water vapor testing shall not be decreased unless approved by the preparing activity for class M. The TRB will ascertain the requirements as provided by MIL-PRF-38535 for classes Q and V. Samples may be pulled any time after seal.

3.3 <u>Electrical performance characteristics</u>. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 <u>Electrical test requirements</u>. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 <u>Marking</u>. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked.

3.5.1 <u>Certification/compliance mark</u>. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, Appendix A. For Class Q product built in accordance with A.3.2.2 of MIL-PRF-38535 or other alternative approved by the Qualifying Activity, the "QD" certification mark shall be used in place of the "QML" or "Q" certification mark.

3.6 <u>Certificate of compliance</u>. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 <u>Certificate of conformance</u>. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 <u>Notification of change</u>. Notification of change to DLA Land and Maritime-VA shall be required for any change that affects this drawing.

3.9 <u>Verification and review</u>. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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STANDARD MICROCIRCUIT DRAWING DLA LAND AMD MARITIME COLUMBUS, OHIO 43218-3990		REVISION LEVEL H	SHEET **4**

TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions 1/ 2/ V_{SS} = 0 V, 4.5 V $\leq V_{CC} \leq$ 5.5 V -55°C $\leq T_C \leq$ +125°C unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
High-level output voltage	V_{OH}	I_{OH} = -1 mA	1,2,3	01-07, 15,16	2.4		V
		I_{OH} = -4 mA	1,2,3	08-14			
Low-level output voltage	V_{OL}	I_{OL} = +3.2 mA	1,2,3	01,07		0.4	V
		I_{OL} = +4.0 mA		02,03, 06,15			
		I_{OL} = +2.0 mA		04,05, 16			
		I_{OL} = +8.0 mA		08-14			
High impedance output leakage current	I_{IOLZ} I_{IOHZ}	$\overline{OE}$ = V_{IH}	1,2,3	01,02, 06,07	-1.0	1.0	μA
				04,05, 09,11, 13,14, 15,16	-10.0	10.0	
				03,08, 10,12	-5.0	5.0	
Input leakage current	I_{IL} I_{IH}	V_{IN} = GND V_{IN} = 5.5 V	1,2,3	01,02, 06,07	-1.0	1.0	μA
				04,05, 15	-2.0	2.0	
				03,08, 10,12, 16	-5.0	5.0	
				09,11, 13,14	-10.0	10.0	
Operating supply current	I_{CC1}	V_{CC} = 5.5 V, f = fmax 3/ $\overline{CE}$ = V_{IL}, outputs open All other inputs at V_{IL}	1,2,3	01,07		10	mA
				04,05, 13,15, 16		90	
				02,03, 06		70	
				08,10, 12		85	
				09,11		120	
				14		150	

See footnotes at end of table.

TABLE I. <u>Electrical performance characteristics</u> - Continued.

Test	Symbol	Test conditions 1/ 2/ $V_{SS} = 0$ V, 4.5 V $\leq V_{CC} \leq 5.5$ V $-55°C \leq T_C \leq +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Standby supply current	I_{CC2}	$\overline{CE} = \overline{WE} = V_{IH}$, $I_O = 0$	1,2,3	02,03, 06		8	mA
				04,05		10	
				10,12, 15,16		15	
				09,11, 13,14		25	
Standby supply current	I_{CC3}	$\overline{CE} = V_{CC} -0.3$ V, $I_O = 0$	1,2,3	06,07		50	µA
				01,02		100	
				04,05		250	
				03,08, 10,12, 15,16		900	
				13		10	mA
				09,11, 14		20	
Data retention current	I_{CC4}	$\overline{CE} = V_{CC}$, $V_{CC} = 2.0$ V	1,2,3	01,02		50	µA
				04,05		100	
				08,10, 12,15, 16		200	
				03		300	
				06,07		25	
Input capacitance 4/	C_I	$V_I = V_{CC}$ or GND $f = 1$ MHz See 4.3.1c	4	All		10	pF
Output capacitance 4/	C_O	$V_I = V_{CC}$ or GND $f = 1$ MHz See 4.3.1c	4	All		12	pF

See footnotes at end of table.

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TABLE I. <u>Electrical performance characteristics</u> - Continued.

Test	Symbol	Test conditions 1/ 2/ V_{SS} = 0 V, 4.5 V ≤ V_{CC} ≤ 5.5 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Read/write cycle time	t_{AVAV}	5/ 6/	9, 10, 11	01	280		ns
				02,03,16	90		
				04	150		
				05	200		
				15	120		
				07	170		
				08,09	45		
				10,11	55		
				06,12,13	70		
				14	35		
Address access time	t_{AVQV}	5/ 6/	9, 10, 11	01		200	ns
				02,03,16		90	
				04		150	
				05		200	
				07,15		120	
				08,09		45	
				10,11		55	
				06,12,13		70	
				14		35	
Output hold after address change 4/	t_{AVQX}	5/ 6/	9, 10, 11	15,16	0		ns
				04,05	10		
				02,03,06, 07,08-14	5		
Output enable to output active 4/	t_{OLQX}	5/ 6/	9, 10, 11	01,07	10		ns
				02,03,06, 08,12,13	5		
				04,05,09, 11,14,15, 16	0		
Output enable access time	t_{OLQV}	5/ 6/	9, 10, 11	01,07,15		80	ns
				02,03,16		65	
				04		60	
				05		70	
				08,09		25	
				10,11		40	
				06,12,13		50	
				14		20	

See footnotes at end of table.

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TABLE I. <u>Electrical performance characteristics</u> - Continued.

Test	Symbol	Test conditions 1/ 2/ V_{SS} = 0 V, 4.5 V $\leq V_{CC} \leq$ 5.5 V -55°C $\leq T_C \leq$ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Chip enable to output active 4/	t_{ELQX}	5/ 6/	9, 10, 11	01,07	10		ns
				02,03,06, 08-14	5		
				04,05,15, 16	0		
Chip enable access time	t_{ELQV}	5/ 6/	9, 10, 11	01		200	ns
				02,03,16		90	
				04		150	
				05		200	
				07,15		120	
				08,09		45	
				10,11		55	
				06,12,13		70	
				14		35	
Chip enable to output in high Z 4/	t_{EHQZ}	5/ 6/	9, 10, 11	01		80	ns
				02,03,07, 15,16		50	
				04,05		60	
				08,09		25	
				10,11		30	
				06,12,13		35	
				14		15	
Write recovery time	t_{WHAV}	5/ 6/	9, 10, 11	02,03,04, 05,06,15, 16	10		ns
				09,11,14	0		
Chip enable to end-of-write	t_{ELWH}	5/ 6/	9, 10, 11	01	200		ns
				02,03,16	55		
				04	90		
				05,07	120		
				06	45		
				08,09,14	30		
				10-13	40		
				15	70		

See footnotes at end of table.

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TABLE I. <u>Electrical performance characteristics</u> - Continued.

Test	Symbol	Test conditions $\underline{1}/$ $\underline{2}/$ $V_{SS} = 0$ V, 4.5 V $\leq V_{CC} \leq 5.5$ V $-55°C \leq T_C \leq +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Address valid to end-of-write	t_{AVWH}	$\underline{5}/$ $\underline{6}/$	9, 10, 11	02,03, 12,13	65		ns
				04	100		
				05	130		
				15	105		
				06	50		
				08,09,14	30		
				10,11	45		
				16	80		
Address to $\overline{WE}$ setup time	t_{AVWL}	$\underline{5}/$ $\underline{6}/$	9, 10, 11	02-06, 15,16	10		ns
				07,08,09, 11,14	0		
				10	5		
				12,13	15		
Address to $\overline{CE}$ setup time	t_{AVEL}	$\underline{5}/$ $\underline{6}/$	9, 10, 11	01,07	0		ns
Output enable to output in high Z $\underline{4}/$	t_{OHQZ}	$\underline{5}/$ $\underline{6}/$	9, 10, 11	01		80	ns
				02,03,15, 16		40	
				04,07		50	
				05		60	
				08,09		25	
				10,11		30	
				06,12,13		35	
				14		15	
Write enable pulse width	t_{WLWH}	$\underline{5}/$ $\underline{6}/$	9, 10, 11	01	200		ns
				02,03,16	55		
				04	90		
				05,07	120		
				15	70		
				08,11	25		
				06,10, 12,13	40		
				09,14	20		

See footnotes at end of table.

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TABLE I. <u>Electrical performance characteristics</u> - Continued.

Test	Symbol	Test conditions 1/ 2/ V_{SS} = 0 V, 4.5 V $\leq V_{CC} \leq$ 5.5 V -55°C $\leq T_C \leq$ +125°C unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Data setup to end-of-write	t_{DVWH}	5/ 6/	9, 10, 11	01	80		ns
				02,03,06, 12,13,16	30		
				04,07	50		
				05	70		
				08,09	20		
				10,11	25		
				15	35		
				14	15		
Data hold after end-of-write	t_{WHDX}	5/ 6/	9, 10, 11	01,06,07	10		ns
				02,03,04, 05,15,16	15		
				08,09,11, 14	0		
				10,12,13	5		
Minimum chip-enable high time after write	t_{EHEL}	5/ 6/	9, 10, 11	01	80		ns
				07	50		
Address hold time after $\overline{CE}$ low	t_{ELAX}	5/ 6/	9, 10, 11	01	50		ns
				07	30		
Chip-enable pulse width during write	t_{ELEH}	5/ 6/	9, 10, 11	01	200		ns
				07	120		
Write enable pulse setup time	t_{WLEH}	5/ 6/	9, 10, 11	01	200		ns
				02,03,16	55		
				04	90		
				05,07	120		
				08	30		
				06,10, 12,13	40		
				09,14	20		
				11	25		
				15	70		

1/ All voltages referenced to V_{SS}.
2/ Negative undershoots to a minimum of -0.3 V are allowed with a maximum of 20 ns pulse width.
3/ fmax = 1/$_{tAVAV}$
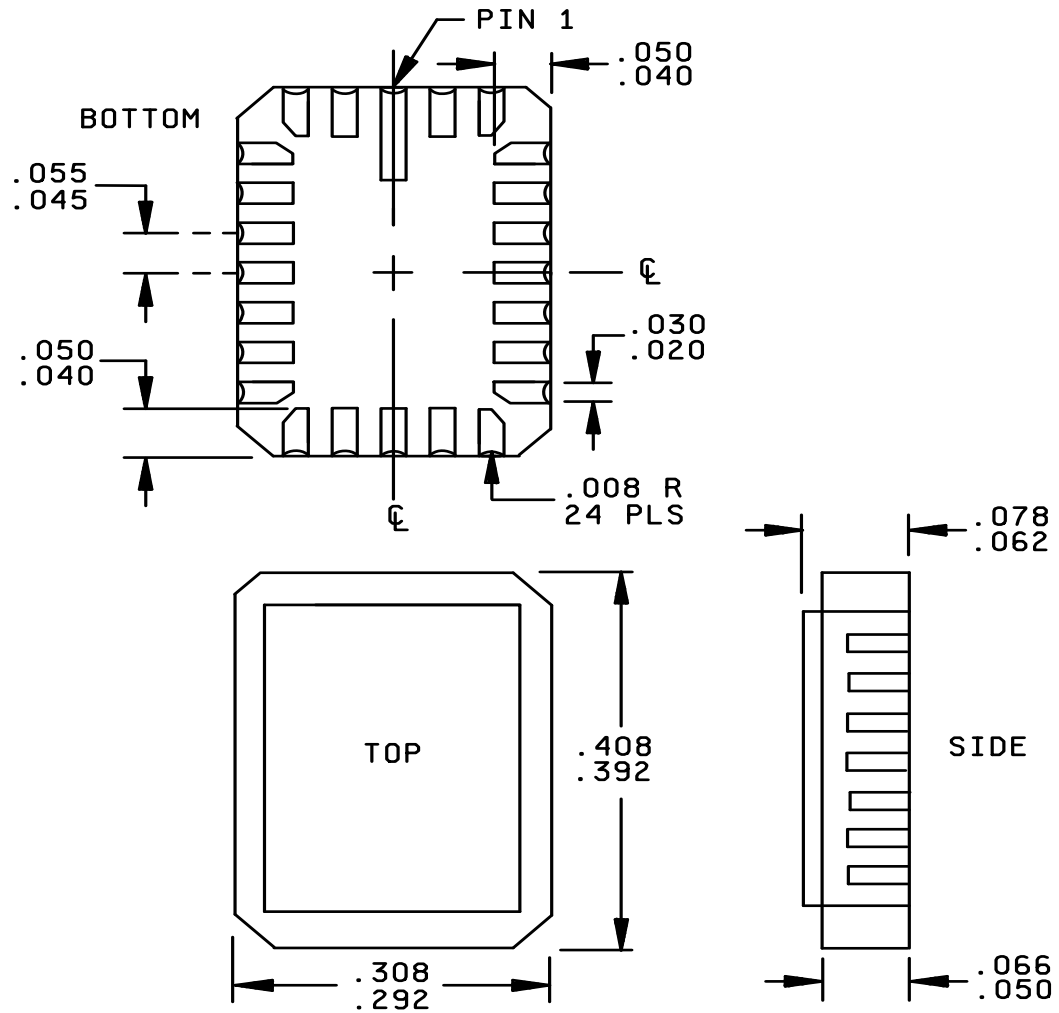4/ Tested initially, and after any design or process change which could affect these parameters.
5/ AC measurements assume transition time $\leq$ 5 ns and input levels are from V_{SS} to 3.0 V. Output load is specified on figure 5. Reference timing levels are at 1.5 V.
6/ For timing waveforms, see figure 6.

Case Y

24 PIN RECTANGULAR LEADLESS CHIP CARRIER

Notes:
1. Dimensions are in inches.
2. Metric equivalents are for general information only.

Inches	mm
.008	0.20
.020	0.50
.030	0.76
.040	1.01
.045	1.14
.050	1.27
.055	1.39
.062	1.57
.066	1.68
.078	1.98
.292	7.41
.308	7.82
.392	9.95
.408	10.36

FIGURE 1. Case outline.

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Device Types	All				
Case Outlines	X and Z		Y, J, K, and L		3
Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol
1	NC	1	A7	1	A7
2	NC	2	A6	2	A6
3	NC	3	A5	3	A5
4	A7	4	A4	4	A4
5	A6	5	A3	5	A3
6	A5	6	A2	6	A2
7	A4	7	A1	7	NC
8	A3	8	A0	8	NC
9	A2	9	DQ0, I/O0	9	A1
10	A1	10	DQ1, I/O1	10	A0
11	A0	11	DQ2, I/O2	11	DQ1, I/O1
12	NC	12	V_{SS}	12	DQ2, I/O2
13	DQ0, I/O0	13	DQ3, I/O3	13	DQ3, I/O3
14	DQ1, I/O1	14	DQ4, I/O4	14	V_{SS}
15	DQ2, I/O2	15	DQ5, I/O5	15	DQ4, I/O4
16	V_{SS}	16	DQ6, I/O6	16	DQ5, I/O5
17	NC	17	DQ7, I/O7	17	DQ6, I/O6
18	DQ3, I/O3	18	$\overline{CE}$, $\overline{E}$	18	DQ7, I/O7
19	DQ4, I/O4	19	A10	19	DQ8, I/O8
20	DQ5, I/O5	20	$\overline{OE}$, $\overline{G}$	20	$\overline{CE}$, $\overline{E}$
21	DQ6, I/O6	21	$\overline{WE}$, $\overline{W}$	21	NC
22	DQ7, I/O7	22	A9	22	NC
23	$\overline{CE}$, $\overline{E}$	23	A8	23	A10
24	A10	24	V_{CC}	24	$\overline{OE}$, $\overline{G}$
25	$\overline{OE}$, $\overline{G}$	---		25	$\overline{WE}$, $\overline{W}$
26	$\overline{WE}$, $\overline{W}$	---		26	A9
27	NC	---		27	A8
28	A9	---		28	V_{CC}
29	A8	---		---	
30	NC	---		---	
31	NC	---		---	
32	V_{CC}	---		---	

FIGURE 2. Terminal connections.

Device types 01 and 07

Read cycle

Time reference	Inputs					Function
	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	A	DQ	
-1	H	X	X	X	Z	Memory disabled
0	Ψ	H	X	V	Z	Cycle begins, addresses are latched
1	L	H	L	X	X	Output enabled
2	L	H	L	X	V	Output valid
3	Ξ	H	X	X	V	Read accomplished
4	H	X	X	X	Z	Prepare for next cycle (same as –1)
5	Ψ	H	X	V	Z	Cycle ends, next cycle begins (same as 0)

Write cycle

Time reference	Inputs					Function
	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	A	DQ	
-1	H	X	H	X	X	Memory disabled
0	Ψ	X	H	V	X	Cycle begins, addresses are latched
1	L	L	H	X	X	Write period begins
2	L	Ξ	H	X	V	Data is written
3	Ξ	H	H	X	X	Write completed
4	H	X	H	X	X	Prepare for next cycle (same as –1)
5	Ψ	X	H	V	X	Cycle ends, next cycle begins (same as 0)

Device types 02 – 06 and 08 - 16

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	DQ
V_{IH}	X	X	Deselect	High Z
V_{IL}	X	V_{IL}	Write	D_{IN}
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}
V_{IL}	V_{IH}	V_{IH}	Read	High Z

X = Don't care
H = HIGH
L = LOW
V = VALID
Ψ = TRANSITION HIGH TO LOW
Ξ = TRANSITION LOW TO HIGH

FIGURE 3. Truth table.

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Device types 01 and 07.
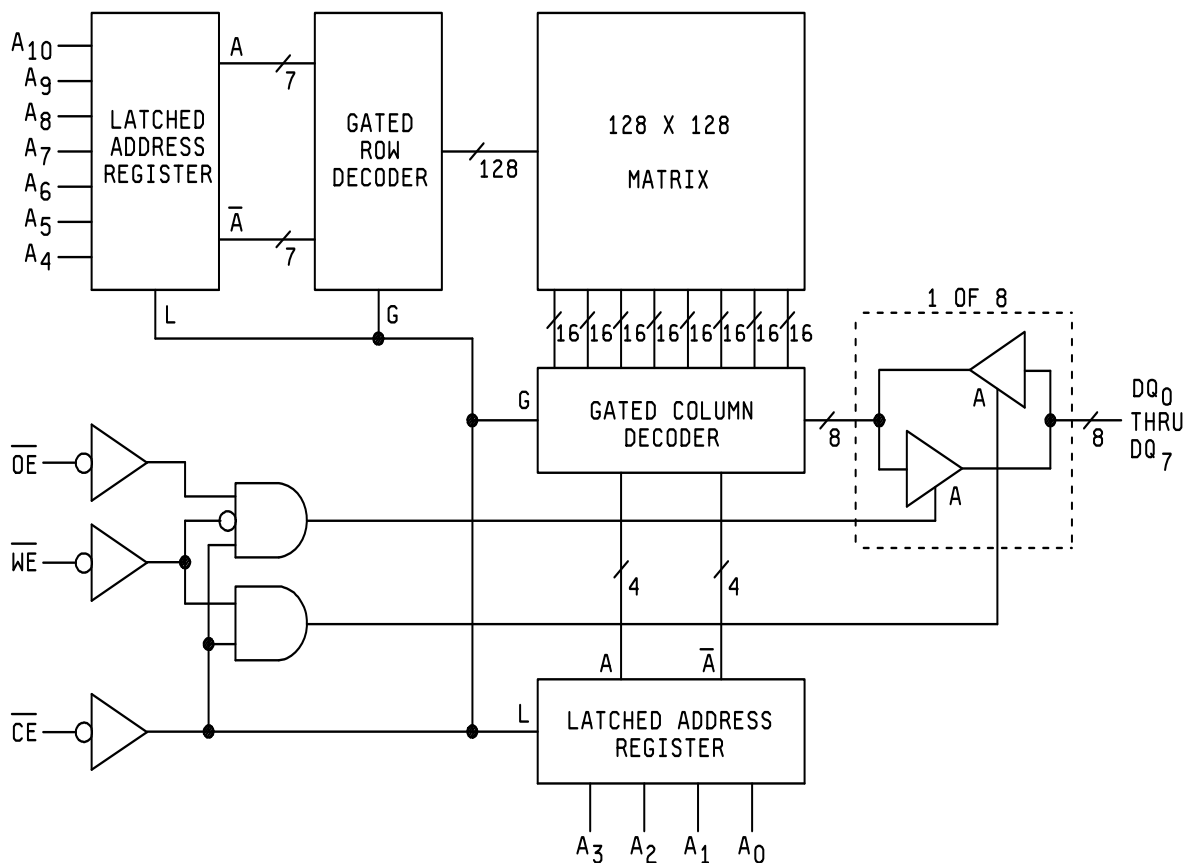
ALL LINES POSITIVE LOGIC –
   ACTIVE HIGH

THREE-STATE BUFFERS:
   A HIGH – OUTPUT ACTIVE

ADDRESS LATCHED AND GATED

DECODERS:
   LATCH ON RISING EDGE OF L
   GATE ON RISING EDGE OF G

FIGURE 4. Block diagram.

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FIGURE 4. Block diagram – Continued.

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+5V

480 Ω

D_{OUT}

255 Ω

30 pF
(SEE NOTE)
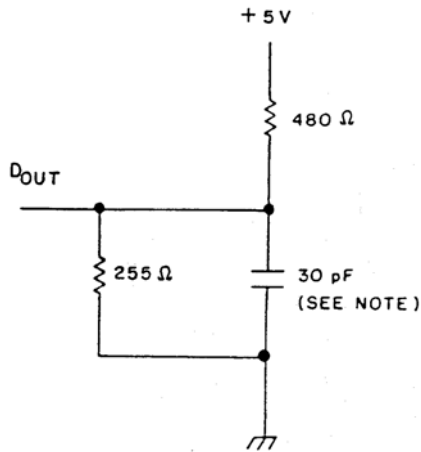
Circuit A or equivalent circuit

For all other switching parameters.

+5V

480 Ω

D_{OUT}

255 Ω

5 pF
(SEE NOTE)
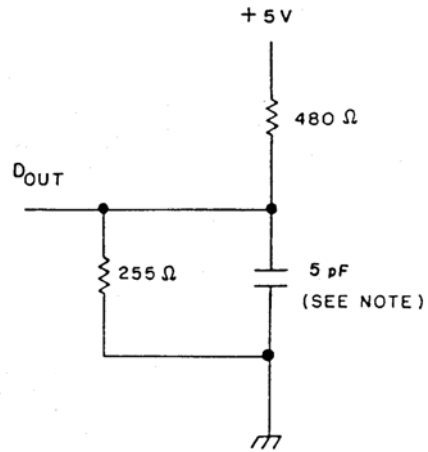
Circuit B or equivalent circuit

for t_{OLQX}, t_{ELQX}, t_{EHQZ}, and t_{OHQZ}.

NOTE:
    1. Including scope and jig capacitance.

FIGURE 5. Output loading.

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READ CYCLE
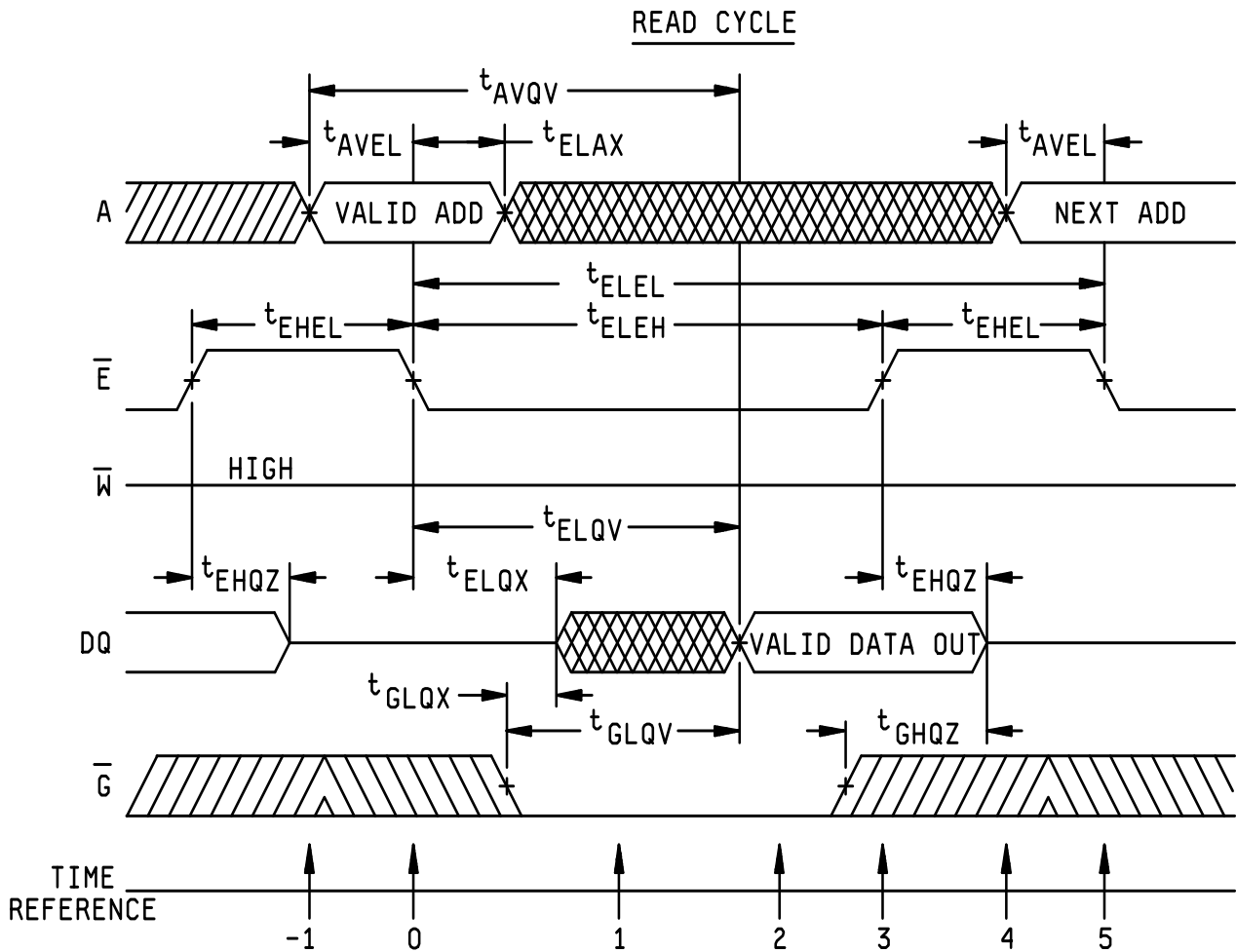
The address information is latched in the on chip registers on the falling edge of $\overline{CE}$ (t = 0), minimum address setup and hold time requirements must be met. After the required hold time, the address may change state without affecting device operation. During time (t = 1), the outputs become enabled but data is not valid until time (t = 2), $\overline{WE}$ must remain high throughout the read cycle. After the data has been read, $\overline{CE}$ may return high (t = 3). This will force the output buffers into a high impedance mode at time (t = 4). $\overline{OE}$ is used to disable the output buffers when in a logical "1" state (t = -1, 0, 3, 4, 5). After (t = 4) time, the memory is ready for the next cycle.

FIGURE 6. Timing waveforms.

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WRITE CYCLE

The write cycles is initiated on the falling edge of $\overline{CE}$ (t = 0), which latches the address information in the on chip registers. If a write cycle is to be performed where the output is not to become active, OE can be held high (inactive). Parameter t_{DVHW} and t_{WHDX} must be met for proper device operation regardless of OE. If CE and OE fall before WE falls (read mode), a possible bus conflict may exist. If CE rises before WE rises, reference data setup and hold times to the CE rising edge. The write operation is terminated by the first rising edge of WE (t = 2) or CE (t = 3). After the minimum CE high time (t_{EHEL}), the next cycle may begin. If a series of consecutive write cycles are to be performed, the WE line may be held low until all desired locations have been written. In this case, data setup and hold times must be referenced to the rising of CE.

FIGURE 6. Timing waveforms - Continued.

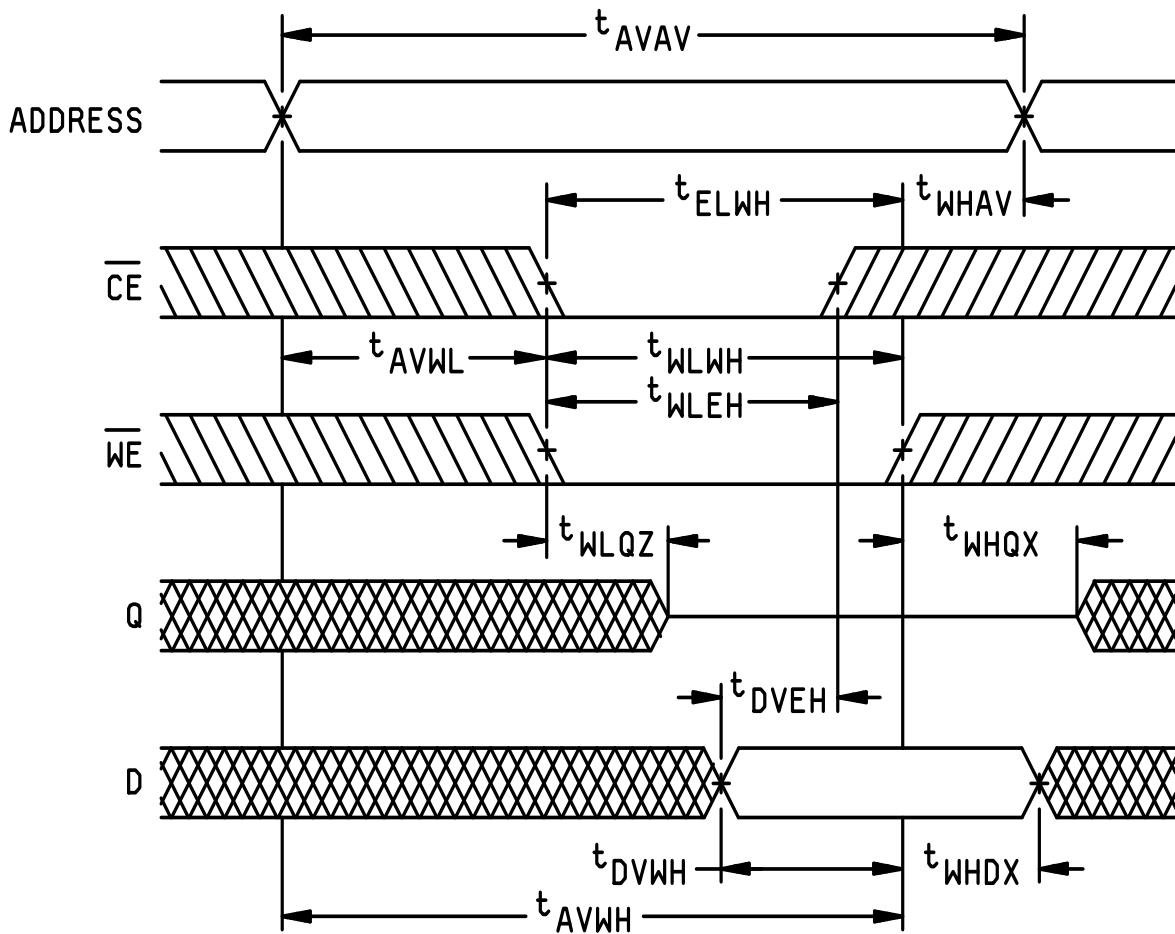| STANDARD MICROCIRCUIT DRAWING	SIZE A		84036
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WRITE CYCLE 1

NOTE: $\overline{G}$ is low throughout write cycle.

To write, addresses must be stable, $\overline{CE}$ low and $\overline{WE}$ falling low for a period no shorter than t_{WLWH}. Data is in referenced with the rising edge of WE or CE whichever occurs first (t_{DVWH} and t_{WHDX}).

While addresses are changing, WE must be high. When WE falls low, the I/O pins are still in the output state for a period of t_{WLOZ} and input data of the opposite phase to the outputs must not be applied (bus contention). If CE transitions low simultaneously with WE line transitioning low or after the WE transition, the output will remain in a high impedance state. OE is held continuously low.

FIGURE 6. Timing waveforms - Continued.

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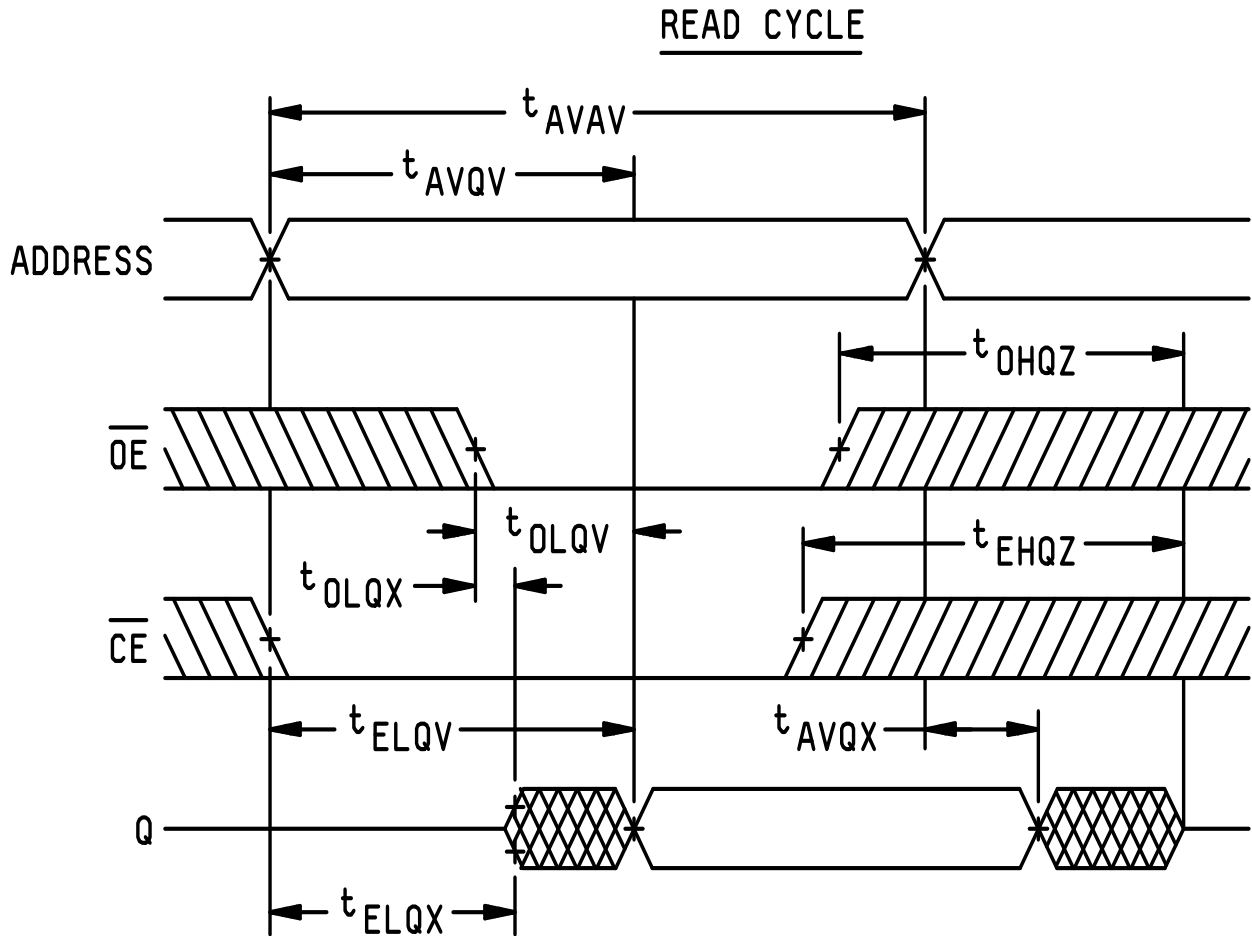
READ CYCLE

NOTE: $\overline{W}$ is high for a read cycle.

Addresses must remain stable for the duration of the read cycle. To read, $\overline{OE}$ and $\overline{CE}$ must be $\leq V_{IL}$ and $\overline{WE} \geq V_{IH}$.   The output buffers can be controlled independently by $\overline{OE}$ while $\overline{CE}$ is low. To execute consecutive read cycles, $\overline{CE}$ may be tied low continuously until all desired locations are accessed. When $\overline{CE}$ is low, addresses must be driven by stable logic levels and must not be in the high impedance stated.

FIGURE 6. Timing waveforms - Continued.

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4. VERIFICATION

4.1 <u>Sampling and inspection</u>. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 <u>Screening</u>. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

   (1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

   (2) $T_A = +125°C$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. <u>Electrical test requirements</u>.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8A, 8B, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8A, 8B, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 7, 9

* PDA applies to subgroup 1.

4.3 <u>Quality conformance inspection</u>. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 <u>Group A inspection</u>.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_I and C_O measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. Sample size is five (5) devices with no failures, and all input and output terminals tested.

d. Subgroups 7, 8A and 8B shall include verification of the truth table.

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4.3.2 <u>Groups C and D inspections</u>.

a.   End-point electrical parameters shall be as specified in table II herein.

b.   Steady-state life test conditions, method 1005 of MIL-STD-883.

   (1)   Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

   (2) T_A = +125°C, minimum.

   (3)   Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 <u>Packaging requirements</u>. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 <u>Intended use</u>. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 <u>Replaceability</u>. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 <u>Configuration control of SMD's</u>. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 <u>Record of users</u>. Military and industrial users should inform DLA Land and Maritime-VA when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime-VA will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-0544.

6.5 <u>Comments</u>. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 <u>Approved sources of supply</u>. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 11-02-14

Approved sources of supply for SMD 84036 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
8403601JA	3/	HM1-6516/883
8403601ZA	3/	HM1-6516/883
8403602JA	34371	HM1-65162/883
8403602ZA	3/	HM1-65162/883
8403603JA 4/	34371	HM1-65162C/883
8403603ZA	3/	HM1-65162C/883
8403604JA	3/ 3/	MKB6116P-82 SMJ5517-15JDM
8403604ZA	3/	SMJ5517-15FGM
8403605JA	3/ 3/	MKB6116P-83 SMJ5517-20JDM
8403605ZA	3/	SMJ5517-20FGM
8403606JA	34371	HM1-65162B/883
8403606ZA	3/	HM1-65162B/883
8403607JA	3/	HM1-6516B/883
8403607ZA	3/	HM1-6516B/883
8403608JA	61772	IDT6116LA45DB
8403608XA	3/	IDT6116LA45L32B
8403608LA	61772	IDT6116LA45TDB
8403608KA	3/	IDT6116LA45EB
84036083A	3/	IDT6116LA45L28B
8403608YA	3/	IDT6116LA45L24B

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
8403609JA	61772 0C7V7 3DTT2 3/	IDT6116SA45DB QP6116A-45DMB P4C116-45CWMB CY6116A-45DMB
8403609XA	0C7V7 3DTT2 3/ 3/	QP6117A-45LMB P4C116-45L32MB IDT6116SA45L32B CY6117A-45LMB
8403609LA	0C7V7 3/ 61772 3/ 3DTT2	QP7C128A-45DMB SMJ68CE16S-45JDM IDT6116SA45TDB CY7C128A-45DMB P4C116-45DMB
8403609KA	0C7V7 3/ 3/ 3DTT2	QP7C128A-45KMB IDT6116SA45EB CY7C128-45KMB P4C116-45FMB
84036093A	0C7V7 3/ 3/ 3DTT2	QP6116A-45LMB IDT6116SA45L28B CY6116A-45LMB P4C116-45L28MB
8403609YA	0C7V7 3/ 3/ 3DTT2	QP7C128A-45LMB IDT6116SA45L24B CY7C128A-45LMB P4C116-45LMB
8403610JA	61772	IDT6116LA55DB
8403610XA	3/ 0C7V7	IDT6116LA55L32B 6116-55/XA
8403610LA	61772	IDT6116LA55TDB
8403610KA	3/ 0C7V7	IDT6116LA55EB 6116-55/KA
84036103A	3/ 0C7V7	IDT6116LA55L28B 6116-55/3A
8403610YA	3/ 0C7V7	IDT6116LA55L24B 6116-55/YA
8403611JA	0C7V7 61772 3DTT2 3/	QP6116A-55DMB IDT6116SA55DB P4C116-55CWMB CY6116A-55DMB
8403611XA	0C7V7 3DTT2 3/ 3/	QP6117A-55LMB P4C116-55L32MB IDT6116SA55L32B CY6117A-55LMB

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
8403611LA	0C7V7 3/ 61772 3/ 3DTT2	QP7C128A-55DMB SMJ68CE16S-55JDM IDT6116SA55TDB CY7C128A-55DMB P4C116-55DMB
8403611KA	0C7V7 3/ 3/ 3DTT2	QP7C128A-55KMB IDT6116SA55EB CY7C128-55KMB P4C116-55FMB
84036113A	0C7V7 3/ 3/ 3DTT2	QP6116A-55LMB IDT6116SA55L28B CY6116A-55LMB P4C116-55L28MB
8403611YA	0C7V7 3/ 3/ 3DTT2	QP7C128A-55LMB IDT6116SA55L24B CY7C128A-55LMB P4C116-55LMB
8403612JA	61772	IDT6116LA70DB
8403612XA	3/	IDT6116LA70L32B
8403612LA	61772	IDT6116LA70TDB
8403612KA	3/	IDT6116LA70EB
84036123A	3/	IDT6116LA70L28B
8403612YA	3/	IDT6116LA70L24B
8403613JA	61772	IDT6116SA70DB
8403613XA	3/	IDT6116SA70L32B
8403613LA	61772	IDT6116SA70TDB
8403613KA	3/	IDT6116SA70EB
84036133A	3/	IDT6116SA70L28B
8403613YA	3/	IDT6116SA70L24B
8403614JA	0C7V7 3DTT2 3/	QP6116A-35DMB P4C116-35CWMB CY6116A-35DMB
8403614XA	0C7V7 3DTT2 3/	QP6117A-35LMB P4C116-35L32MB CY6117A-35LMB
8403614LA	0C7V7 3/ 3/ 3DTT2	QP7C128A-35DMB SMJ68CE16S-35JDM CY7C128A-35DMB P4C116-35DMB

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
8403614KA	0C7V7 3/ 3DTT2	QP7C128A-35KMB CY7C128A-35KMB P4C116-35FMB
84036143A	0C7V7 3/ 3DTT2	QP6116A-35LMB CY6116A-35LMB P4C116-35L28MB
8403614YA	0C7V7 3/ 3DTT2	QP7C128A-35LMB CY7C128A-35LMB P4C116-35LMB
8403615JA	3/ 61772	L6116HMB120 IDT6116LA120DB
8403615XA	3/ 3/ 0C7V7	L6116TMB120 IDT6116LA120L32B 6116-120/XA
8403615LA	3/ 61772	L6116CMB120 IDT6116LA120TDB
8403615KA	3/ 3/ 0C7V7	L6116FMB120 IDT6116LA120EB 6116-120/KA
84036153A	3/ 3/ 0C7V7	L6116KMB120 IDT6116LA120L28B 6116-120/3A
8403615YA	3/ 3/ 0C7V7	L6116TMB IDT6116LA120L24B 6116-120/YA
8403616JA	3/ 61772	L6116HMB90 IDT6116LA90DB
8403616XA	3/ 3/	L6116TMB90 IDT6116LA90L32B
8403616LA	3/ 61772	L6116CMB90 IDT6116LA90TDB
8403616KA	3/ 3/	L6116FMB90 IDT6116LA90EB
84036163A	3/ 3/	L6116KMB90 IDT6116LA90L28B
8403616YA	3/ 3/	L6116TMB IDT6116LA120L24B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source.

Vendor CAGE number	Vendor name and address
34371	Intersil Corporation 2401 Palm Bay Blvd PO Box 883 Melbourne, FL 32902-0883
61772	Integrated Device Technology 2975 Stender Way Santa Clara, CA 95054
3DTT2	Pyramid Semiconductor Corporation 1340 Bordeaux Drive Sunnyvale, CA 94089
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051

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