






# 88PL810/88PL815/88PL830

High Current, Adjustable 8 Level  
LDO Regulator

**Datasheet**

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# Table of Contents

<b>Table of Contents</b> .....	<b>1</b>
<b>List of Tables</b> .....	<b>1</b>
<b>List of Figures</b> .....	<b>1</b>
<b>1 Signal Description</b> .....	<b>5</b>
1.1 Pin Configuration .....	5
1.2 Pin Description .....	6
1.2.1 Pin Types .....	6
<b>2 Electrical Specifications</b> .....	<b>7</b>
2.1 Absolute Maximum Ratings .....	7
2.2 Recommended Operating Conditions .....	7
2.3 Electrical Characteristics .....	8
<b>3 Functional Description</b> .....	<b>11</b>
3.1 Output Voltage – AnyVoltage™ Technology .....	12
3.2 Soft Start .....	13
3.3 Hiccup Current Limit .....	14
3.4 Output Capacitor (COUT) Selection .....	15
3.5 Input Capacitor .....	15
3.6 Enable .....	15
3.7 Minimum Load Current .....	15
3.8 Undervoltage Lockout (UVLO) .....	16
3.9 Thermal Shutdown .....	16
3.10 Thermal Considerations .....	17
<b>4 Functional Characteristics</b> .....	<b>19</b>
<b>5 Typical Characteristics</b> .....	<b>21</b>
5.1 IC Case and Board Temperature .....	21
<b>6 Mechanical Drawings</b> .....	<b>25</b>
6.1 Mechanical Dimensions .....	25
6.1.1 MSOP-8 Package .....	25
6.1.2 5x5mm QFN-5L Package .....	27
6.2 Typical Pad Layout Dimensions .....	29
<b>7 Ordering Information</b> .....	<b>33</b>
7.1 Ordering Part Numbers and Package Markings .....	33



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7.2	Sample Ordering Part Number.....	33
7.3	Package Markings.....	34
7.3.1	5 X 5 QFN-5 Package Marking.....	34
7.3.2	3 X 3 MSOP-8 Package Marking.....	34
<b>A</b>	<b>Revision History .....</b>	<b>35</b>

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## List of Tables

Table 1:	Product Table .....	5
Table 2:	Pin Type Definitions .....	6
Table 4:	Absolute Maximum Ratings .....	7
Table 5:	Recommended Operating Conditions.....	7
Table 6:	Electrical Characteristics .....	8
Table 7:	Output Voltage .....	12
Table 8:	Recommended Capacitors .....	15
Table 9:	MSOP-8L Dimensions .....	26
Table 10:	5x5mm QFN-5L Dimensions .....	28
Table 11:	Order Samples Table.....	33
Table 12:	Revision History.....	35



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## List of Figures

Figure 1:	Typical LDO Regulator .....	3
Figure 2:	3x3mm MSOP-8 - Top View .....	5
Figure 3:	5x5mm QFN-5 - Top View .....	5
Figure 4:	88PL810/88PL815/88PL830 Simplified Block Diagram.....	11
Figure 5:	Startt-Up Sequence .....	12
Figure 6:	VSET Voltage Steps for 2.5V Output.....	12
Figure 7:	Rise Time with CO <sub>UT</sub> = 10mF.....	13
Figure 8:	Rise Time with CO <sub>UT</sub> = 1000mF.....	13
Figure 9:	Hiccup Period .....	14
Figure 10:	Current Limit Response Time .....	14
Figure 11:	Startt-Up Using the Enable Pin.....	19
Figure 12:	Turn Off Using the Enable Pin .....	19
Figure 13:	Input Voltage Soft Start.....	19
Figure 14:	Input Voltage Hot Plug.....	19
Figure 15:	UVLO Thresholds .....	20
Figure 16:	Load Transient Response.....	20
Figure 17:	5x5mm QFN-5L Package .....	21
Figure 18:	Input Voltage Graphs.....	22
Figure 19:	Temperature Graphs .....	23
Figure 20:	Temperature Graphs (Continued).....	24
Figure 21:	88PL810/88PL815/88PL830 MSOP Mechanical Dimensions .....	25
Figure 22:	88PL810/88PL815/88PL830 5x5mm QFN-5L Mechanical Dimensions .....	27
Figure 23:	Recommended Solder Pad Layout for MSOP-8.....	29
Figure 24:	Recommended Solder Pad Layout for QFN-5.....	30
Figure 25:	Ordering Part Numbers and Package Markings .....	33
Figure 26:	Package Marking and Pin 1 Location for 5 X 5mm QFN-5.....	34
Figure 27:	Package Marking and Pin 1 Location for 3 X 3mm MSOP-8.....	34





## PRODUCT OVERVIEW

The 88PL810/88PL815/88PL830 family of devices are high current ultra-low-dropout linear (LDO) regulators, featuring up to 235mV at 3A dropout voltage and very low ground current. Quiescent current is typically 1.5mA and drops to 0.1A in shutdown. The devices protect themselves from short circuit conditions by turning OFF for about 6ms and ON ("hiccup"), thereby limiting temperature rise. In "Hot-Swap" applications, no additional circuitry is required since these devices have an integrated "Soft Start" mode. Additionally, a unique output voltage programming technique is used to provide eight output voltage options.

The whole 88PL810/15/30 family's output voltage can be adjusted to 8 different levels between 2.4V and 2.75V (2% or 50mV per step), for an input voltage range of 2.7V to 3.6V. This voltage is defined by the user with a single external resistor (RVSET). The 88PL810 device is adjustable in 30mV steps and the 88PL815 device is adjustable in 36mV steps.

The 88PL810/88PL815/88PL830 devices are stable with a 10µF ceramic output capacitor. However, any other type of capacitor up to 1000µF can be placed in parallel with it as long as the 10µF ceramic output capacitor is placed next to the 88PL810/88PL815/88PL830.

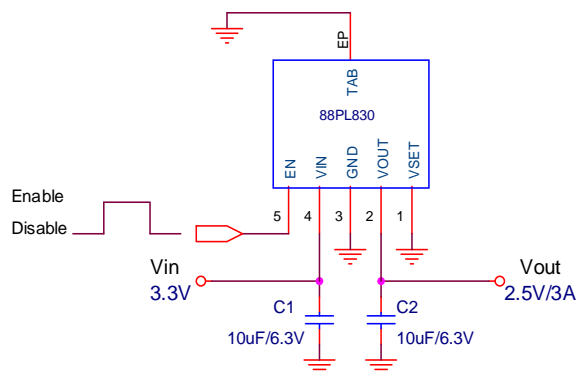
## Features

- 88PL810: 1.5V/1.0A; 88PL815: 1.8V/1.5A; 88PL830: 2.5V/3.0A
- Ultra-low dropout (235mV @ 3A typ.)
- Input voltage range 2.7V to 3.6V
- One resistor sets the output voltage level
- Fixed Soft start ramp with any output capacitor up to 1000µF
- "Hiccup" short circuit protection
- Stable with ceramic output capacitors
- Adjustable 8 level, programmable output voltage in 2% steps
- Logic controlled shutdown
- 0.1µA supply current in shutdown
- Stable with 0A load current
- Lead-free MSOP-8L and QFN-5L packages
- -40°C to +125°C junction temperature range

## Applications

- Adjustable linear regulator for low-voltage digital ICs
- PC add-in cards
- Backup power supplies and 3.3V PCI Express Bus

**Figure 1: Typical LDO Regulator**





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# 1 Signal Description

## 1.1 Pin Configuration

Figure 2: 3x3mm MSOP-8 - Top View

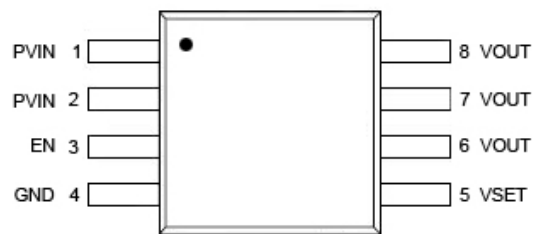


Figure 3: 5x5mm QFN-5 - Top View

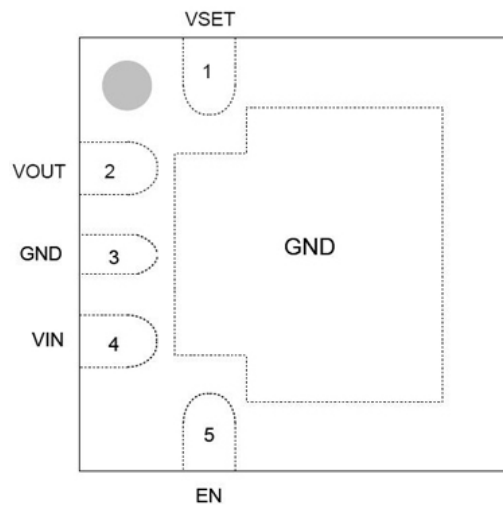


Table 1: Product Table

Product Number	Output Voltage	Output Current
88PL830	2.40, 2.45, 2.50, 2.55, 2.60, 2.65, 2.70, 2.75	3.0A
88PL815	1.728, 1.764, 1.80, 1.836, 1.872, 1.908, 1.944, 1.980	1.5A
88PL810	1.44, 1.47, 1.50, 1.53, 1.56, 1.59, 1.62, 1.65	1.0A

## 1.2 Pin Description

### 1.2.1 Pin Types

This section provides the pin description of the 88PL810/88PL815/88PL830 devices. Table 2 shows the pin types used in Table 3.

**Table 2: Pin Type Definitions**

Pin Type	Definition
I	Input only
O	Output Only
S	Supply
NC	Not Connected
GND	Ground

**Table 3: Pin Description**

5x5 QFN-5 Pin #	3x3 MSOP-8 Pin #	Pin Name	Pin Type	Pin Function
5	1, 2	PVIN	S	Input Voltage: Input voltage supplies current to output. Connect a 10 $\mu$ F decouple capacitor (CIN) between this pin and GND pin.
4	3	EN	I	Enable: CMOS compatible input. Logic low = Disable, Logic high = Enable.
3	4	GND	GND	Ground: Tab is connected to GND.
1	5	VSET		Voltage Setting: Connect to an external resistor that is connected to ground to set the output voltage of the resistor. The total capacitance across this pin and GND should be less than 25pF. Use a resistor with tolerance better than 2%. If this pin is connected to GND, the output voltage will be set to 2.5V. If this pin is PVIN, the output voltage will be set to 3.3V. Do not float this pin.
2	6, 7, 8	VOUT	O	Output Voltage: Adjustable regulator output. A 10 $\mu$ F capacitor is connected between this pin and the GND pin.

# 2 Electrical Specifications

## 2.1 Absolute Maximum Ratings

Table 4: Absolute Maximum Ratings<sup>1</sup>

Parameter	Symbol	Range	Units
Input Voltage to GND	$V_{IN}$	-0.6 to 4.2	V
Enable voltage ( $V_{EN}$ ) to GND	$V_{EN}$	-0.6 to max ( $V_{IN} + 0.6$ , 4.2)	V
Voltage set to GND	$V_{SET}$	-0.6 to max ( $V_{IN} + 0.6$ , 4.2)	V
Output Voltage to GND	$V_{OUT}$	-0.6 to max ( $V_{IN} + 0.6$ , 4.2)	V
Operating Temperature Range <sup>2</sup>	$T_{OP}$	-40 to 85	°C
Storage Temperature Range	$T_{STOR}$	-65 to 150	°C
Maximum Junction Temperature	$T_{JMAX}$	150	°C
ESD Rating <sup>3</sup>		2	kV

1. Exceeding the absolute the maximum rating may damage the device.
2. Specifications over the -40°C to 85°C operating temperature ranges are assured by design, characterization and correlation with statistical process controls.
3. Devices are ESD sensitive. Handling precautions recommended. Human Body model, 1.5k $\Omega$ , in series with 100pF.

## 2.2 Recommended Operating Conditions

Table 5: Recommended Operating Conditions<sup>1</sup>

Parameter	Symbol	Range	Units
Input Voltage	$V_{IN}$	2.7 to 3.6	V
MSOP Package Thermal Resistance	$\theta_{JA}$	150.88	°C/W
5 X 5mm QFN-5L Package Thermal Resistance	$\theta_{JA}$	See Section 5	°C/W
Maximum Operating Junction Temperature	$T_{JMAX}$	125	°C

1. This device is not guaranteed to function outside the specified operating range

## 2.3 Electrical Characteristics

**Table 6: Electrical Characteristics**

**NOTE:** The following table applies unless otherwise noted:  $C_{IN} = 10\mu\text{F}$ ;  $C_{OUT} = 10\mu\text{F}$  (Ceramic);  $I_{OUT} = 10\text{mA}$ ;  $T_A = 25^\circ\text{C}$ ;  $V_{IN} = 3.3\text{V}$ . Bold values indicate  $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ .

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Voltage Range	$V_{IN}$		2.7		3.6	V
Output Voltage Accuracy	$V_{OUT}$	1mA [ IOUT [ 3A (88PL830)	-2		2	%
		1mA [ IOUT [ 1.5A (88PL815)				
		1mA [ IOUT [ 1A (88PL810)				
Output Voltage Load Regulation	$DV_{OUT}/V_{OUT}$	10mA [ IOUT [ 3A (88PL830)		0.1		%
		10mA [ IOUT [ 1.5A (88PL815)				
		10mA [ IOUT [ 1A (88PL810)				
Output Voltage Line Regulation	$DV_{OUT}/V_{OUT}$	$V_{IN} = 3.0\text{V}-3.6\text{V}$ , $I_{OUT} = 10\text{mA}$		0.01		%
Dropout Voltage (88PL830 only)	$V_{IN}-V_{OUT}$	$I_{OUT} = 1\text{A}$ , Output voltage variation=1%		75		mV
		$I_{OUT} = 2\text{A}$ , Output voltage variation=1%		156		mV
		$I_{OUT} = 3\text{A}$ , Output voltage variation=1%		235		mV
Quiescent Current (88PL810)	$I_Q$	$I_{OUT} = 0\text{mA}$		1.0		mA
Quiescent Current (88PL815)				1.2		
Quiescent Current (88PL830)				1.5		
Shutdown Input Current	$I_{SHDN}$	$V_{EN} = \text{GND}$		0.1	50	mA
Output Current Limit (88PL810)	$I_{OUT(LIM)}$	$V_{OUT} = 1.5\text{V}$		3.0		A
Output Current Limit (88PL815)				3.0		
Output Current Limit (88PL830)				7.0		
<b>Enable Input</b>						
Enable Input Logic low	$V_{EN}$	LDO Shutdown			1.1	V
Enable Input Logic high		LDO Enable	2.2			V
Enable Pin Input Current	$I_{EN}$	$V_{EL} = 1.1\text{V}$		1	10	mA
		$V_{EH} = 2.2\text{V}$		1	10	mA
<b>Under Voltage Lockout</b>						
Under Voltage Lockout	$V_{UVLO}$	High threshold (UTH), $V_{IN}$ increasing		2.60	2.70	V
		Low threshold (UTL), $V_{IN}$ increasing		2.45		V
Under Voltage Lockout Hysteresis				150		mV

**Table 6: Electrical Characteristics**

**NOTE:** The following table applies unless otherwise noted:  $C_{IN} = 10\mu\text{F}$ ;  $C_{OUT} = 10\mu\text{F}$  (Ceramic);  $I_{OUT} = 10\text{mA}$ ;  $T_A = 25^\circ\text{C}$ ;  $V_{IN} = 3.3\text{V}$ . Bold values indicate  $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ .

Parameter	Symbol	Condition	Min	Typ	Max	Units
<b>LDO Output Voltage</b>						
Output Voltage (88PL830)		$R_{SET} = 11\text{K}\Omega$	2.352	2.40	2.448	V
		$R_{SET} = 18.7\text{K}\Omega$	2.401	2.45	2.499	V
		$R_{SET} = 31.6\text{k}\Omega$ or $0\Omega$	2.450	2.50	2.550	V
		$R_{SET} = 53.6\text{K}\Omega$	2.499	2.55	2.601	V
		$R_{SET} = 97.6\text{K}\Omega$	2.548	2.60	2.652	V
		$R_{SET} = 165\text{K}\Omega$	2.597	2.65	2.703	V
		$R_{SET} = 280\text{K}\Omega$	2.646	2.70	2.754	V
Output Voltage (88PL815)		$R_{SET} = 11\text{K}\Omega$	1.693	1.728	1.763	V
		$R_{SET} = 18.7\text{K}\Omega$	1.729	1.764	1.799	V
		$R_{SET} = 31.6\text{k}\Omega$ or $0\Omega$	1.764	1.800	1.836	V
		$R_{SET} = 53.6\text{K}\Omega$	1.799	1.836	1.873	V
		$R_{SET} = 97.6\text{K}\Omega$	1.835	1.872	1.909	V
		$R_{SET} = 165\text{K}\Omega$	1.870	1.908	1.946	V
		$R_{SET} = 280\text{K}\Omega$	1.905	1.944	1.983	V
Output Voltage (88PL810)		$R_{SET} = 11\text{K}\Omega$	1.411	1.44	1.469	V
		$R_{SET} = 18.7\text{K}\Omega$	1.441	1.47	1.499	V
		$R_{SET} = 31.6\text{k}\Omega$ or $0\Omega$	1.470	1.50	1.530	V
		$R_{SET} = 53.6\text{K}\Omega$	1.499	1.53	1.561	V
		$R_{SET} = 97.6\text{K}\Omega$	1.529	1.56	1.591	V
		$R_{SET} = 165\text{K}\Omega$	1.558	1.59	1.622	V
		$R_{SET} = 280\text{K}\Omega$	1.588	1.62	1.652	V
	$R_{SET} = 475\text{K}\Omega$	1.617	1.65	1.683	V	
<b>Soft Start</b>						
Start-up Time (88PL830)	$t_{SS}$	$V_{OUT} = 2.5\text{V}$		3		ms
Start-up Time (88PL815)		$V_{OUT} = 1.8\text{V}$		2.2		
Start-up Time (88PL810)		$V_{OUT} = 1.5\text{V}$		2.1		
<b>Low Drop Out Auto-restart</b>						
LDO Auto-restart <sup>1</sup>		Time to restart after current limit shut down		6	30	ms
<b>Over Temperature Protection</b>						
Over-temperature Protection	$T_{OT}$	$T_J$ increasing (Disable IC)		150		$^\circ\text{C}$
		$T_J$ decreasing (Enable IC)		120		$^\circ\text{C}$

1. Specifications over the  $-40\text{C}$  to  $85\text{C}$  operating temperature ranges are assured by design, characterization, and correlation with statistical process controls.

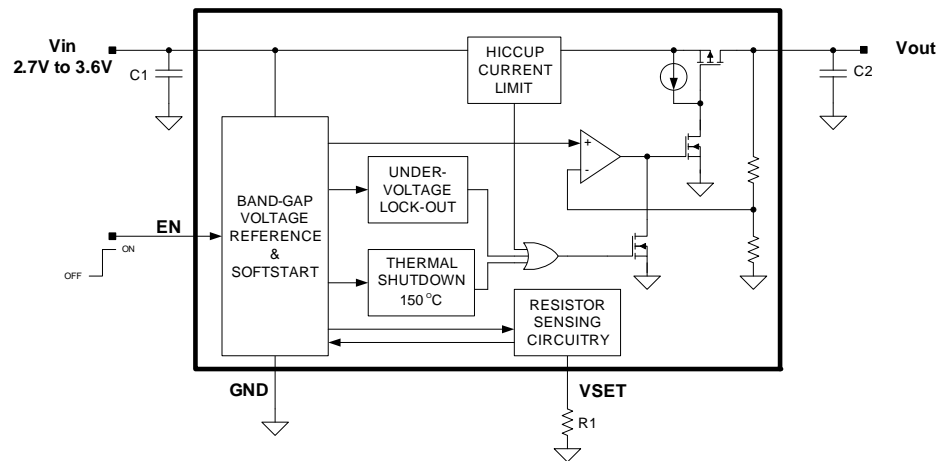


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# 3 Functional Description

Figure 4: 88PL810/88PL815/88PL830 Simplified Block Diagram



### 3.1 Output Voltage – AnyVoltage™ Technology

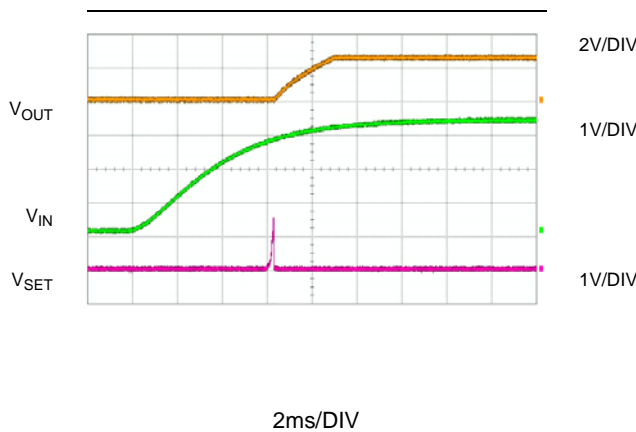
For 88PL830, the output voltage is set by using a single resistor ( $R_{VSET}$ ) to provide eight output voltage options from 2.40V to 2.75V in 50mV steps (See Table 4). The Resistor is only read once during start-up before the output voltage is turned on; therefore, the output voltage cannot be changed on-the-fly. To configure the output to a different voltage either power has to recycle or the enable input has to turn OFF and back ON.

**Table 7: Output Voltage**

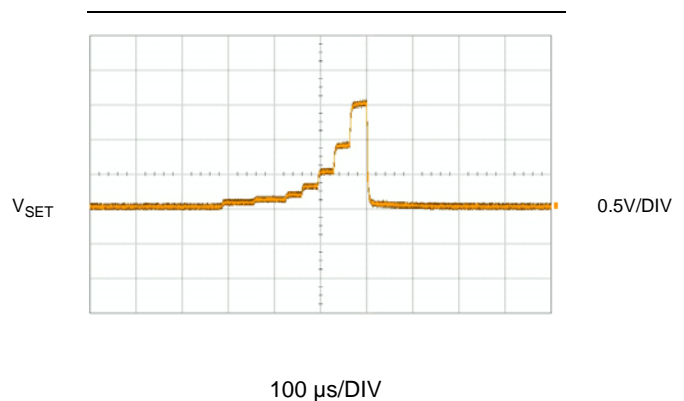
Step	V <sub>OUT</sub> 88PL830 (V)	V <sub>OUT</sub> 88PL815 (V)	V <sub>OUT</sub> 88PL810 (V)	R <sub>VSET</sub> (kΩ)
1	2.50	1.80	1.50	0
2	2.75	1.980	1.65	475
3	2.70	1.944	1.62	280
4	2.65	1.908	1.59	165
5	2.60	1.872	1.56	97.6
6	2.55	1.836	1.53	53.6
7	2.50	1.80	1.50	31.6
8	2.45	1.764	1.47	18.8
9	2.40	1.728	1.44	11

Figure 3 shows the startup sequence of the 88PL830. Once the input voltage ( $V_{IN}$ ) is above the under voltage lockout (UVLO) upper threshold (UTH) of 2.65V, the VSET pin becomes active. Current is sourced out of this pin in exponentially increasing steps. After each step there is a blanking time before the VSET voltage is compared to an internal 1.2V reference. If the VSET voltage is below this reference voltage, the current source proceeds to the next set. Once the VSET voltage is above the reference voltage the sequence stops and the output voltage ( $V_{out}$ ) is allowed to turn-on. Figure 4 shows the  $V_{SET}$  waveform for a 2.5V output. The 88PL830 keeps track of how many steps were required to determine the appropriate output voltage. Table 4 provides the number of steps necessary for each output voltage option. Using a 31.6kΩ resistor requires the current source to step 7 times, see Figure 4.

**Figure 5: Start-Up Sequence**



**Figure 6: VSET Voltage Steps for 2.5V Output**



The 88PL810/88PL815/88PL830 devices provide an innovative technique to set the output voltage. The output voltage is determined during startup by the device reading the value of an external resistor that is located outside the regulator's feedback loop. By placing the output voltage-programming resistor outside the regulator's feedback loop, its tolerance does not affect the accuracy of the output voltage. Normally, adjustable regulators use 1% resistors to set the output voltage. However, these resistors are located inside the feedback loop, introducing as much as 2% of initial accuracy error to the output voltage, resulting in an overall initial accuracy of 3%. The 88PL810/88PL815/88PL830 initial accuracy is 2% for any of the eight output voltages.

The  $V_{SET}$  pin is sensitive to excessive leakage currents and stray capacitance. The output voltage can potentially be programmed to the lower output voltage if there is contamination that introduces excessive leakage current on the  $V_{SET}$  pin, especially for a  $R_{VSET}$  of 475k $\Omega$ . The parasitic resistance on the node must be greater than 3M $\Omega$  and the stray capacitance must be equal to 25pF or less.

## 3.2 Soft Start

Soft start is a highly desirable property in "Hot-Swap" applications. Most LDOs start-up within 100 $\mu$ s, producing large inrush currents on the input power supply. The 88PL810/88PL815/88PL830 device controls the rise time of the output voltage, thereby dramatically reducing the inrush current. The 88PL830 device rise time is typically 3ms and it is independent of output capacitance and load current. Figure 5 shows the rise time with a 10 $\mu$ F output capacitor at 50mA load and Figure 6 shows the rise time with a 1000 $\mu$ F output capacitor at 500mA load. Even with these extreme loading conditions and different inrush current, the output voltage rise time difference is less than 0.1ms. Also note that the output voltage starts at near 0V while other LDO soft start techniques typically start at 1.25V.

Figure 7: Rise Time with  $C_{OUT} = 10\mu F$

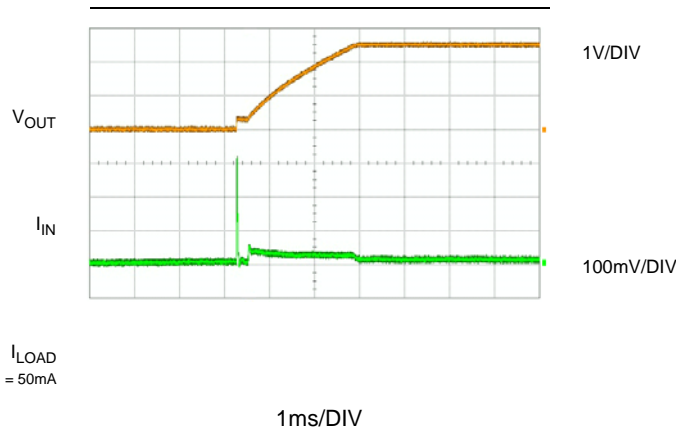
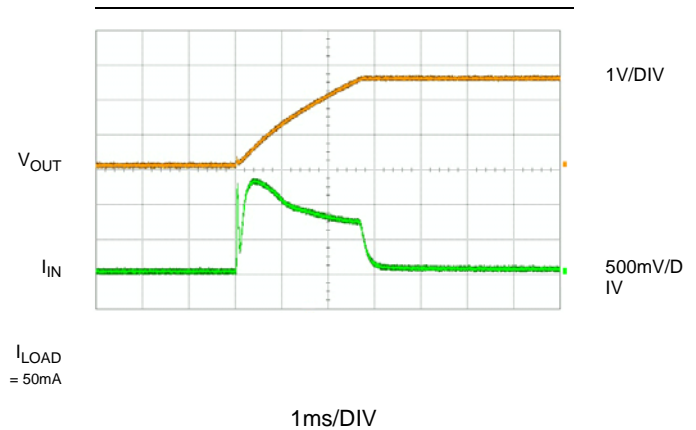


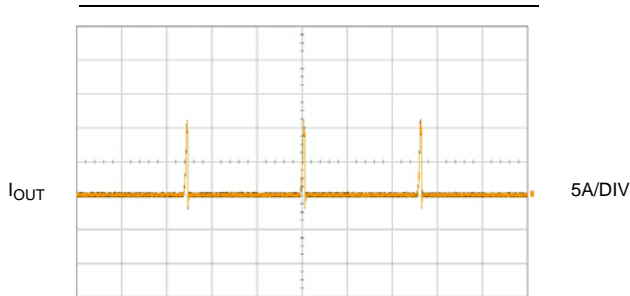
Figure 8: Rise Time with  $C_{OUT} = 1000\mu F$



### 3.3 Hiccup Current Limit

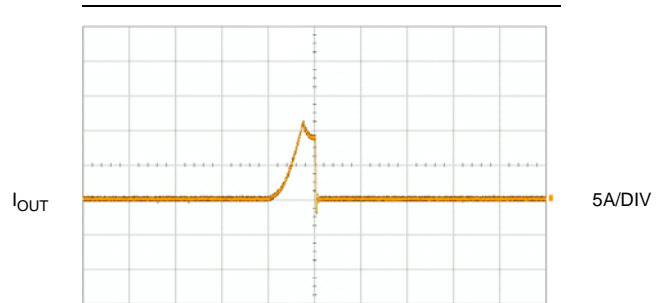
The "Hiccup" short-circuit protection is a feature that is not common among other LDOs. When the current-sense circuit sees an over-current condition, the 88PL810/88PL815/88PL830 device shuts off for about 6ms and then tries to start up again, see Figure 7. If the over-load condition is removed, the 88PL810/88PL815/88PL830 devices will start-up normally; otherwise, the 88PL810/88PL815/88PL830 device will see another over-current event and shut off again, repeating the previous cycle.

**Figure 9: Hiccup Period**



2ms/DIV

**Figure 10: Current Limit Response Time**



200µs/DIV

Hiccup mode protection offers protection against over current situations, since it limits the average current to the load at a low level, reducing power dissipation and case temperature of the IC. The 88PL810/88PL815/88PL830 device case temperature will only rise about 20°C and have a case temperature of around 45°C at room, reducing the thermal stress on the device.

Figure 8 shows the response time of the current limit circuitry. The response time of the protection circuit must be quick enough to prevent damage from overloads, yet allow enough time to respond to transient loads without prematurely tripping the protection circuit.

### 3.4 Output Capacitor (C<sub>OUT</sub>) Selection

The 88PL810/88PL815/88PL830 device requires a 10 $\mu$ F ceramic output capacitor as part of the frequency compensation. However, any other type of capacitor up to 1000 $\mu$ F can be placed in parallel with it as long as the 10 $\mu$ F ceramic output capacitor is placed next to the 88PL810/88PL815/88PL830 device. Additional output capacitance further improves load-transient response and power supply rejection.

X7R and X5R type ceramic capacitors are recommended because of their performance over temperature. Capacitance of the X7R type capacitors changes only 15% over their operating temperature range. Y5V and Z5U type ceramic capacitors change value by as much as 60% and 50%, respectively, over their operating temperature range. If Y5V type ceramic capacitors are used, then higher value capacitor in comparison with X7R and X5R capacitors must be used to ensure a sufficient capacitance value over the operating temperature range. The following capacitors are some of the capacitors recommended to be used with the 88PL810/88PL815/88PL830.

**Table 8: Recommended Capacitors**

Manufacturer	Part Number	Dielectric	Capacitance ( $\mu$ F)	Voltage (V)	Case Size (inch)	Max Height (mm)
Murata	GRM188R60G106M	X5R	10	4.0	0603	0.9
Murata	GRM219R60J106K	X5R	10	6.3	0805	0.95
Murata	GRM21BR60J106K	X5R	10	6.3	0805	1.35
Taiyo-Yuden	CE JMK212BJ106MG-T	X5R	10	6.3	0805	1.40
TDK	C2012X5R0J106MT	X5R	10	6.3	0805	1.55

### 3.5 Input Capacitor

An input capacitor of 1 $\mu$ F or greater is required between the 88PL810/88PL815/88PL830 device's V<sub>IN</sub> pin and ground. It must be placed as close as possible to the 88PL810/88PL815/88PL830 device for stable operation. While 1 $\mu$ F will provide adequate bypassing of the V<sub>IN</sub> supply, larger value input capacitors (10 $\mu$ F) can improve bypassing to handle fast transient response requirements.

### 3.6 Enable

The 88PL810/88PL815/88PL830 devices feature an active high enable (EN) input that allows ON/OFF control of the device. Near "zero" current drain is achieved when the device is disabled, with only microamperes of leakage current flow. The EN input includes TTL/CMOS compatible thresholds for simple interfacing with logic, or that may be directly tied to V<sub>IN</sub> for a constant ON state. The enable input must not be left floating; it must be tied either high or low.

### 3.7 Minimum Load Current

The 88PL810/88PL815/88PL830 device, unlike most other high current regulators, does not require a minimum load to maintain output voltage regulation.

### 3.8 Undervoltage Lockout (UVLO)

The 88PL810/88PL815/88PL830 incorporates undervoltage-lockout circuitry to disable the LDO when the input voltage is below 2.45V (typical). The LDO is enabled when the input voltage is above 2.60V (typical).

### 3.9 Thermal Shutdown

When the junction temperature of the 88PL810/88PL815/88PL830 device exceeds 150°C (typical), the thermal shutdown circuitry disables the LDO. The LDO is enabled when the junction temperature is decreased to 120°C (typical).

## 3.10 Thermal Considerations

The power handling capability of the device is limited by the maximum rated junction temperature (125°C). The power dissipated by the device is made up of two components:

1. Output current multiplied by the differential of input and output voltage:  $(I_{OUT})(V_{IN}-V_{OUT})$ .
2. Input current into the device (used by internal circuitry in mA) multiplied by the input voltage:  $(I_Q)(V_{IN})$

The actual power dissipation ( $P_D$ ) will be the sum of the two components listed above:

$$P_D = (I_{OUT})(V_{IN} - V_{OUT}) + (I_Q)(V_{IN})$$

To determine the maximum power dissipation ( $P_{D(max)}$ ) of the package, use the junction-to-ambient thermal resistance ( $\theta_{JA}$ ) of the device and the following equation:

$$P_{D(max)} = \frac{(T_{J(max)} - T_{A(max)})}{\theta_{JA}}$$

Where  $T_{J(max)}$  is the maximum junction temperature of the die (125°C) and  $T_{A(max)}$  is the ambient operating temperature. Note that  $\theta_{JA}$  is layout dependent.

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the air. Each material in the heat flow between the IC and the outside environment has a thermal resistance. Starting from the die, we have  $\theta_{JC}$  (junction to case),  $\theta_{CS}$  (case to heat sink), and  $\theta_{SA}$  (heat sink to ambient). These thermal resistances are added together to determine the total thermal resistance between the die and the air,  $\theta_{JA}$ .

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

The value for  $\theta_{SA}$  is dependent on the heat sink, where the  $\theta_{CS}$  is dependent on the package type and contact between heat sink and package. The proper heat sink can be selected based on the following equation:

$$\theta_{SA} = \frac{T_{J(max)} - T_{A(max)}}{P_{D(max)}} - (\theta_{JC} + \theta_{CS})$$

The  $\theta_{JA}$  can be calculated after the proper heat sink is selected.

To prevent the device from entering Thermal Shutdown, the actual power dissipation needs to be equal or less than the maximum power dissipation:

$$\frac{T_{J(max)} - T_{A(max)}}{\theta_{JA}} \geq (I_{OUT}) \times (V_{IN} - V_{OUT})$$



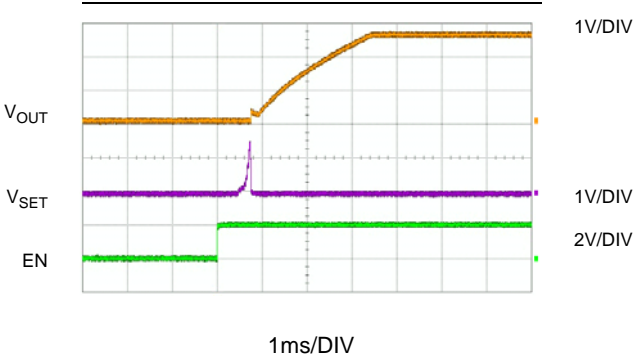
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# 4 Functional Characteristics

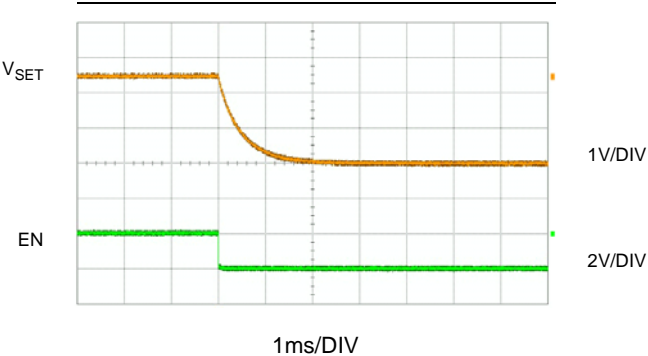
The following is used  $C_{IN} = 10\mu\text{F}$ ;  $C_{OUT} = 10\mu\text{F}$  (Ceramic);  $V_{IN}=3.3\text{V}$ ;  $V_{OUT}=2.5\text{V}$ ; unless otherwise noted.

**Figure 11: Start-Up Using the Enable Pin**



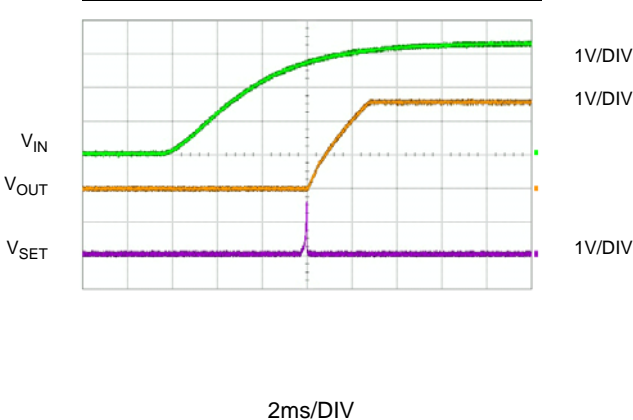
$I_{LOAD} = 50\Omega$

**Figure 12: Turn Off Using the Enable Pin**



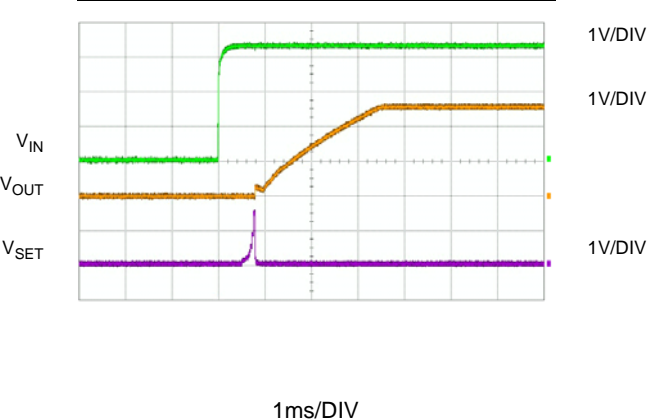
$I_{LOAD} = 50\Omega$

**Figure 13: Input Voltage Soft Start**



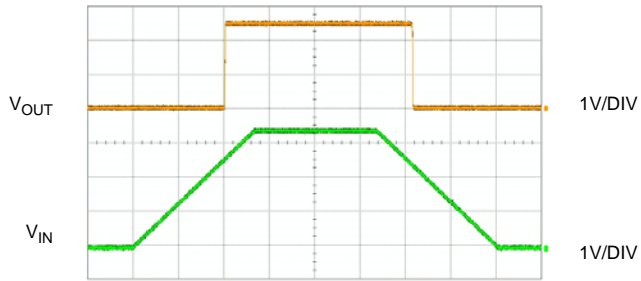
$I_{LOAD} = \text{No Load}$

**Figure 14: Input Voltage Hot Plug**



$I_{LOAD} = \text{No Load}$

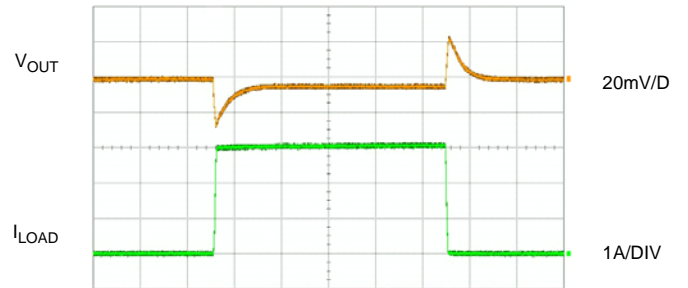
**Figure 15: UVLO Thresholds**



100ms/DIV

$V_{H_{TH}} = 2.60V$   
 $V_{L_{TH}} = 2.45V$

**Figure 16: Load Transient Response**



200  $\mu$ s/DIV

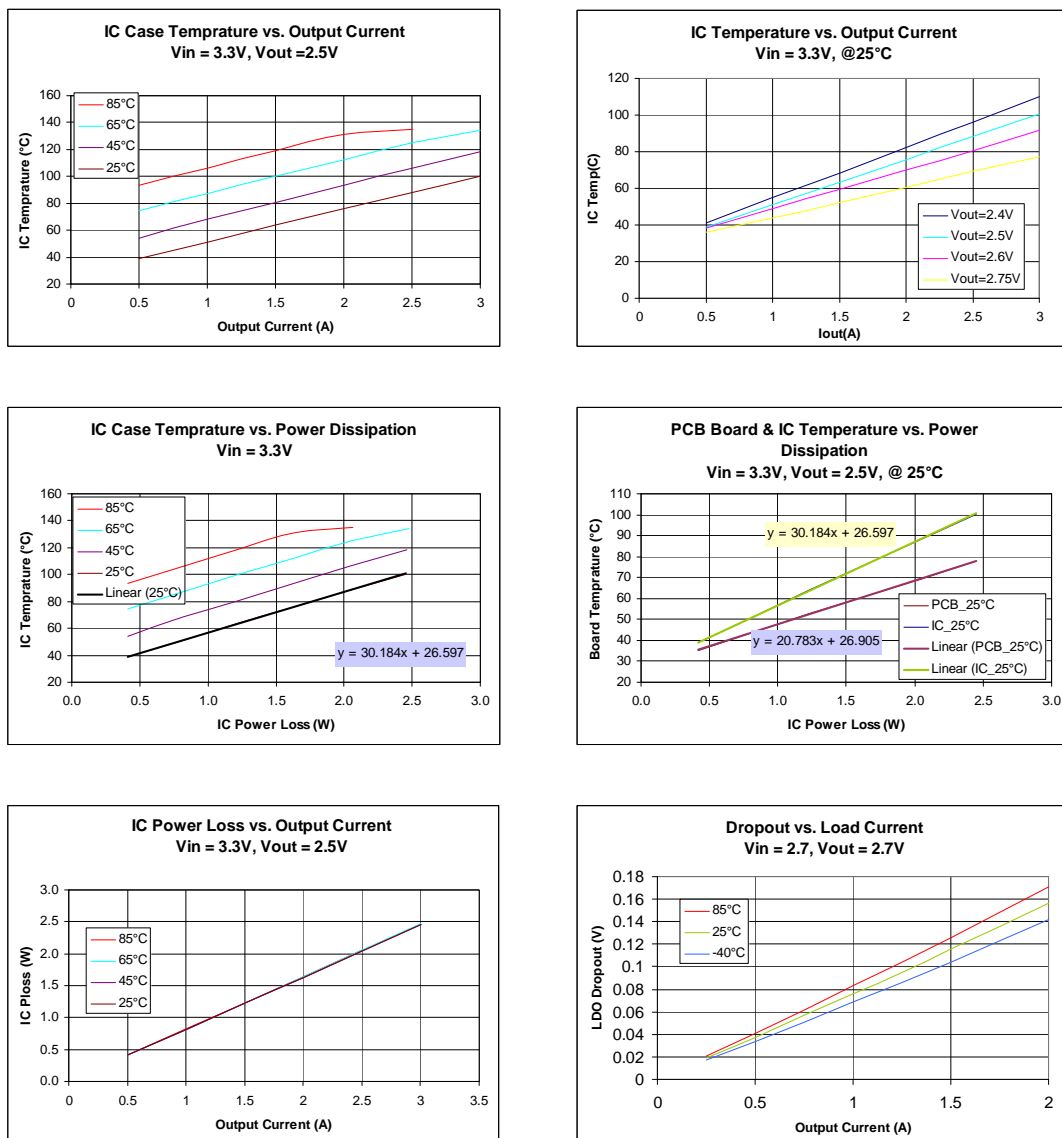
$I_{LOAD} = 0.01A$  to  $3.0A$   
 $C_{OUT} = 10\mu F$

# 5 Typical Characteristics

## 5.1 IC Case and Board Temperature

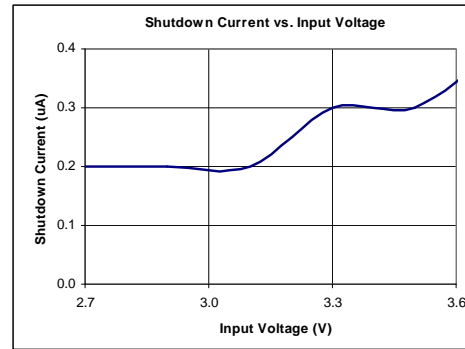
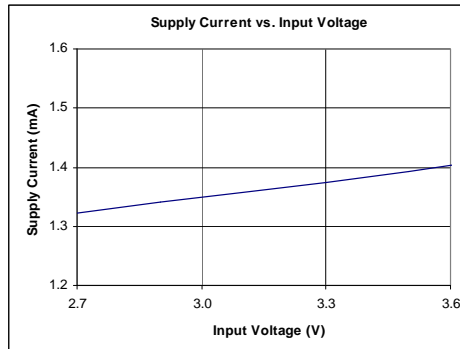
Actual results depend upon the size of the PCB and proximity to other heat emitting components. The following test data used a  $\frac{3}{4}$  in<sup>2</sup> PCB, 1 oz copper, and 88PL830 part.

Figure 17: 5x5mm QFN-5L Package

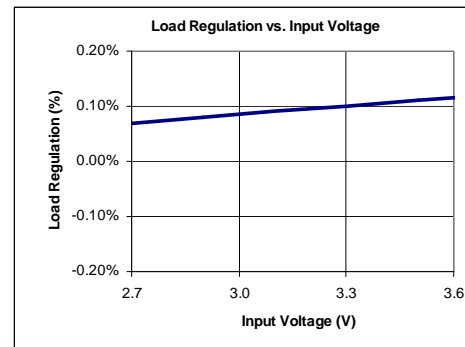
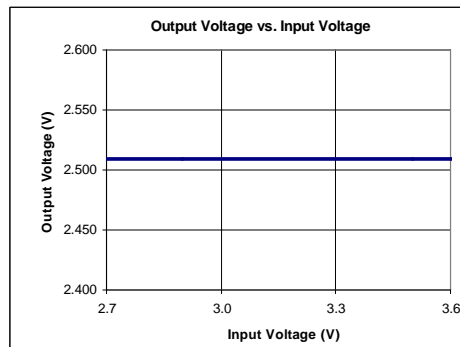


### Figure 18: Input Voltage Graphs

The following data applies to 88PL830;  $C_{IN} = 10\mu\text{F}$ ;  $C_{OUT} = 10\mu\text{F}$  (Ceramic); unless otherwise noted.



Load = No Load



$I_{OUT(LDO)} = 10\text{mA}$

$V_{OUT(LDO)} = 2.5\text{V}$   
 $I_{OUT(LDO)} = 10\text{mA} - 3.0\text{A}$

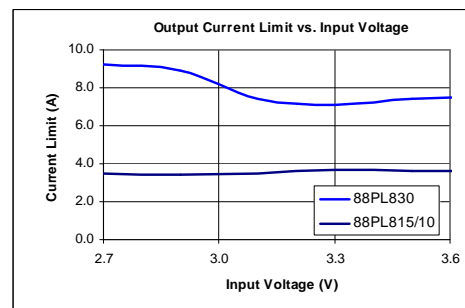
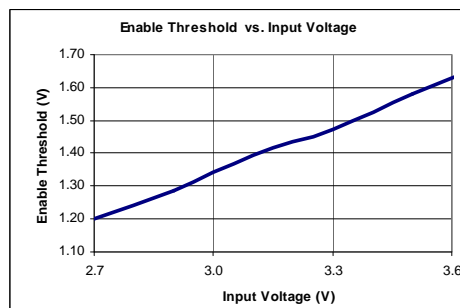
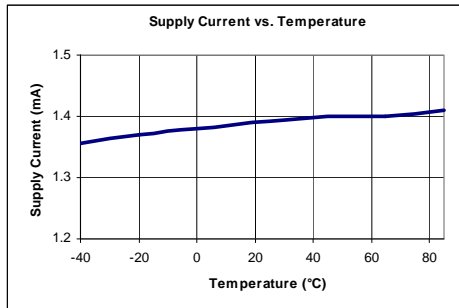
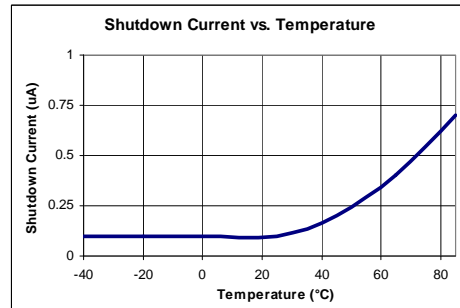


Figure 19: Temperature Graphs

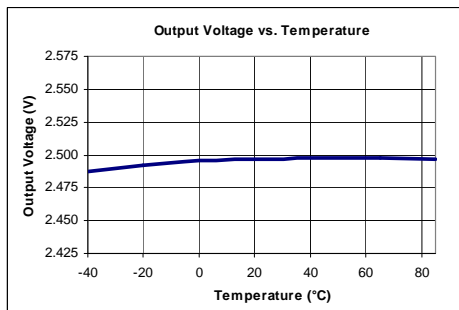
The following data applies to 88PL830;  $C_{IN} = 10\mu\text{F}$ ;  $C_{OUT} = 10\mu\text{F}$  (Ceramic);  $V_{IN}=3.3\text{V}$ ;  $V_{OUT}=2.5\text{V}$ ; unless otherwise noted.



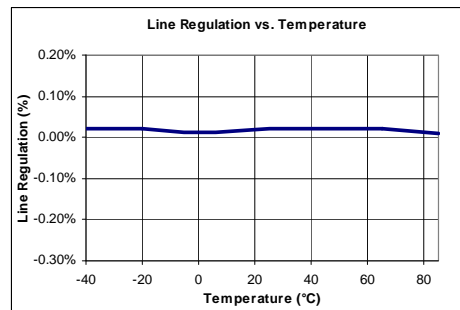
$I_{OUT(LDO)} = \text{No Load}$



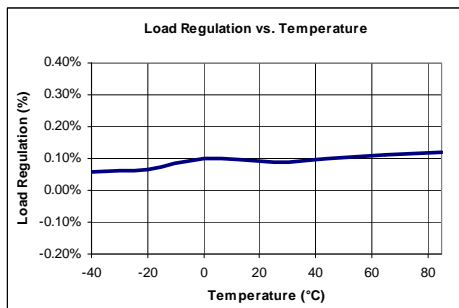
$I_{OUT(LDO)} = 10\text{mA}$



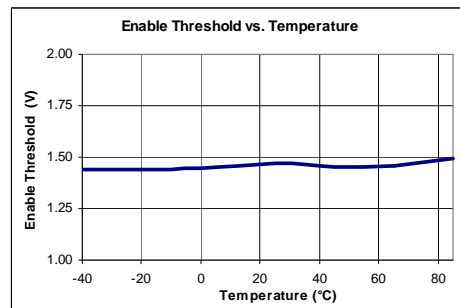
$I_{OUT(LDO)} = 10\text{mA}$



$V_{IN} = 3.0\text{V} - 3.6\text{V}$

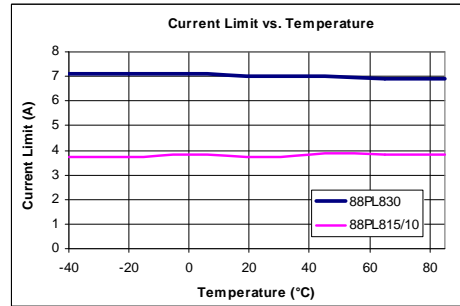
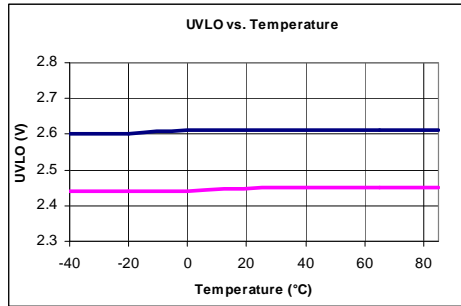


$I_{OUT(LDO)} = 10\text{mA} - 3\text{A}$



**Figure 20: Temperature Graphs (Continued)**

The following data applies to 88PL830;  $C_{IN} = 10\mu\text{F}$ ;  $C_{OUT} = 10\mu\text{F}$  (Ceramic);  $V_{IN}=3.3\text{V}$ ;  $V_{OUT}=2.5\text{V}$ ; unless otherwise noted.



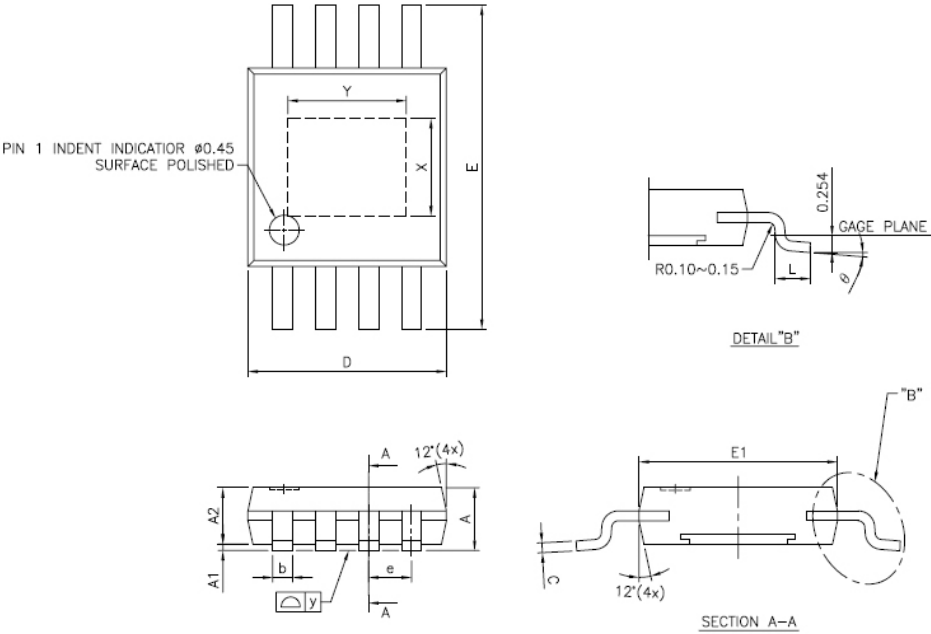
$I_{OUT(LDO)} = 10\text{mA}$

# 6 Mechanical Drawings

## 6.1 Mechanical Dimensions

### 6.1.1 MSOP-8 Package

Figure 21: 88PL810/88PL815/88PL830 MSOP Mechanical Dimensions



**Table 9: MSOP-8L Dimensions**

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A			1.10			0.043
A1	0.05		0.15	0.002		0.006
A2	0.76	0.85	0.95	0.030	0.033	0.037
b	0.25	0.30	0.35	0.010	0.012	0.014
C	0.13	0.15	0.23	0.005	0.006	0.09
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.80	4.90	5.00	0.189	0.193	0.197
E1	2.90	3.00	3.10	0.114	0.118	0.122
e		0.65			0.0256	
L	0.40	0.53	0.66	0.016	0.021	0.026
y			0.10			0.004
θ	0°	3°	6°	0°	3°	6°

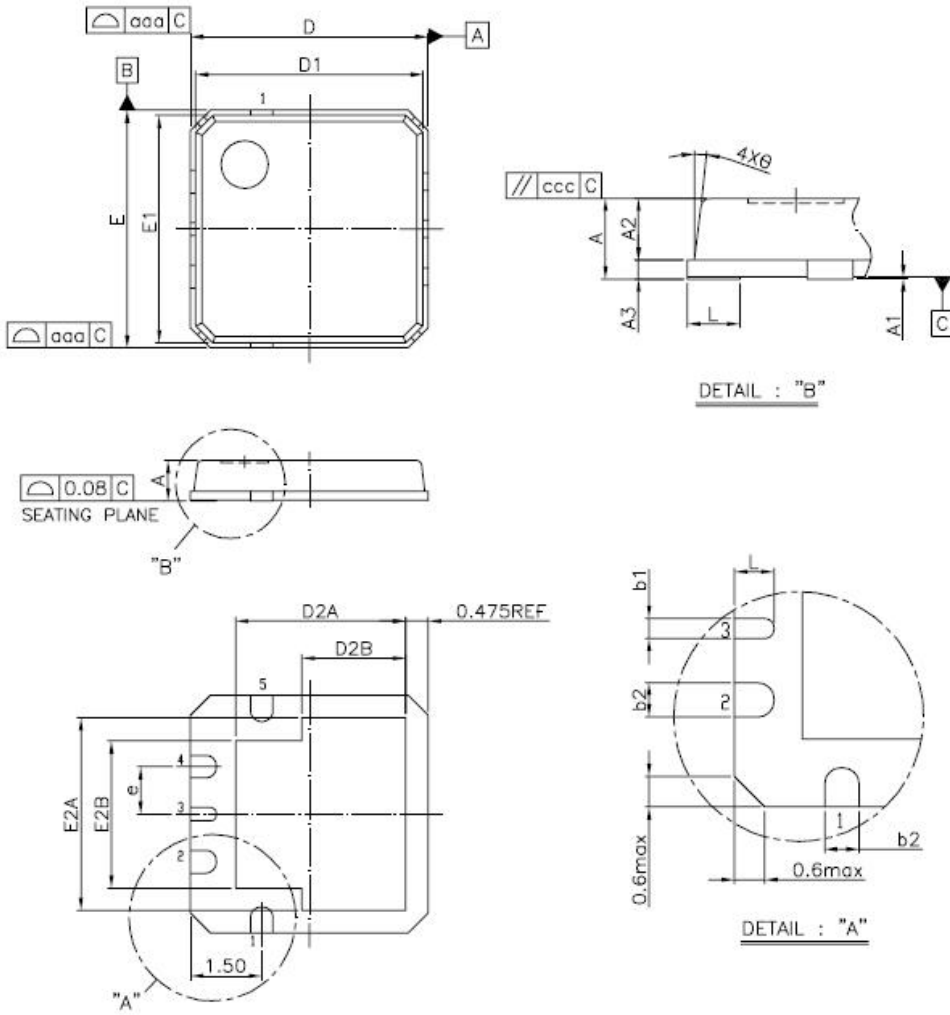
**Notes:**

3. Controlling Dimension: mm
4. Lead Frame Material: OLIN C7025
5. Dimension "D" does not include mold flash, tie bar burrs and gate burrs. Mold flash, tie bar burrs and gate burrs shall not exceed 0.006" [0.15mm] per end. Dimension "E1" does not include interlead flash. Interlead flash shall not exceed 0.010" [0.25mm] per side.
6. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.003" [0.08mm] total in excess of the "b" dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead to be 0.0028" [0.07mm].
7. Tolerance: 60.010" [0.25mm] unless otherwise specified.
8. Otherwise dimensions follow acceptable specifications.



6.1.2 5x5mm QFN-5L Package

Figure 22: 88PL810/88PL815/88PL830 5x5mm QFN-5L Mechanical Dimensions



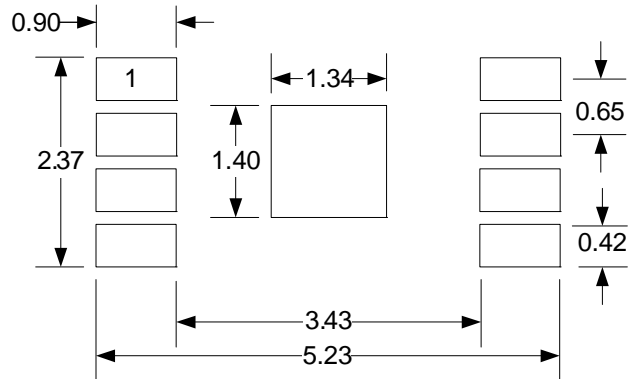
- Notes:
1. Controlling Dimension: Millimeter
  2. Reference Document: JEDEC MO-229

**Table 10: 5x5mm QFN-5L Dimensions**

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
<b>A</b>	0.80	0.85	1.00	0.031	0.033	0.039
<b>A1</b>	0.00	0.02	0.05	0.00	0.001	0.002
<b>A2</b>	0.60	0.65	0.50	0.024	0.026	0.031
<b>A3</b>	0.020 REF			0.008 REF		
<b>b1</b>	0.25	0.30	0.35	0.010	0.012	0.014
<b>B2</b>	0.45	0.50	0.55	0.018	0.020	0.022
<b>D/E</b>	5.00 BSC			0.197 BSC		
<b>D1/E1</b>	4.95 BSC			0.187 BSC		
<b>D2A</b>	3.43	3.58	3.73	0.135	0.141	0.147
<b>D2B</b>	2.03	2.18	2.33	0.080	0.086	0.092
<b>E2A</b>	3.90	4.05	4.20	0.154	0.159	0.165
<b>E2B</b>	2.95	3.10	3.25	0.116	0.122	0.128
<b>e</b>	1.00 BSC			0.039 BSC		
<b>L</b>	0.35	0.55	0.75	0.014	0.022	0.030
<b>K</b>	0.20			0.008		
$\theta$	0°		12°	0°		12°
<b>aaa</b>			0.15			0.006
<b>bbb</b>			0.10			0.004
<b>ccc</b>			0.10			0.004
<b>ddd</b>			0.05			0.002

## 6.2 Typical Pad Layout Dimensions

Figure 23: Recommended Solder Pad Layout for MSOP-8

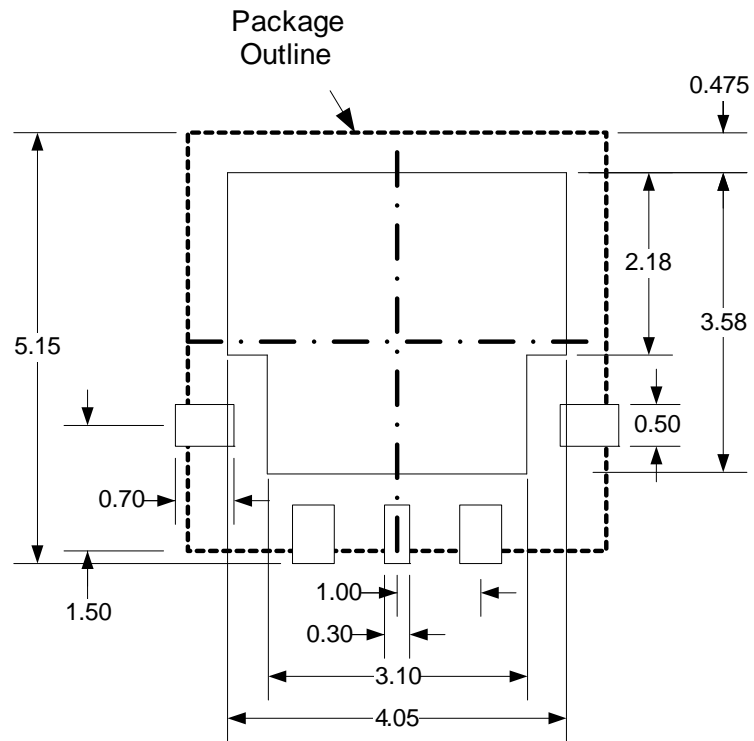


### 3X3 MSOP-8L Land Pattern (mm)

**Notes:**

1. Top View
2. Drawing Not to Scale
3. Dimensions are in millimeters
4. Tolerance  $\pm 0.05\text{mm}$

Figure 24: Recommended Solder Pad Layout for QFN-5



**5X5 QFN-5L  
 Land Pattern (mm)**

**Notes:**

1. Top View
2. Drawing Not to Scale
3. Dimensions are in millimeters
4. Tolerance  $\pm 0.05\text{mm}$



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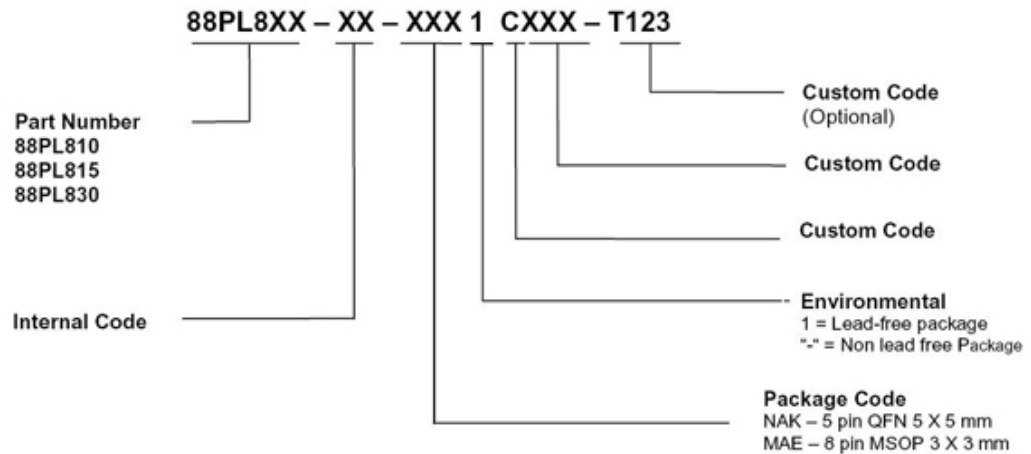


# 7 Ordering Information

## 7.1 Ordering Part Numbers and Package Markings

Figure 11 shows the ordering part numbering scheme of the 88PL810/88PL815/88PL830. For complete information, contact Marvell FAE or sales representative.

Figure 25: Ordering Part Numbers and Package Markings



## 7.2 Sample Ordering Part Number

The standard ordering part numbers for the respective solutions are as follows:

Table 11: Order Samples Table

Part Number	Marking	LDO Output Voltage	LDO Output Current	Ambient Temp Range <sup>1</sup>	Package <sup>2</sup>
88PL810-NAK1	L10	1.5V	1.0A	-40°C to +85°C	5x5 QFN-5
88PL815-NAK1	L15	1.8V	1.5A	-40°C to +85°C	5x5 QFN-5
88PL830-NAK1	L30	2.5V	3.0A	-40°C to +85°C	5x5 QFN-5
88PL810-MAE1	L10	1.5V	1.0A	-40°C to +85°C	3x3 MSOP-8
88PL815-MAE1	L15	1.8V	1.5A	-40°C to +85°C	3x3 MSOP-8
88PL830-MAE1	L30	2.5V	3.0A	-40°C to +85°C	3x3 MSOP-8

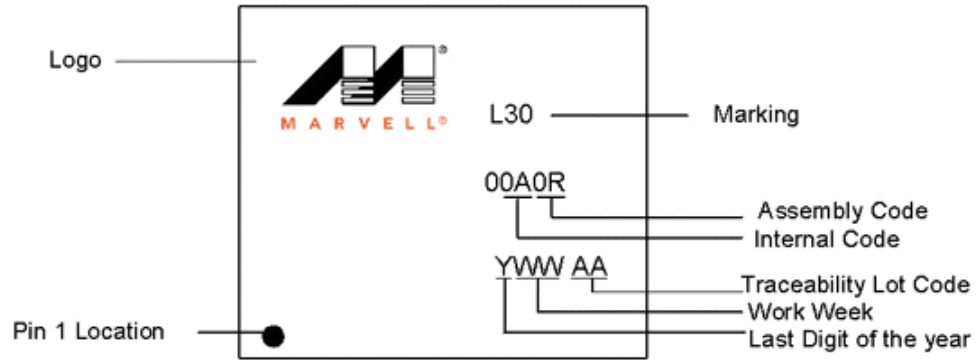
1. Specifications over the -40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.
2. Package dimensions are in millimeters.

## 7.3 Package Markings

Figures 12 and 13 show a typical package marking and pin 1 location for the 88PL810/88PL815/88PL830 part in 5 X 5mm QFN-5 and 3 X 3mm MSOP-8.

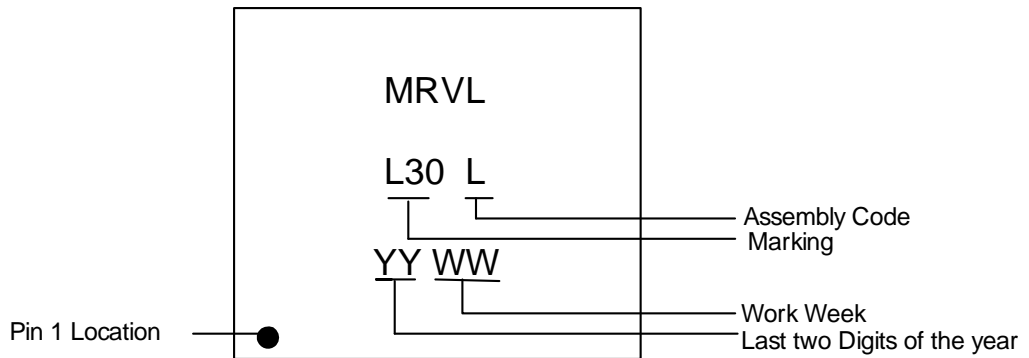
### 7.3.1 5 X 5 QFN-5 Package Marking

Figure 26: Package Marking and Pin 1 Location for 5 X 5mm QFN-5



### 7.3.2 3 X 3 MSOP-8 Package Marking

Figure 27: Package Marking and Pin 1 Location for 3 X 3mm MSOP-8





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# A Revision History

**Table 12: Revision History**

Document Type	Document Revision
Release	Rev. E
<p>Document brought over from MS Word Updated Template Added new MSOP-8 package and removed DPAK package. Changes included: Section 1. Signal Description Section 2. Electrical Specifications Section 6. Mechanical Drawings Section 7. Ordwering Information</p>	



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