Automotive ProASIC3 Flash Family FPGAs

FlashLock

Features and Benefits

High-Temperature AEC-Q100–Qualified Devices
- Grade 2 105°C T_A (115°C T_J)
- Grade 1 125°C T_A (135°C T_J)
- PPAP Documentation

Firm-Error Immune
- Only Automotive FPGAs to Offer Firm-Error Immunity
- Can Be Used without Configuration Upset Risk

High Capacity
- 60 k to 1 M System Gates
- Up to 144 kbits of SRAM
- Up to 300 User I/Os

Reprogrammable Flash Technology
- 130-nm, 7-Layer Metal (6 Copper), Flash-Based CMOS Automotive Process
- Live-at-Power-Up (LAPU) Level 0 Support
- Single-Chip Solution
- Retains Programmed Design when Powered Off

On-Chip User Nonvolatile Memory
- 1 kbit of FlashROM with Synchronous Interface

High Performance
- 350 MHz System Performance
- 3.3 V, 66 MHz 64-Bit PCI

In-System Programming (ISP) and Security
- Secure ISP Using On-Chip 128-Bit Advanced Encryption Standard (AES) Decryption via JTAG (IEEE 1532–compliant)
- FlashLock® to Secure FPGA Contents (anti-tampering)

Low Power
- 1.5 V Core Voltage
- Support for 1.5-V-Only Systems
- Low-Impedance Flash Switches

High-Performance Routing Hierarchy
- Segmented, Hierarchical Routing and Clock Structure
- High-Performance, Low-Skew Global Network
- Architecture Supports Ultra-High Utilization

Advanced I/O
- 700 Mbps DDR, LVDS-Capable I/Os
- 1.5 V, 1.8 V, 2.5 V, and 3.3 V Mixed-Voltage Operation
- Bank-Selectable I/O Voltages—up to 4 Banks per Chip
- Single-Ended I/O Standards: LVTTL, LVCMOS 3.3 V / 2.5 V / 1.8 V / 1.5 V, 3.3 V PCI / 3.3 V PCI-X, and LVCMOS 2.5 V / 5.0 V Input
- Differential I/O Standards: LVPECL, LVDS, B-LVDS, and M-LVDS (A3P250 and A3P1000)
- I/O Registers on Input, Output, and Enable Paths
- Hot-Swappable and Cold-Sparing I/Os
- Programmable Output Slew Rate and Drive Strength
- Weak Pull-Up/-Down
- IEEE 1149.1 (JTAG) Boundary Scan Test
- Pin-Compatible Packages across the Automotive ProASIC®3 Family

Clock Conditioning Circuit (CCC) and PLL
- Six CCC Blocks, One with an Integrated PLL
- Configurable Phase Shift, Multiply/Divide, Delay Capabilities, and External Feedback
- Wide Input Frequency Range (1.5 MHz up to 350 MHz)

SRAMs
- Variable-Aspect-Ratio 4,608-Bit RAM Blocks (×1, ×2, ×4, ×9, and ×18 organizations available)

Automotive ProASIC3 Product Family

ProASIC3 Devices	A3P060	A3P125	A3P250	A3P1000
System Gates	60 k	125 k	250 k	1 M
VersaTiles (D-flip-flops)	1,536	3,072	6,144	24,576
RAM kbits (1,024 bits)	18	36	36	144
4,608-Bit Blocks	4	8	8	32
FlashROM Bits	1 k	1 k	1 k	1 k
Secure (AES) ISP	Yes	Yes	Yes	Yes
Integrated PLL in CCCs	1	1	1	1
VersaNet Globals1	18	18	18	18
I/O Banks	2	2	4	4
Maximum User I/Os	96	133	157	300
Package Pins				
VQFP	VQ100	VQ100	VQ100	
FBGA	FG144	FG144	FG144, FG256	FG144, FG256, FG484
QFN[2]		QNG132	QNG132	

Notes:

1. *Six chip-wide (main) globals and three additional global networks in each quadrant are available.*
2. *QFN packages are available as RoHS compliant only.*

I/Os Per Package

ProASIC3 Devices	A3P060	A3P125	A3P250		A3P1000	
	I/O Type					
Package	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O [2]	Differential I/O Pairs	Single-Ended I/O [2]	Differential I/O Pairs
VQ100	71	71	68	13	–	–
FG144	96	97	97	24	97	25
FG256	–	–	157	38	177	44
FG484	–	–	–	–	300	74
QNG132	–	84	87	19	–	–

Notes:

1. *When considering migrating your design to a lower- or higher-density device, refer to the ProASIC3 Flash Family FPGAs handbook to ensure complying with design and board migration requirements.*
2. *Each used differential I/O pair reduces the number of available single-ended I/Os by two.*
3. *FG256 and FG484 are footprint-compatible packages.*

Automotive ProASIC3 Ordering Information

A3P1000 – 1 FG G 144 T

T – Application (Temperature Range)
T = Grade 2 and Grade 1 AECQ100
Grade 2 = 105°C T_A and 115°C T_J
Grade 1 = 125°C T_A and 135°C T_J

144 – Package Lead Count

G – Lead-Free Packaging
Blank = Standard Packaging
G = RoHS-Compliant (Green) Packaging

FG – Package Type
VQ = Very Thin Quad Flat Pack (0.5 mm pitch)
FG = Fine Pitch Ball Grid Array (1.0 mm pitch)
QN = Quad Flat Pack (0.5 mm pitch)

1 – Speed Grade
Blank = Standard
1 = 15% Faster than Standard

A3P1000 – Part Number
Automotive ProASIC3 Devices
A3P060 = 60,000 System Gates
A3P125 = 125,000 System Gates
A3P250 = 250,000 System Gates
A3P1000 = 1,000,000 System Gates

Note: Minimum order quantities apply. Contact your local Actel sales office for details.

Temperature Grade Offerings

Package	A3P060	A3P125	A3P250	A3P1000
VQ100	C, I, T	C, I, T	C, I, T	–
FG144	C, I, T	C, I, T	C, I, T	C, I, T
FG256	–	–	C, I, T	C, I, T
FG484	–	–	–	C, I, T
QNG132	–	C, I, T	C, I, T	–

Notes:

1. *C = Commercial temperature range: 0°C to 70°C*
2. *I = Industrial temperature range: –40°C to 85°C*
3. *T = Automotive temperature range: Grade 2 and Grade 1 AEC-Q100*
   Grade 2 = 105°C T_A and 115°C T_J
   Grade 1 = 125°C T_A and 135°C T_J
4. *Specifications for Commercial and Industrial grade devices can be found in the ProASIC3 Flash Family FPGAs handbook.*

Speed Grade and Temperature Grade Matrix

Temperature Grade	Std.	–1
T (Grade 1 and Grade 2), Commercial, Industrial	✓	✓

Notes:

1. *T = Automotive temperature range: Grade 2 and Grade 1 AEC-Q100*
   Grade 2 = 105°C T_A and 115°C T_J
   Grade 1 = 125°C T_A and 135°C T_J
2. *Specifications for Commercial and Industrial grade devices can be found in the ProASIC3 Flash Family FPGAs handbook.*

Contact your local Actel representative for device availability:
http://www.actel.com/contact/default.aspx.

1 – Automotive ProASIC3 Device Family Overview

General Description

Automotive ProASIC3 nonvolatile flash technology gives automotive system designers the advantage of a secure, low-power, single-chip solution that is live at power-up (LAPU). Automotive ProASIC3 is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost. These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

Automotive ProASIC3 devices offer 1 kbit of on-chip, reprogrammable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on an integrated phase-locked loop (PLL). Automotive ProASIC3 devices have up to 1 million system gates, supported with up to 144 kbits of SRAM and up to 300 user I/Os.

Automotive ProASIC3 devices are the only firm-error-immune automotive grade FPGAs. Firm-error immunity makes them ideally suited for demanding applications in powertrain, safety, and telematics-based subsystems, where firm-error failure is not an option.

Firm errors in SRAM-based FPGAs can result in high defect levels in field-deployed systems. These unavoidable defects must be considered separately from standard defects and failure mechanisms when looking at overall system quality and reliability.

Flash Advantages

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, flash-based Automotive ProASIC3 devices allow all functionality to be live at power-up; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Flash-based FPGAs are LAPU Class 0 devices, offering the lowest available power in a single-chip device and providing firm-error immunity. The Automotive ProASIC3 family device architecture mitigates the need for ASIC migration at high user volumes. This makes the Automotive ProASIC3 family a cost-effective ASIC replacement solution, especially for automotive applications.

Security

The nonvolatile, flash-based Automotive ProASIC3 devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. Automotive ProASIC3 devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

Automotive ProASIC3 devices utilize a 128-bit flash-based lock and a separate AES key to secure programmed intellectual property and configuration data. In addition, all FlashROM data in Automotive ProASIC3 devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. The AES was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. Automotive ProASIC3 devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. Automotive ProASIC3 devices with AES-based security allow for secure, remote field updates over public networks such as the Internet, and ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves. The contents of a programmed Automotive ProASIC3 device cannot be read back, although secure design verification is possible. Additionally, security features of Automotive ProASIC3 devices provide anti-tampering protection.

Security, built into the FPGA fabric, is an inherent component of the Automotive ProASIC3 family. The flash cells are located beneath seven metal layers, and many device design and layout

techniques have been used to make invasive attacks extremely difficult. The Automotive ProASIC3 family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected and secure. An Automotive ProASIC3 device provides the most impenetrable security for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based Automotive ProASIC3 FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

Live at Power-Up

The Actel flash-based Automotive ProASIC3 devices support Level 0 of the LAPU classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The LAPU feature of flash-based Automotive ProASIC3 devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and external clock generation PLLs. In addition, glitches and brownouts in system power will not corrupt the Automotive ProASIC3 device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based Automotive ProASIC3 devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

Firm-Error Immunity

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of Automotive ProASIC3 flash-based FPGAs. Once it is programmed, the flash cell configuration element of Automotive ProASIC3 FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Low Power

Flash-based Automotive ProASIC3 devices exhibit very low power characteristics, similar to those of an ASIC, making them an ideal choice for power-sensitive applications. Automotive ProASIC3 devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

Automotive ProASIC3 devices also have low dynamic power consumption to further maximize power savings.

Advanced Flash Technology

The Automotive ProASIC3 family offers many benefits, including nonvolatility and reprogrammability, through an advanced flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

Advanced Architecture

The proprietary Automotive ProASIC3 architecture provides granularity comparable to standard-cell ASICs. The Automotive ProASIC3 device consists of five distinct and programmable architectural features (Figure 1-1 on page 1-4 and Figure 1-2 on page 1-4):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM memory
- Extensive CCCs and PLLs
- Advanced I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the Automotive ProASIC3 core tile as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the Actel ProASIC family of third-generation-architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of Automotive ProASIC3 devices via an IEEE 1532 JTAG interface.

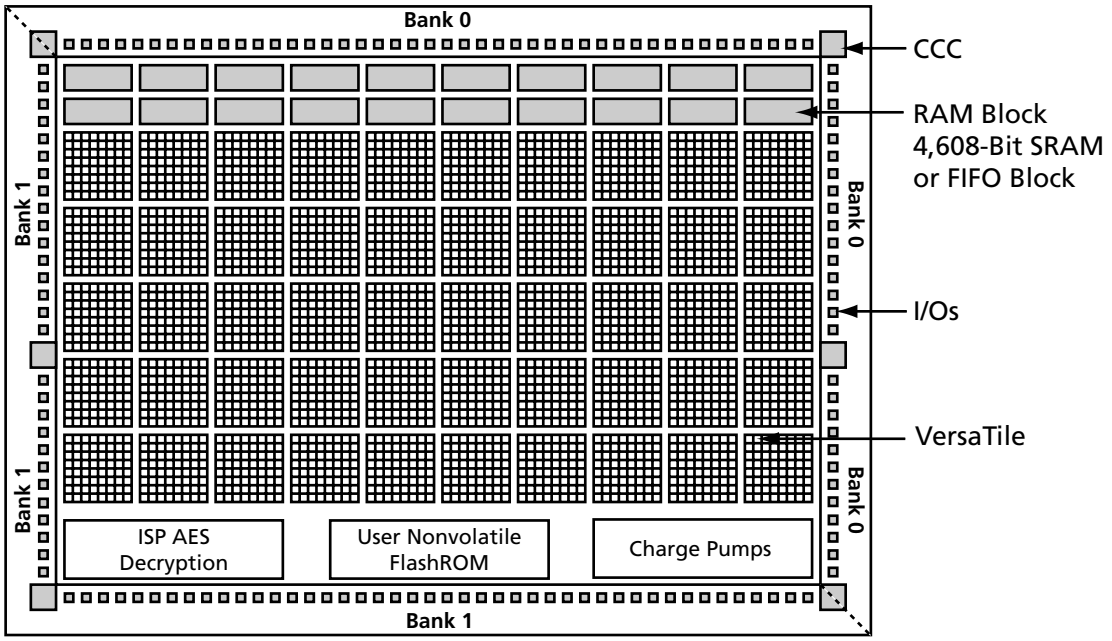

Figure 1-1 • **Automotive ProASIC3 Device Architecture Overview with Two I/O Banks (A3P060 and A3P125)**

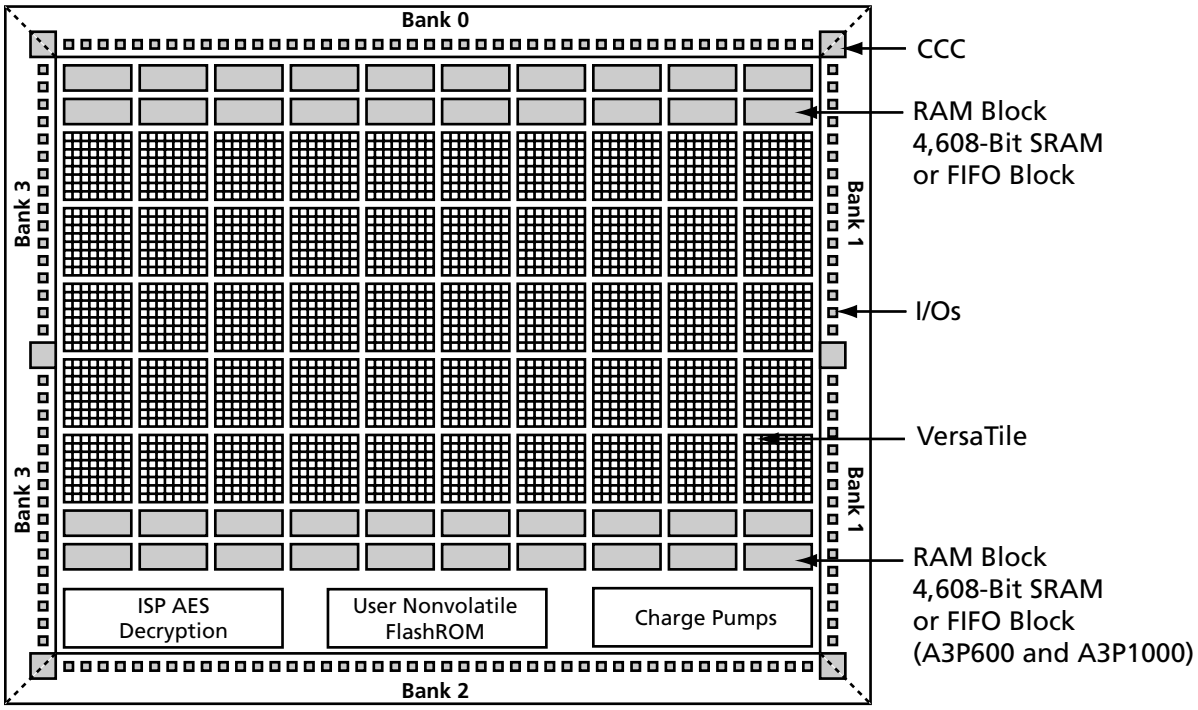

Figure 1-2 • **Automotive ProASIC3 Device Architecture Overview with Four I/O Banks (A3P600 and A3P1000)**

VersaTiles

The Automotive ProASIC3 core consists of VersaTiles, which have been enhanced beyond the ProASIC[PLUS]® core tiles. The Automotive ProASIC3 VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to Figure 1-3 for VersaTile configurations.

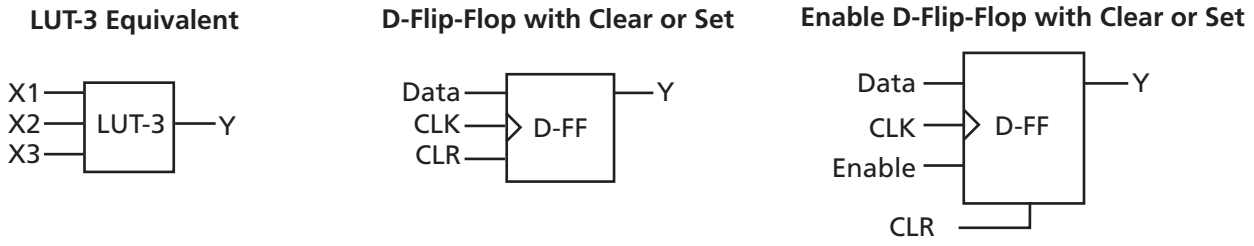

Figure 1-3 • **VersaTile Configurations**

User Nonvolatile FlashROM

Actel Automotive ProASIC3 devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Unique protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, infotainment systems)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard Automotive ProASIC3 IEEE 1532 JTAG programming interface.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The Actel Automotive ProASIC3 development software solutions, Libero® Integrated Design Environment (IDE) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Actel Libero IDE and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM

Automotive ProASIC3 devices have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro.

PLL and CCC

Automotive ProASIC3 devices provide designers with very flexible clock conditioning circuit (CCC) capabilities. Each member of the Automotive ProASIC3 family contains six CCCs. One CCC (center west side) has a PLL.

The six CCC blocks are located at the four corners and the centers of the east and west sides. One CCC (center west side) has a PLL.

All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has these key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz to 350 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz to 350 MHz
- Clock delay adjustment via programmable and fixed delays from –7.56 ns to +11.12 ns
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis (for PLL only)

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration (for PLL only).
- Output duty cycle = 50% ± 1.5% or better (for PLL only)
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used (for PLL only)
- Maximum acquisition time is 300 µs (for PLL only)
- Low power consumption of 5 mW
- Exceptional tolerance to input period jitter— allowable input jitter is up to 1.5 ns (for PLL only)
- Four precise phases; maximum misalignment between adjacent phases of 40 ps × 350 MHz / f_{OUT_CCC} (for PLL only)

Global Clocking

Automotive ProASIC3 devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

I/Os with Advanced I/O Standards

The Automotive ProASIC3 family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). Automotive ProASIC3 FPGAs support many different I/O standards—single-ended and differential.

The I/Os are organized into banks, with two or four banks per device. The configuration of these banks determines the I/O standards supported.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-Data-Rate applications
- Double-Data-Rate applications—DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications

Automotive ProASIC3 banks for the A3P250 and A3P1000 devices support LVPECL, LVDS, B-LVDS, and M-LVDS. B-LVDS and M-LVDS can support up to 20 loads.

Part Number and Revision Date

Part Number 51700099-001-1

Revised December 2009

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (v2.0)	Page
v1.0 (January 2008)	The QNG132 package was added to the "Automotive ProASIC3 Product Family" table, "I/Os Per Package" table, "Automotive ProASIC3 Ordering Information", and "Temperature Grade Offerings".	I – III

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advance," "Preliminary," and "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Unmarked (production)

This version contains information that is considered to be final.

Export Administration Regulations (EAR)

The products described in this document are subject to the Export Administration Regulations (EAR). They could require an approved export license prior to export from the United States. An export includes release of product or disclosure of technology to a foreign national inside or outside the United States.

Actel Safety Critical, Life Support, and High-Reliability Applications Policy

The Actel products described in this advance status document may not have completed Actel's qualification process. Actel may amend or enhance products during the product introduction and qualification process, resulting in changes in device functionality or performance. It is the responsibility of each customer to ensure the fitness of any Actel product (but especially a new product) for a particular purpose, including appropriateness for safety-critical, life-support, and other high-reliability applications. Consult Actel's Terms and Conditions for specific liability exclusions relating to life-support applications. A reliability report covering all of Actel's products is available on the Actel website at http://www.actel.com/documents/ORT_Report.pdf. Actel also offers a variety of enhanced qualification and lot acceptance screening procedures. Contact your local Actel sales office for additional reliability information.

Actel is the leader in low-power and mixed-signal FPGAs and offers the most comprehensive portfolio of system and power management solutions. Power Matters. Learn more at www.actel.com.

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