Microprocessor-Compatible 12-Bit D/A Converter

AD667

1.0 SCOPE

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein.

The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification. http://www.analog.com/aerospace

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at www.analog.com/AD667

2.0 Part Number. The complete part number(s) of this specification follow:

Part Number	Description
AD667-703F	Microprocessor-Compatible 12-Bit D/A Converter
AD667-703D	Microprocessor-Compatible 12-Bit D/A Converter
AD667-713D	Radiation Tested, Microprocessor-Compatible 12-Bit D/A Converter
AD667-713F	Radiation Tested, Microprocessor-Compatible 12-Bit D/A Converter

2.1 Case Outline.

Letter	Descriptive designator [1]	Case Outline (Lead Finish per MIL-PRF-38535)
D	CDIP2-T28	28-Lead ceramic dual-in-line package (SIDEBRAZED)
F	CDFP3-F28	28-Lead bottom-brazed flatpack

[1] See MIL-STD-1835

3.0 Absolute Maximum Ratings. (T_A = 25°C, unless otherwise noted)

V_{CC} to power ground.....0 to +18V
V_{EE} to power ground .....0 to -18V
Digital inputs (pins 11-15, 17-28) to power ground.....-1.0V to +7.0V
Reference in to Reference ground.....±12V
Bipolar offset to reference ground ..... ±12V
10V span R to reference ground..... ±12V
20V span R to reference ground..... ±24V
REF_{OUT}, V_{OUT} (Pins 6, 9)..... Indefinite short to power ground
..... Momentary short to V_{CC}
Power dissipation 1000mW
Storage temperature range.....-65° to +150°C
Lead temperature range (Soldering, 10sec).....+300°C

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3.1 Thermal Characteristics:

Thermal Resistance, Sidebrazed (D) Package

Junction-to-Case (Θ_{JC}) = 25°C/W Max 22 for F

Junction-to-Ambient (Θ_{JA}) = 60°C/W Max 60 for F

PACKAGE PIN	FUNCTION
1	20V SPAN
2	10V SPAN
3	SUM JCT
4	BIP OFF
5	AGND
6	VREF OUT
7	VREF IN
8	+VCC
9	VOUT
10	-VEE
11	CS
12	A3
13	A2
14	A1
15	A0
16	POWER GROUND
17	DB0 LSB
18	DB1
19	DB2
20	DB3
21	DB4
22	DB5
23	DB6
24	DB7
25	DB8
26	DB9
27	DB10
28	DB11 MSB

Figure 1 - Terminal connections.

4.0 Electrical Table: See notes at end of table

Table I

Parameter	Symbol	Conditions 1/	Sub-group	Limit Min	Limit Max	Units
Resolution	RES			12		Bits
Relative accuracy Integral linearity error	RA LE	All bits with positive errors on & All bits with negative errors on.	1		±½	LSB
			2, 3		±¾	
Differential nonlinearity Differential linearity error	DNL DLE	Major carry errors	1		±¾	
			2, 3		±1	
Gain Error 2/	A_E	All bits on All bits high	1		0.20	%FSR
Gain temperature coefficient	TCA_E		2, 3		30	ppm/°C
Unipolar offset error	V_{OS}	All bits off All bits low	1		±2	LSB
Unipolar offset temperature coefficient	TCV_{OS}		2, 3		±3	ppm/°C
Bipolar zero error 2/	B_{PZE}	MSB on, all other bits off	1		±0.10	%FSR
B_{PZE} Temperature coefficient	TCB_{PZE}		2, 3		±10	ppm/°C
Reference output voltage	V_{REF}	Bipolar mode, V_S = ±11.4V, 0.1mA external load	1, 2, 3	9.9	10.1	V
Latch functionality	$A_{E\Delta}$	4/ 5/	1,2,3		±1	LSB
Latch functionality	$V_{OS\Delta}$	4/	1,2,3		±1	
Power supply rejection ratio	PSRR	All bits on +11.4V ≤ V_{CC} ≤ +16.5V	1		10	ppm of FSR/%
		All bits on; -11.4V ≥ V_{EE} ≥ -16.5V	1		10	
Power supply current	I_{CC}	V_S = ± 16.5V, All bits on	1		12	mA
	I_{EE}		1		25	
Digital input high voltage	V_{IH}		1,2,3	2.0		V
Digital input low voltage	V_{IL}		1		0.8	
			2,3		0.7	
Digital input high current	I_{IH}	V_{IH} = 5.5V	1		10	µA
Digital input low current	I_{IL}	V_{IL} = 0.0V	1		5	

TABLE I NOTES:

1/ V_{CC} = +15V, V_{EE} = -15V, 50Ω resistor pin 6 to pin 7, A0, A1, A2, A3, CS = Logic "0", V_{IH} = 2.0V, V_{IL} = 0.8V, Unipolar configuration unless otherwise specified. Unipolar configuration - Pins 1 and 2 to Pin 9, Pin 4 to Pin 4. Bipolar configuration - Pin 1 to Pin 9, 50Ω resistor Pin 4 to Pin 6.

2/ Adjustable to 0

3/ In subgroup 1, the reference output is loaded with 0.5mA nominal reference current, 1.0mA bipolar offset current and 0.1mA additional current. In subgroups 2 and 3, only the 0.5mA reference input current is applied. The reference must be buffered to supply external loads at elevated temperatures.

4/ All bits low, A0, A1, A2, A3, LOGIC "0"; A0, A1, A2, A3 initialized to Logic "1", each 4-bit register set to LOGIC "1", and A0, A1, A2 set sequentially to LOGIC "0" and back to LOGIC "1" to latch data into first rank.

5/ A3 set to LOGIC "0" and back to LOGIC "1" to latch full-scale output into second rank.

6/ See figure 1 and Table 2.

4.1 Electrical Test Requirements:

Table II	
Test Requirements	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1
Final Electrical Parameters	1, 2, 3 1/ 2/
Group A Test Requirements	1, 2, 3
Group C end-point electrical parameters	1 2/
Group D end-point electrical parameters	1
Group E end-point electrical parameters	1

1/ PDA applies to subgroup 1 only. Deltas excluded from PDA.
2/ See table III for deltas.

4.2 Table III. Burn-in test delta limits.

Table III			
TEST TITLE	ENDPOINT LIMIT	DELTA LIMIT	UNITS
V_{OS}	±2	±1	LSB
B_{PZE}	±0.1	±0.05	%FS
I_{CC}	12	1.2	mA
I_{EE}	25	2.5	mA

5.0 Life Test/Burn-In Circuit:

5.1 HTRB is not applicable for this drawing.
5.2 Burn-in is per MIL-STD-883 Method 1015 test condition B.
5.3 Steady state life test is per MIL-STD-883 Method 1005.

Rev	Description of Change	Date
A	Initiate	5-Jun-00
B	Update web address	6-Feb-2002
C	Update web address. Remove burn-in and rad bias circuits	15-May-03
D	Update header/footer and add to 1.0 Scope description.	March 11, 2008