Wideband Synthesizer with Integrated VCO

Preliminary Technical Data

ADF4351

FEATURES

Output frequency range: 35 MHz to 4400 MHz
Fractional-N synthesizer and integer-N synthesizer
Low phase noise VCO
Programmable divide-by-1/-2/-4/-8/-16/-32/-64 output
Typical rms jitter: 0.3 ps rms
Typical EVM at 2.1 GHz: 0.4%
Power supply: 3.0 V to 3.6 V
Logic compatibility: 1.8 V
Programmable dual-modulus prescaler of 4/5 or 8/9
Programmable output power level
RF output mute function
3-wire serial interface
Analog and digital lock detect
Switched bandwidth fast-lock mode
Cycle slip reduction

APPLICATIONS

Wireless infrastructure (W-CDMA, TD-SCDMA, WiMAX, GSM, PCS, DCS, DECT)
Test equipment
Wireless LANs, CATV equipment
Clock generation

GENERAL DESCRIPTION

The ADF4351 allows implementation of fractional-N or integer-N phase-locked loop (PLL) frequency synthesizers if used with an external loop filter and external reference frequency.

The ADF4351 has an integrated voltage controlled oscillator (VCO) with a fundamental output frequency ranging from 2200 MHz to 4400 MHz. In addition, divide-by-1/2/4/8/16/32 or 64 circuits allow the user to generate RF output frequencies as low as 35 MHz. For applications that require isolation, the RF output stage can be muted. The mute function is both pin- and software-controllable. An auxiliary RF output is also available, which can be powered down if not in use.

Control of all the on-chip registers is through a simple 3-wire interface. The device operates with a power supply ranging from 3.0 V to 3.6 V and can be powered down when not in use.

FUNCTIONAL BLOCK DIAGRAM

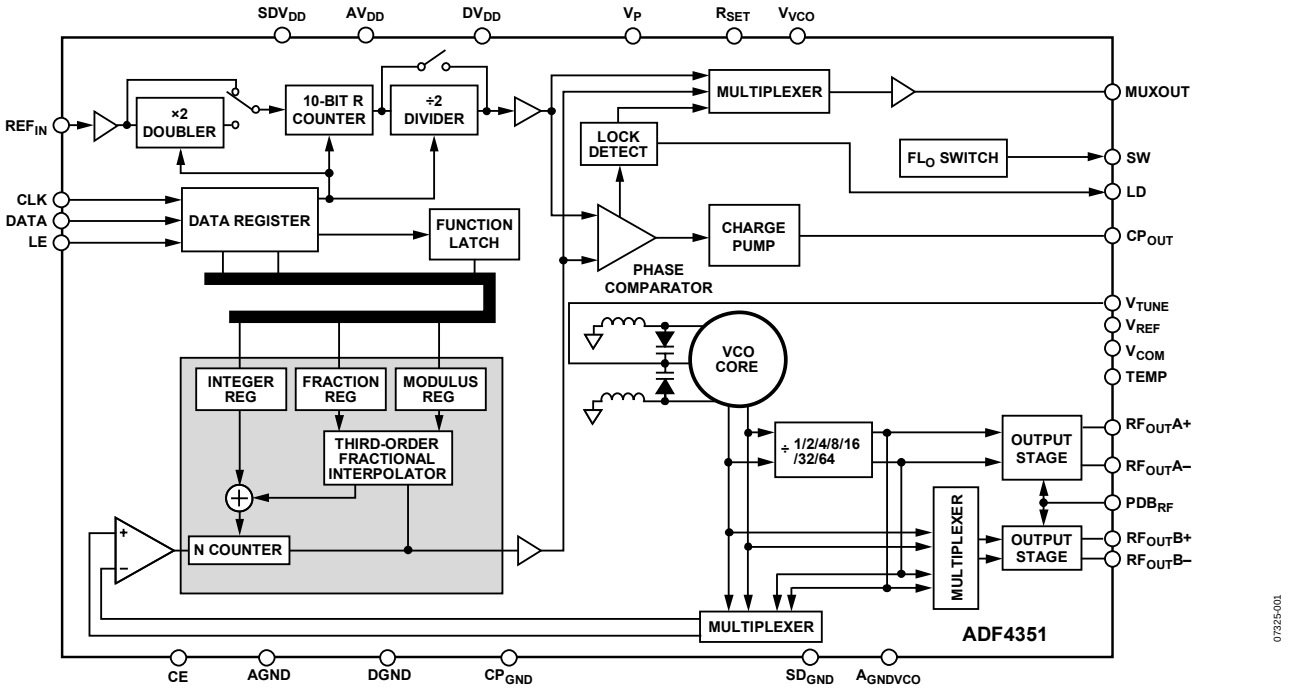

Figure 1.

Rev. PrC

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SPECIFICATIONS

AV_{DD} = DV_{DD} = V_{VCO} = SDV_{DD} = V_P = 3.3 V ± 10%; AGND = DGND = 0 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Operating temperature range is −40°C to +85°C.

Table 1.

	B Version				
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Conditions/Comments**
REF_{IN} CHARACTERISTICS					
Input Frequency	10		250	MHz	For f < 10 MHz ensure slew rate > 21 V/µs
Input Sensitivity	0.7		AV_{DD}	V p-p	Biased at AV_{DD}/2[1]
Input Capacitance		10		pF	
Input Current			±60	µA	
PHASE DETECTOR					
Phase Detector Frequency[2]			32	MHz	
CHARGE PUMP					
I_{CP} Sink/Source[3]					With R_{SET} = 5.1 kΩ
High Value		5		mA	
Low Value		0.312		mA	
R_{SET} Range	2.7		10	kΩ	
Sink and Source Current Matching		2		%	0.5 V ≤ V_{CP} ≤ 2.5 V
I_{CP} vs. V_{CP}		1.5		%	0.5 V ≤ V_{CP} ≤ 2.5 V
I_{CP} vs. Temperature		2		%	V_{CP} = 2.0 V
LOGIC INPUTS					
Input High Voltage, V_{INH}	1.5			V	
Input Low Voltage, V_{INL}			0.6	V	
Input Current, I_{INH}/I_{INL}			±1	µA	
Input Capacitance, C_{IN}		3.0		pF	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	DV_{DD} − 0.4			V	CMOS output chosen
Output High Current, I_{OH}			500	µA	
Output Low Voltage, V_{OL}			0.4	V	I_{OL} = 500 µA
POWER SUPPLIES					
AV_{DD}	3.0		3.6	V	
DV_{DD}, V_{VCO}, SD_{VDD}, V_P		AV_{DD}			These voltages must equal AV_{DD}
DI_{DD} + AI_{DD}[4]		21	27	mA	
Output Dividers		6 to 36		mA	Each output divide-by-2 consumes 6 mA
I_{VCO}[4]		70	80	mA	
I_{RFOUT}[4]		21	26	mA	RF output stage is programmable
Low Power Sleep Mode		7	TBD	µA	
RF OUTPUT CHARACTERISTICS					
Maximum VCO Output Frequency			4400	MHz	
Minimum VCO Output Frequency	2200			MHz	Fundamental VCO mode
Minimum VCO Output Frequency Using Dividers	34.375			MHz	2200 MHz fundamental output and divide by 64 selected
VCO Sensitivity		TBD		MHz/V	
Frequency Pushing (Open-Loop)		1		MHz/V	
Frequency Pulling (Open-Loop)		90		kHz	Into 2.00 VSWR load
Harmonic Content (Second)		−19		dBc	Fundamental VCO output
Harmonic Content (Third)		−13		dBc	Fundamental VCO output
Harmonic Content (Second)		−20		dBc	Divided VCO output
Harmonic Content (Third)		−10		dBc	Divided VCO output
Minimum RF Output Power[5]		−4		dBm	Programmable in 3 dB steps
Maximum RF Output Power[5]		5		dBm	
Output Power Variation		±1		dB	
Minimum VCO Tuning Voltage		0.5		V	
Maximum VCO Tuning Voltage		2.5		V	

Parameter	B Version Min	Typ	Max	Unit	Conditions/Comments
NOISE CHARACTERISTICS					
VCO Phase-Noise Performance[6]		−89		dBc/Hz	10 kHz offset from 2.2 GHz carrier
		−114		dBc/Hz	100 kHz offset from 2.2 GHz carrier
		−134		dBc/Hz	1 MHz offset from 2.2 GHz carrier
		−148		dBc/Hz	5 MHz offset from 2.2 GHz carrier
		−86		dBc/Hz	10 kHz offset from 3.3 GHz carrier
		−111		dBc/Hz	100 kHz offset from 3.3 GHz carrier
		−134		dBc/Hz	1 MHz offset from 3.3 GHz carrier
		−145		dBc/Hz	5 MHz offset from 3.3 GHz carrier
		−83		dBc/Hz	10 kHz offset from 4.4 GHz carrier
		−110		dBc/Hz	100 kHz offset from 4.4 GHz carrier
		−132		dBc/Hz	1 MHz offset from 4.4 GHz carrier
		−145		dBc/Hz	5 MHz offset from 4.4 GHz carrier
Normalized Phase Noise Floor (PN_{SYNTH})[7]		−220		dBc/Hz	PLL Loop BW = 500kHz (ABP = 6 ns)
Normalized 1/f Noise (PN_{1_f})[8]		-116		dBc/Hz	10kHz offset. Normalized to 1GHz. (ABP = 6 ns)
Normalized Phase Noise Floor (PN_{SYNTH})[7]		−221		dBc/Hz	PLL Loop BW = 500kHz (ABP = 3 ns)
Normalized 1/f Noise (PN_{1_f})[8]		-118		dBc/Hz	10kHz offset. Normalized to 1GHz. (ABP = 3 ns)
Integrated RMS Jitter[9]		0.32		ps	
Spurious Signals Due to PFD Frequency		−80		dBc	
Level of Signal With RF Mute Enabled		−40		dBm	

[1] AC coupling ensures $AV_{DD}/2$ bias.
[2] Guaranteed by design. Sample tested to ensure compliance.
[3] I_{CP} is internally modified to maintain constant loop gain over the frequency range.
[4] T_A = 25°C; AV_{DD} = DV_{DD} = V_{VCO} = 3.3 V; prescaler = 8/9; f_{REFIN} = 100 MHz; f_{PFD} = 25 MHz; f_{RF} = 4.4 GHz.
[5] Using 50 Ω resistors to V_{VCO}, into a 50 Ω load. Power measured with auxiliary RF output disabled. The current consumption of the auxiliary output is the same as for the main output.
[6] The noise of the VCO is measured in open-loop conditions.
[7] The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20 log N (where N is the N divider value) and 10 log F_{PFD}. $PN_{SYNTH} = PN_{TOT} - 10 \log F_{PFD} - 20 \log N$.
[8] The PLL phase noise is composed of 1/f (flicker) noise plus the normalized PLL noise floor. The formula for calculating the 1/f noise contribution at an RF frequency F_{RF} and at a frequency offset f is given by $PN = P_{1\_f} + 10\log(10kHz/f) + 20\log(F_{RF}/1GHz)$. Both the normalized phase noise floor and flicker noise are modeled in ADIsimPLL.
[9] f_{REFIN} = 100 MHz; f_{PFD} = 25 MHz; VCO frequency = 4222.56 MHz, RF_{OUT} = 2111.28 MHz; N = 168; loop BW = 40 kHz, I_{CP} = 2.5 mA; low noise mode. The noise was measured with an EVAL-ADF4351EB1Z and the Rohde & Schwarz FSUP signal source analyzer.

TIMING CHARACTERISTICS

AV_{DD} = DV_{DD} = V_{VCO} = SDV_{DD} = V_P = 3.3 V ± 10%; AGND = DGND = 0 V; 1.8 V and 3 V logic levels used; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Limit (B Version)	Unit	Test Conditions/Comments
t_1	20	ns min	LE setup time
t_2	10	ns min	DATA to CLK setup time
t_3	10	ns min	DATA to CLK hold time
t_4	25	ns min	CLK high duration
t_5	25	ns min	CLK low duration
t_6	10	ns min	CLK to LE setup time
t_7	20	ns min	LE pulse width

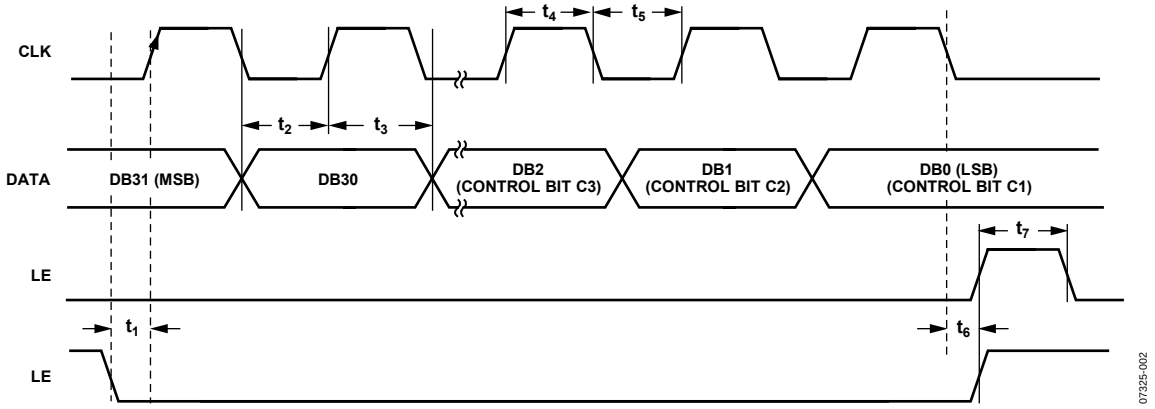


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AV_{DD} to GND[1]	−0.3 V to +3.9 V
AV_{DD} to DV_{DD}	−0.3 V to +0.3 V
V_{VCO} to GND	−0.3 V to +3.9 V
V_{VCO} to AV_{DD}	−0.3 V to +0.3 V
Digital I/O Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to GND	−0.3 V to V_{DD} + 0.3 V
REF_{IN} to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
LFCSP θ_{JA} Thermal Impedance (Paddle-Soldered)	27.3°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec

[1] GND = AGND = DGND = 0 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high-performance RF integrated circuit with an ESD rating of <0.5 kV and is ESD sensitive. Proper precautions should be taken for handling and assembly.

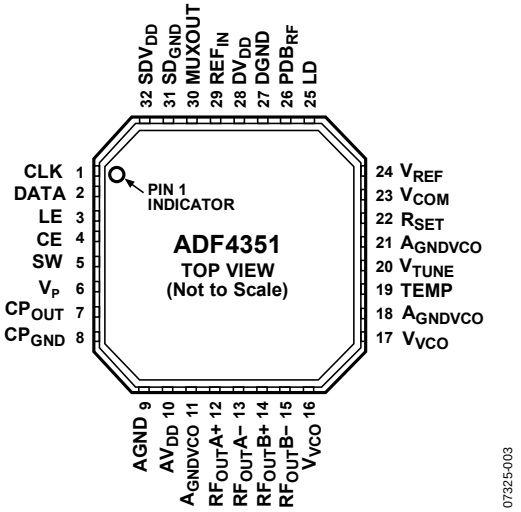
TRANSISTOR COUNT

TBD (CMOS) and TBD (bipolar)

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE LFCSP HAS AN EXPOSED PADDLE THAT MUST BE CONNECTED TO GND.

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CLK	Serial Clock Input. Data is clocked into the 32-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
2	DATA	Serial Data Input. The serial data is loaded MSB first with the three LSBs as the control bits. This input is a high impedance CMOS input.
3	LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift register is loaded into the register that is selected by the three LSBs.
4	CE	Chip Enable. A logic low on this pin powers down the device and puts the charge pump into three-state mode. A logic high on this pin powers up the device depending on the status of the power-down bits.
5	SW	Fast-Lock Switch. A connection should be made from the loop filter to this pin when using the fast-lock mode.
6	V_P	Charge Pump Power Supply. This pin is to be equal to AV_{DD}. Decoupling capacitors to the ground plane are to be placed as close as possible to this pin.
7	CP_{OUT}	Charge Pump Output. When enabled, this provides $\pm I_{CP}$ to the external loop filter. The output of the loop filter is connected to V_{TUNE} to drive the internal VCO.
8	CP_{GND}	Charge Pump Ground. This is the ground return pin for CP_{OUT}.
9	AGND	Analog Ground. This is a ground return pin for AV_{DD}.
10	AV_{DD}	Analog Power Supply. This pin ranges from 3.0 V to 3.6 V. Decoupling capacitors to the analog ground plane are to be placed as close as possible to this pin. AV_{DD} must have the same value as DV_{DD}.
11, 18, 21	A_{GNDVCO}	VCO Analog Ground. These are the ground return pins for the VCO.
12	$RF_{OUT}A+$	VCO Output. The output level is programmable. The VCO fundamental output or a divided down version is available.
13	$RF_{OUT}A–$	Complementary VCO Output. The output level is programmable. The VCO fundamental output or a divided down version is available.
14	$RF_{OUT}B+$	Auxilliary VCO Output. The output level is programmable. The VCO fundamental output or a divided down version is available.
15	$RF_{OUT}B–$	Complementary Auxilliary VCO Output. The output level is programmable. The VCO fundamental output or a divided down version is available.
16, 17	V_{VCO}	Power Supply for the VCO. This ranges from 3.0 V to 3.6 V. Decoupling capacitors to the analog ground plane should be placed as close as possible to these pins. V_{VCO} must have the same value as AV_{DD}.
19	TEMP	Temperature Compensation Output. Decoupling capacitors to the ground plane are to be placed as close as possible to this pin.
20	V_{TUNE}	Control Input to the VCO. This voltage determines the output frequency and is derived from filtering the CP_{OUT} output voltage.

Pin No.	Mnemonic	Description
22	R_{SET}	Connecting a resistor between this pin and GND sets the charge pump output current. The nominal voltage bias at the R_{SET} pin is 0.55 V. The relationship between I_{CP} and R_{SET} is $I_{CP} = \frac{25.5}{R_{SET}}$ where: R_{SET} = 5.1 kΩ I_{CP} = 5 mA
23	V_{COM}	Internal Compensation Node Biased at Half the Tuning Range. Decoupling capacitors to the ground plane should be placed as close as possible to this pin.
24	V_{REF}	Reference Voltage. Decoupling capacitors to the ground plane should be placed as close as possible to this pin.
25	LD	Lock Detect Output Pin. This pin outputs a logic high to indicate PLL lock. A logic low output indicates loss of PLL lock.
26	PDB_{RF}	RF Power-Down. A logic low on this pin mutes the RF outputs. This function is also software controllable.
27	DGND	Digital Ground. Ground return path for DV_{DD}.
28	DV_{DD}	Digital Power Supply. This pin should be the same voltage as AV_{DD}. Decoupling capacitors to the ground plane should be placed as close as possible to this pin.
29	REF_{IN}	Reference Input. This is a CMOS input with a nominal threshold of V_{DD}/2 and a dc equivalent input resistance of 100 kΩ. This input can be driven from a TTL or CMOS crystal oscillator, or it can be ac-coupled.
30	MUXOUT	Multiplexer Output. This multiplexer output allows either the lock detect, the scaled RF, or the scaled reference frequency to be accessed externally.
31	SD_{GND}	Digital Sigma-Delta (Σ-Δ) Modulator Ground. Ground return path for the Σ-Δ modulator.
32	SDV_{DD}	Power Supply Pin for the Digital Σ-Δ Modulator. Should be the same voltage as AV_{DD}. Decoupling capacitors to the ground plane are to be placed as close as possible to this pin.
33	EP	Exposed Pad.

TYPICAL PERFORMANCE CHARACTERISTICS

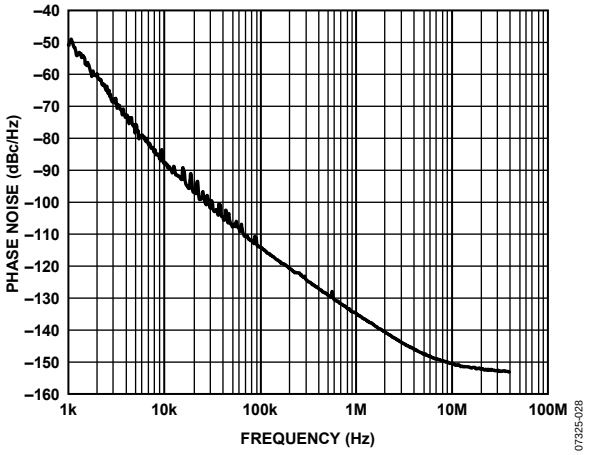


Figure 4. Open-Loop VCO Phase Noise, 2.2 GHz

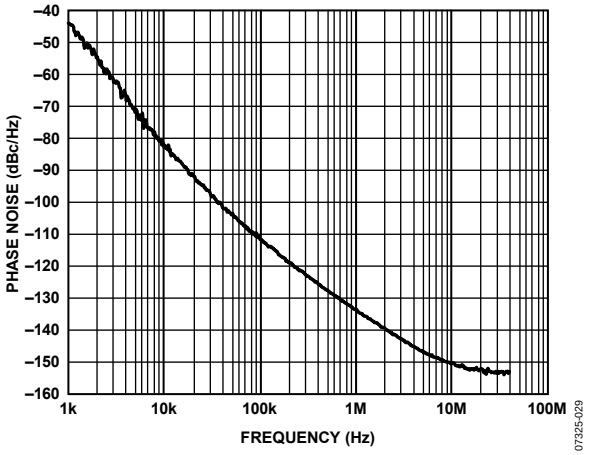


Figure 5. Open-Loop VCO Phase Noise, 3.3 GHz

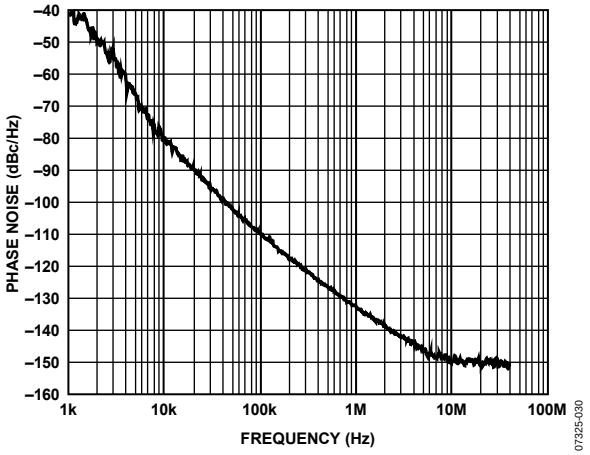


Figure 6. Open-Loop VCO Phase Noise, 4.4 GHz

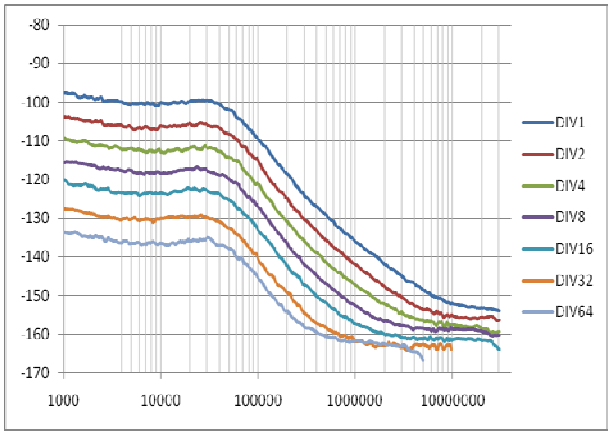


Figure 7. Closed-Loop Phase Noise, Fundamental VCO and Dividers, VCO = 2.2 GHz, PFD = 25 MHz, Loop Bandwidth = 43 kHz

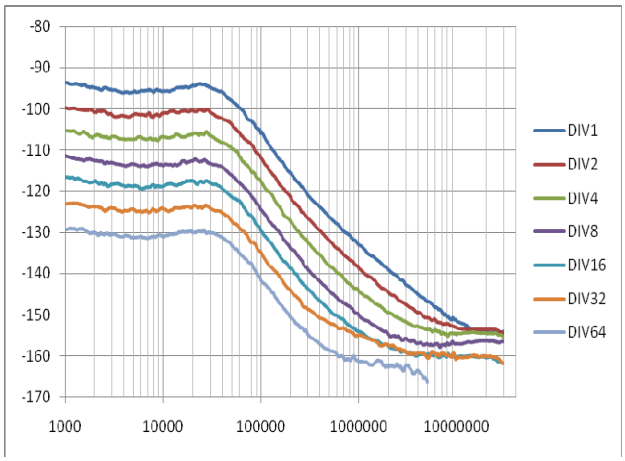


Figure 8. Closed-Loop Phase Noise, Fundamental VCO and Dividers, VCO = 3.3 GHz, PFD = 25 MHz, Loop Bandwidth = 43 kHz

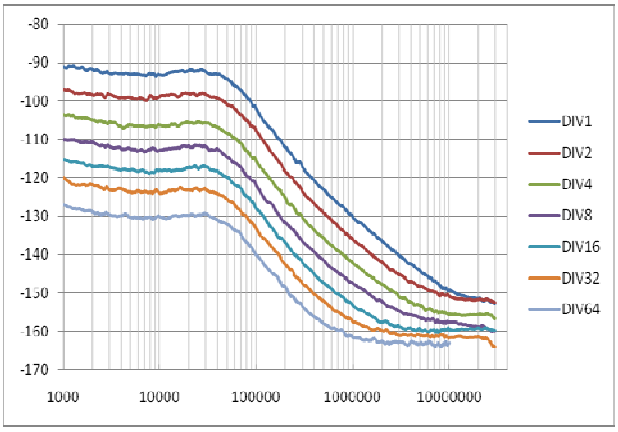


Figure 9. Closed-Loop Phase Noise, Fundamental VCO and Dividers, VCO = 4.4 GHz, PFD = 25 MHz, Loop Bandwidth = 43 kHz

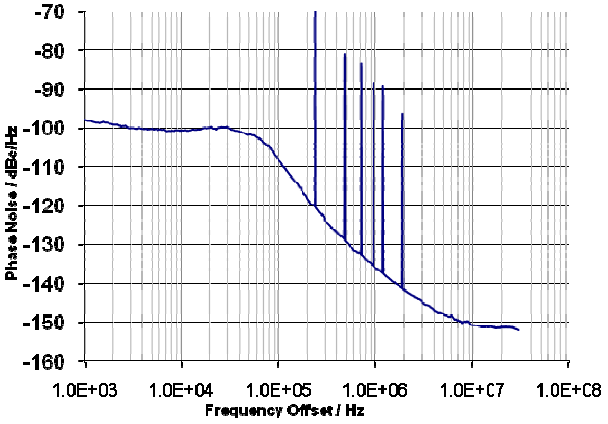


Figure 10. Fractional-N Spur Performance; Low Noise Mode. W-CDMA Band, RF_{OUT} = 2111.28 MHz, REF_{IN} = 100 MHz, PFD = 25 MHz, Output Div-by-2 Selected; Loop B/W= 40 kHz, Channel Spacing = 240 kHz. RMS Phase error = 0.22°, RMS Jitter = 0.3 ps, EVM = 0.38%

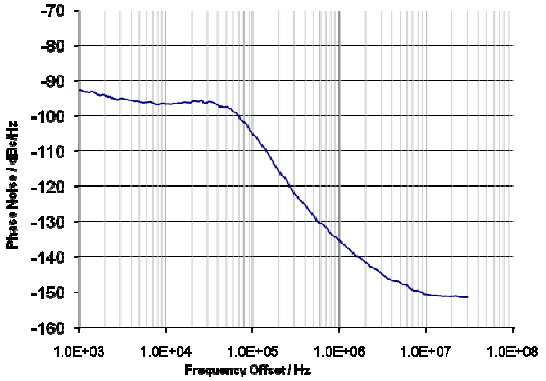


Figure 11. Fractional-N Spur Performance; Low Spur Mode. W-CDMA Band, RF_{OUT} = 2111.28 MHz, REF_{IN} = 100 MHz, PFD = 25 MHz, Output Divide-by-2 Selected; Loop Filter Bandwidth = 40 kHz, Channel Spacing = 240 kHz, RMS Phase error = 0.35°, RMS Jitter = 0.46 ps, EVM = 0.60% .

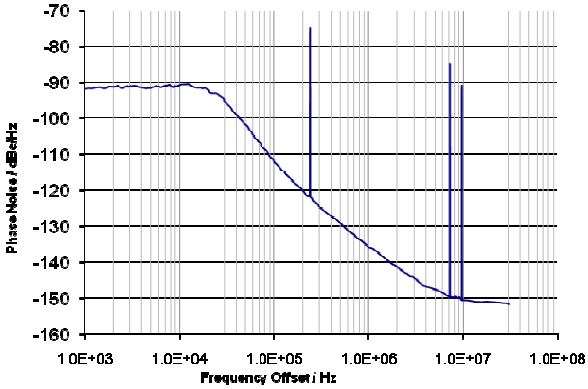


Figure 12. Fractional-N Spur Performance; Low Noise Mode. W-CDMA Band, RF_{OUT} = 2111.28 MHz, REF_{IN} = 100 MHz, PFD = 25 MHz, Output Divide-by-2 Selected; Loop Filter Bandwidth = 20 kHz, Channel Spacing = 240 kHz, RMS Phase error = 0.39°, RMS Jitter = 0.51 ps, EVM = 0.68% .

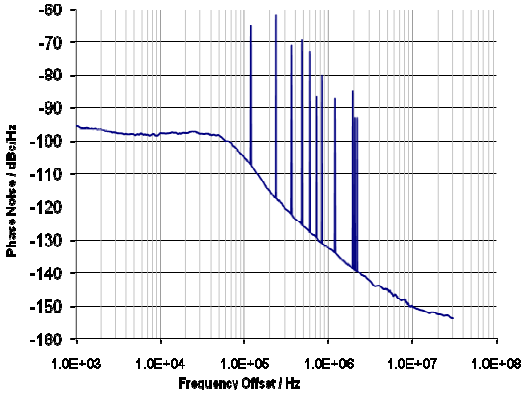


Figure 13. Fractional-N Spur Performance; Low Noise Mode. LTE Band, RF_{OUT} = 2646.96 MHz, REF_{IN} = 100 MHz, PFD = 25 MHz, Loop Filter Bandwidth = 40 kHz, Channel Spacing = 240 kHz, Phase word =9. RMS Phase error = 0.3°, RMS Jitter = 0.31 ps, EVM = 0.52% .

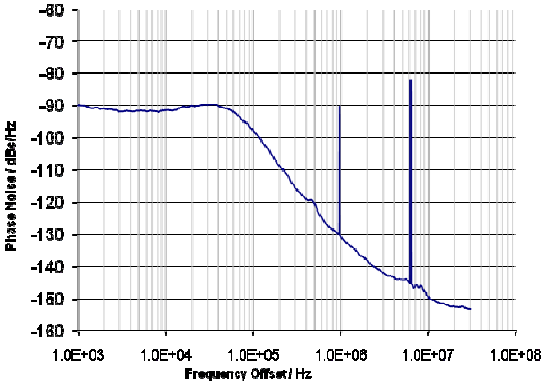


Figure 14. Fractional-N Spur Performance; Low Spur Mode. LTE Band, RF_{OUT} = 2646.96 MHz, REF_{IN} = 100 MHz, PFD = 25 MHz, Loop Filter Bandwidth = 40 kHz, Channel Spacing = 240 kHz, RMS Phase error = 0.69°, RMS Jitter = 0.72 ps, EVM = 1.2%.

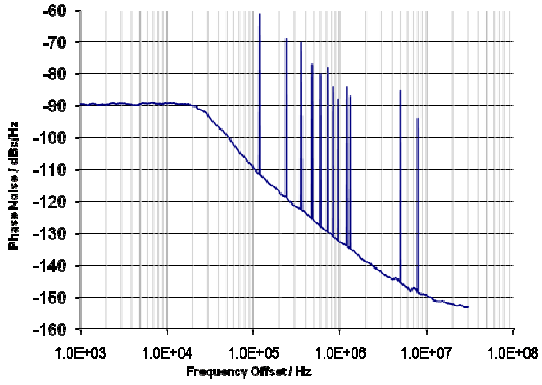


Figure 15. Fractional-N Spur Performance; Low Noise Mode. W-CDMA Band, RF_{OUT} = 2646.96 MHz, REF_{IN} = 100 MHz, PFD = 25 MHz, Loop Filter Bandwidth = 20 kHz, Channel Spacing = 240 kHz, RMS Phase error = 0.49°, RMS Jitter = 0.52 ps, EVM = 0.86%.

CIRCUIT DESCRIPTION

REFERENCE INPUT SECTION

The reference input stage is shown in Figure 16. SW1 and SW2 are normally closed switches. SW3 is normally open. When power-down is initiated, SW3 is closed, and SW1 and SW2 are opened. This ensures that there is no loading of the REF_{IN} pin during power-down.

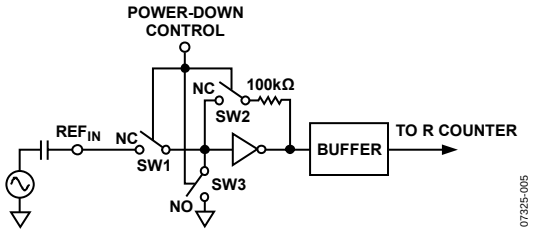


Figure 16. Reference Input Stage

RF N DIVIDER

The RF N divider allows a division ratio in the PLL feedback path. The division ratio is determined by INT, FRAC and MOD values, which build up this divider.

INT, FRAC, MOD, AND R COUNTER RELATIONSHIP

The INT, FRAC, and MOD values, in conjunction with the R counter, make it possible to generate output frequencies that are spaced by fractions of the PFD frequency. See the RF Synthesizer—A Worked Example section for more information. The RF VCO frequency (RF_{OUT}) equation is

$$RF_{OUT} = f_{PFD} \times (INT + (FRAC/MOD)) \quad (1)$$

where RF_{OUT} is the output frequency of external voltage controlled oscillator (VCO).
INT is the preset divide ratio of the binary 16-bit counter (23 to 65535 for 4/5 prescaler, 75 to 65,535 for 8/9 prescaler).
MOD is the preset fractional modulus (2 to 4095).
FRAC is the numerator of the fractional division (0 to MOD − 1).

$$f_{PFD} = REF_{IN} \times [(1 + D)/(R \times (1 + T))] \quad (2)$$

where:
REF_{IN} is the reference input frequency.
D is the REF_{IN} doubler bit.
T is the REF_{IN} divide-by-2 bit (0 or 1).
R is the preset divide ratio of the binary 10-bit programmable reference counter (1 to 1023).

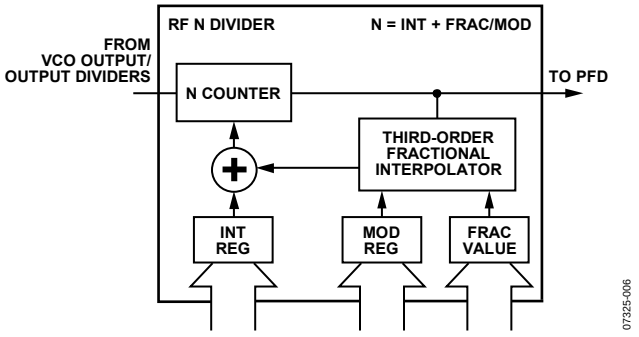


Figure 17. RF INT Divider

INT N MODE

If the FRAC = 0 and DB8 in Register 2 (LDF) is set to 1, the synthesizer operates in integer-N mode. The DB8 in Register 2 (LDF) should be set to 1 to get integer-N digital lock detect.

R COUNTER

The 10–bit R counter allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the PFD. Division ratios from 1 to 1023 are allowed.

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The phase frequency detector (PFD) takes inputs from the R counter and N counter and produces an output proportional to the phase and frequency difference between them. Figure is a simplified schematic of the phase frequency detector. The PFD includes a programmable delay element that sets the width of the anti-backlash pulse. This is controlled by bit DB22, register 3, which if set to '0' programs a 6 ns delay for Fractional-N applications or if programmed with a '1' programs a 3 ns delay for Integer-N applications. This pulse ensures there is no dead zone in the PFD transfer function.

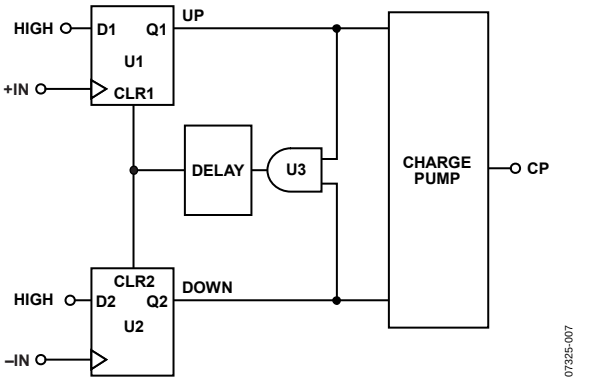


Figure 18. PFD Simplified Schematic

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4351 allows the user to access various internal points on the chip. The state of MUXOUT is controlled by M3, M2, and M1 (for details, see Figure 26). Figure shows the MUXOUT section in block diagram form.

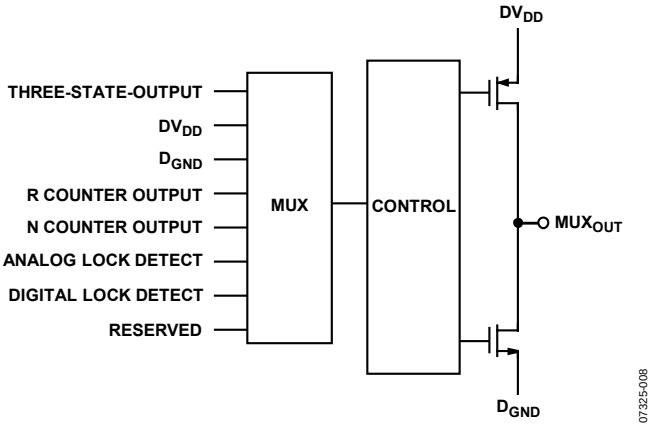


Figure 19. MUXOUT Schematic

INPUT SHIFT REGISTERS

The ADF4351 digital section includes a 10–bit RF R counter, a 16–bit RF N counter, a 12-bit FRAC counter, and a 12–bit modulus counter. Data is clocked into the 32–bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of six latches on the rising edge of LE. The destination latch is determined by the state of the three control bits (C3, C2, and C1) in the shift register. These are the 3 LSBs, DB2, DB1, and DB0, as shown in Figure 2. The truth table for these bits is shown in Table 5. Figure shows a summary of how the latches are programmed.

Table 5. C3, C2, and C1 Truth Table

Control Bits			
C3	**C2**	**C1**	**Register**
0	0	0	Register 0 (R0)
0	0	1	Register 1 (R1)
0	1	0	Register 2 (R2)
0	1	1	Register 3 (R3)
1	0	0	Register 4 (R4)
1	0	1	Register 5 (R5)

PROGRAM MODES

Table 5 and Figure through Figure show how the program modes are to be set up in the ADF4351.

A number of settings in the ADF4351 are double buffered. These include the modulus value, phase value, R counter value, reference doubler, reference divide-by-2, and current setting. This means that two events have to occur before the part uses a new value of any of the double buffered settings. First, the new value is latched into the device by writing to the appropriate register. Second, a new write must be performed on Register R0. For example, any time the modulus value is updated, Register 0 (R0) must be written to, to ensure the modulus value is loaded correctly. Divider select in Register 4 (R4) is also double buffered, but only if DB13 of Register 2 (R2) is high.

VCO

The VCO core in the ADF4351 consists of three separate VCOs each of which uses 16 overlapping bands, as shown in Figure , to allow a wide frequency range to be covered without a large VCO sensitivity (K_V) and resultant poor phase noise and spurious performance.

The correct VCO and band are chosen automatically by the VCO and band select logic at power-up or whenever Register 0 (R0) is updated.

VCO and band selection take 10 PFD cycles × band select clock divider value. The VCO V_{TUNE} is disconnected from the output of the loop filter and is connected to an internal reference voltage.

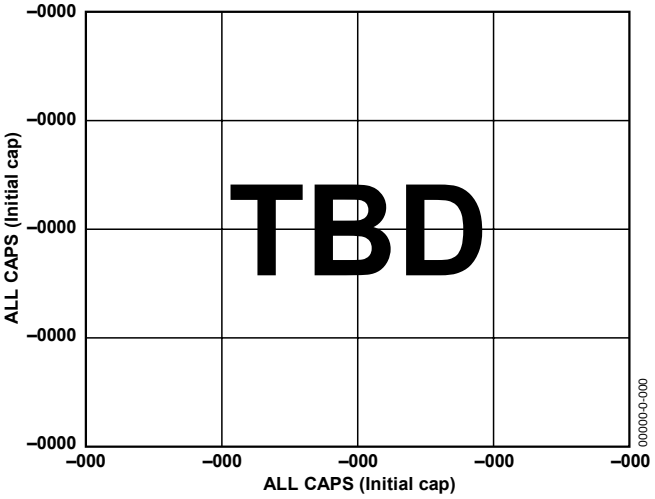


Figure 20. V_{TUNE} vs. Frequency

The R counter output is used as the clock for the band select logic. A programmable divider is provided at the R counter output to allow division by 1 to 255 and is controlled by Bits [BS8:BS1] in Register 4 (R4). When the required PFD frequency is higher than 125 kHz, the divide ratio should be set to allow enough time for correct band selection. Band select takes 10 cycles of this frequency, equal to 80 µs. If faster lock times are required, then bit DB23 in Register R3 must be set high. This allows the user to choose a higher band select clock frequency of up to 1 MHz, which speeds up the minimum band select time to 10 µs.

After band select, normal PLL action resumes. The nominal value of K_V is 33 MHz/V when the N-divider is driven from the VCO output or this value divided by D. D is the output divider value if the N-divider is driven from the RF divider output (chosen by programming Bits [D12:D10] in Register 4 (R4). The ADF4351 contains linearization circuitry to minimize any variation of the product of I_{CP} and K_V to keep the loop bandwidth constant.

The VCO shows variation of K_V as the V_{TUNE} varies within the band and from band-to-band. It has been shown for wideband applications covering a wide frequency range (and changing output dividers) that a value of 33 MHz/V provides the most accurate K_V as this is closest to an average value. Figure shows how K_V varies with fundamental VCO frequency along with an average value for the frequency band. Users may prefer this figure when using narrowband designs.

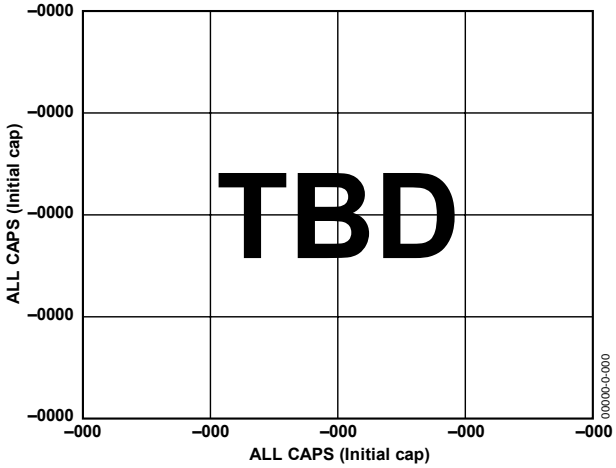


Figure 21. K_V vs. Frequency

OUTPUT STAGE

The $RF_{OUT}A+$ and $RF_{OUT}A–$ pins of the ADF4351 are connected to the collectors of an NPN differential pair driven by buffered outputs of the VCO, as shown in Figure . To allow the user to optimize the power dissipation vs. the output power requirements, the tail current of the differential pair is programmable by Bits [D2:D1] in Register 4 (R4). Four current levels of 8 mA, 11 mA , 15 mA and 21 mA may be set. These levels give output power levels of −4 dBm, −1 dBm, +2 dBm, and +5 dBm, respectively, using a 50 Ω resistor to AV_{DD} and ac coupling into a 50 Ω load. Alternatively, both outputs can be combined in a 1 + 1:1 transformer or a 180° microstrip coupler (see the Output Matching section). If the outputs are used individually, the optimum output stage consists of a shunt inductor to V_{VCO}. The unused complementary output must
be terminated with a similar circuit to the used output.

An auxiliary output stage exists on Pins $RF_{OUT}B+$ and $RF_{OUT}B–$ providing a second set of differential outputs which can be used to drive another circuit, or which can be powered down if unused. The auxiliary output stage can only be used if the primary outputs are enabled.

Another feature of the ADF4351 is that the supply current to the RF output stage can be shut down until the part achieves lock as measured by the digital lock detect circuitry. This is enabled by the mute till lock detect (MTLD) bit in Register 4 (R4).

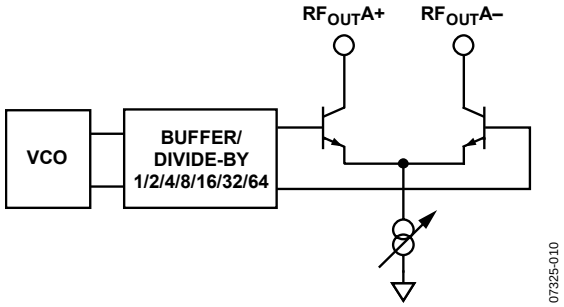


Figure 22. Output Stage

REGISTER MAPS

REGISTER 0

RESERVED	16-BIT INTEGER VALUE (INT)																12-BIT FRACTIONAL VALUE (FRAC)												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	N16	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	C3(0)	C2(0)	C1(0)

REGISTER 1

RESERVED			PHASE ADJUST	PRESCALER	12-BIT PHASE VALUE (PHASE) DBR[1]												12-BIT MODULUS VALUE (MOD) DBR[1]												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	PH1	P1	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	C3(0)	C2(0)	C1(1)

REGISTER 2

RESERVED	NOISE MODE		MUXOUT			REFERENCE DOUBLER DBR[1]	RDIV2 DBR[1]	10-BIT R COUNTER DBR[1]									DOUBLE BUFF	CURRENT SETTING DBR[1]				LDF	LDP	PD POLARITY	PD	CP THREE-STATE	COUNTER RESET	CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	L2	L1	M3	M2	M1	RD2	RD1	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	D1	CP4	CP3	CP2	CP1	U6	U5	U4	U3	U2	U1	C3(0)	C2(1)	C1(0)

REGISTER 3

RESERVED								BAND SELECT MODE	ABP	CHARGE CANCEL	RESERVED	CSR	RESERVED	CLK DIV MODE	12-BIT CLOCK DIVIDER VALUE												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	BS1	F3	F2	V2	V1	F1	0	C2	C1	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	C3(0)	C2(1)	C1(1)

REGISTER 4

RESERVED								FEEDBACK SELECT	DBB[2] DIVIDER SELECT			RESERVED									MTLD	RESERVED				RF OUTPUT ENABLE	OUTPUT POWER		CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	D13	D12	D11	D10	0	0	0	0	0	0	0	0	0	D8	D7	D6	D5	D4	D3	D2	D1	C3(1)	C2(0)	C1(0)

REGISTER 5

RESERVED								LD PIN MODE		RESERVED	RESERVED		RESERVED																CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	D15	D14	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C3(1)	C2(0)	C1(1)

[1]DBR = DOUBLE BUFFERED REGISTER—BUFFERED BY THE WRITE TO REGISTER 0.
[2]DBB = DOUBLE BUFFERED BITS—BUFFERED BY THE WRITE TO REGISTER 0, IF AND ONLY IF DB13 OF REGISTER 2 IS HIGH.

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Figure 23. Register Summary

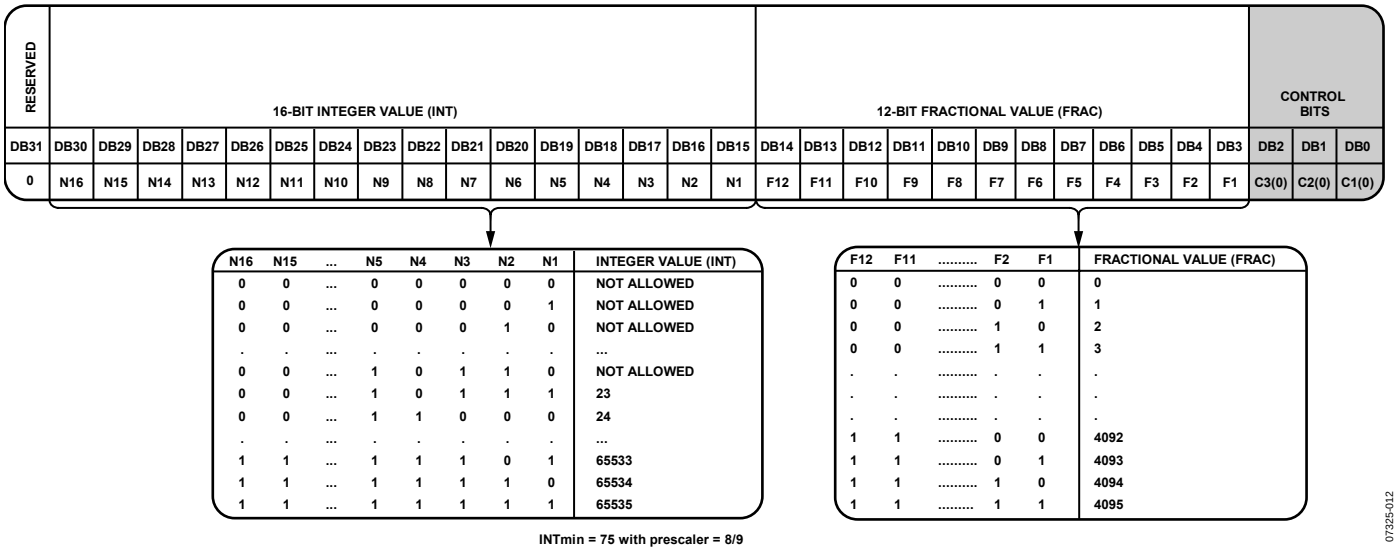


Figure 24. Register 0 (R0)

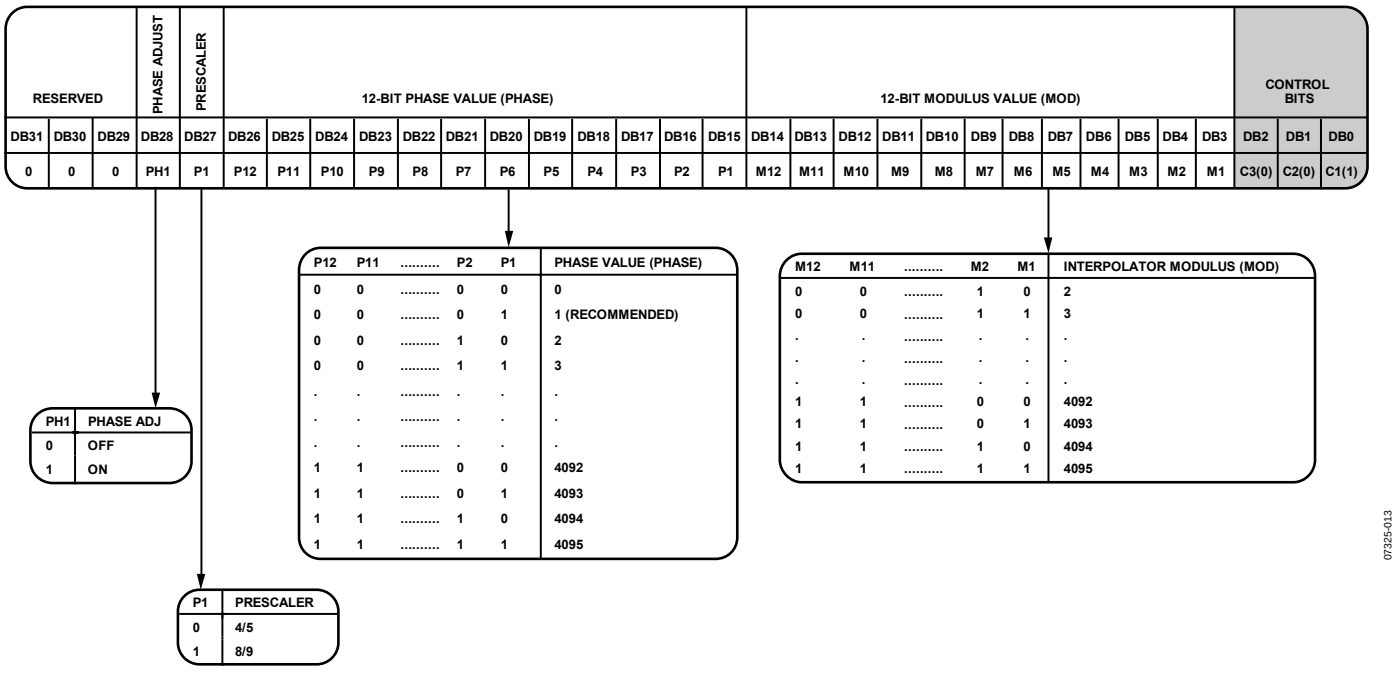


Figure 25. Register 1 (R1)

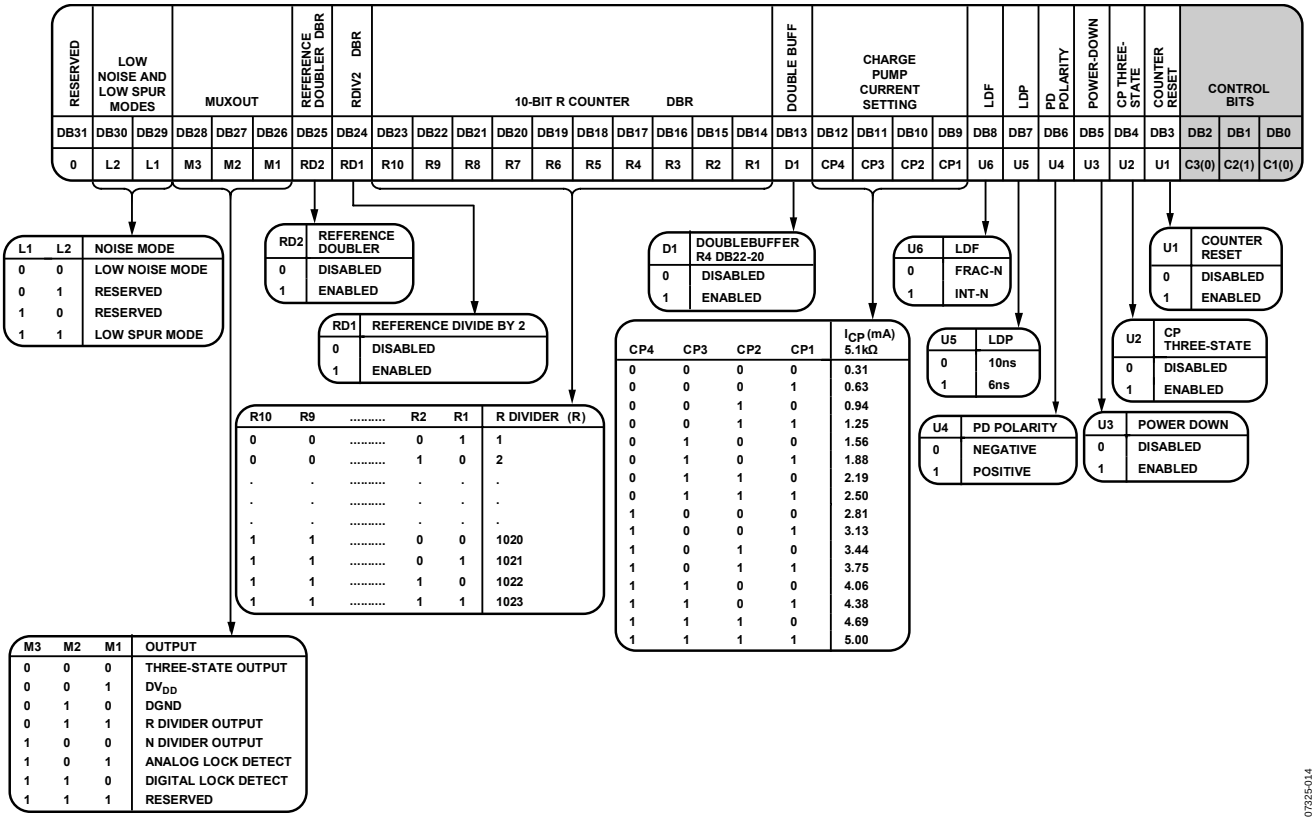


Figure 26. Register 2 (R2)

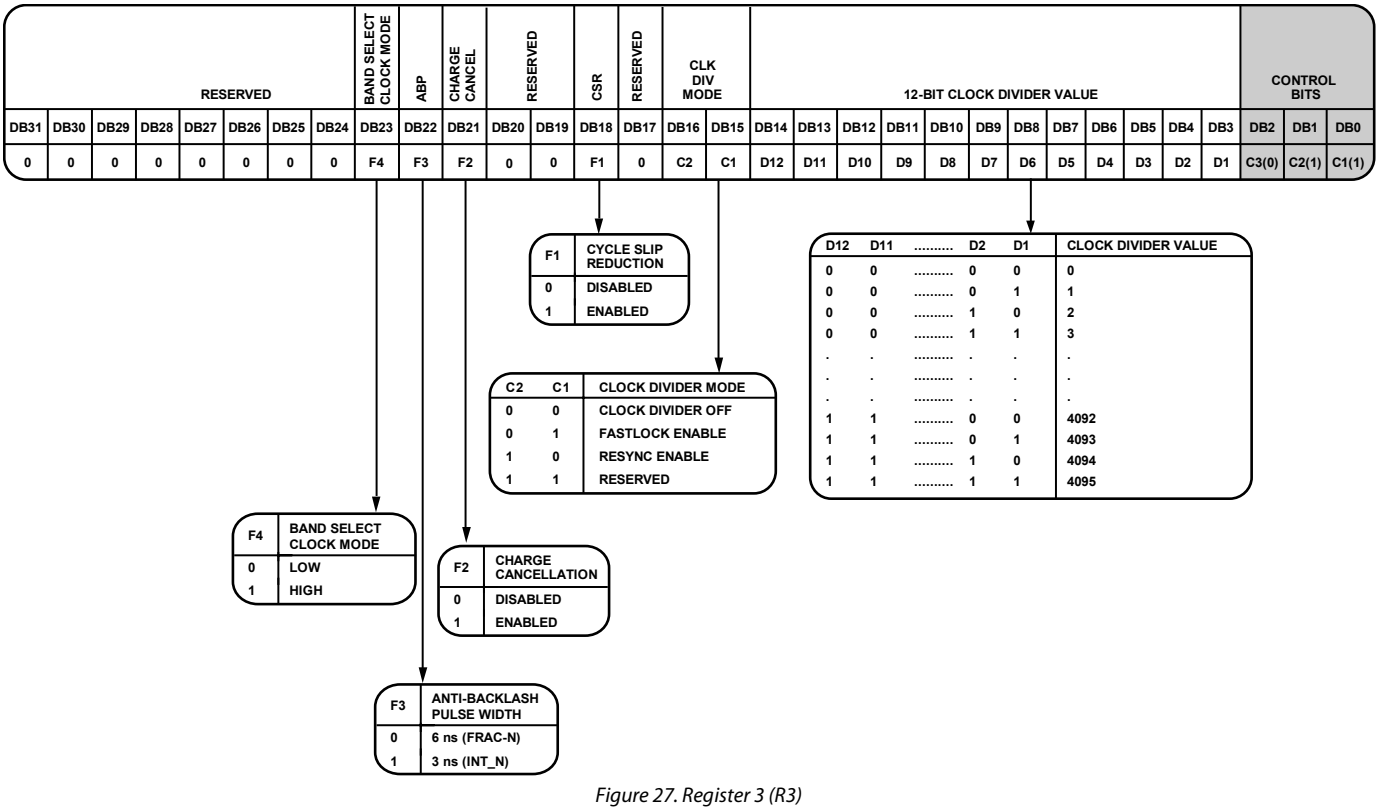


Figure 27. Register 3 (R3)

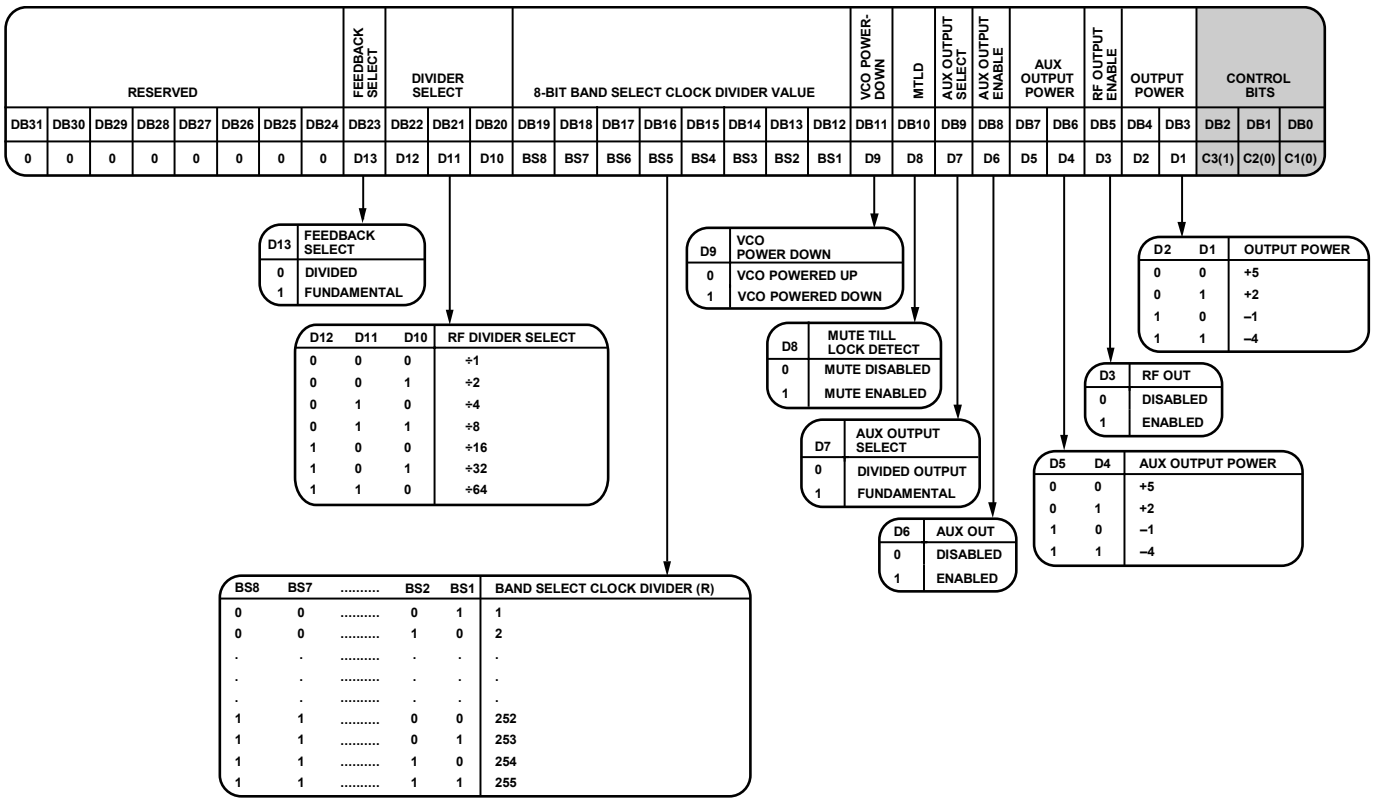


Figure 28. Register 4 (R4)

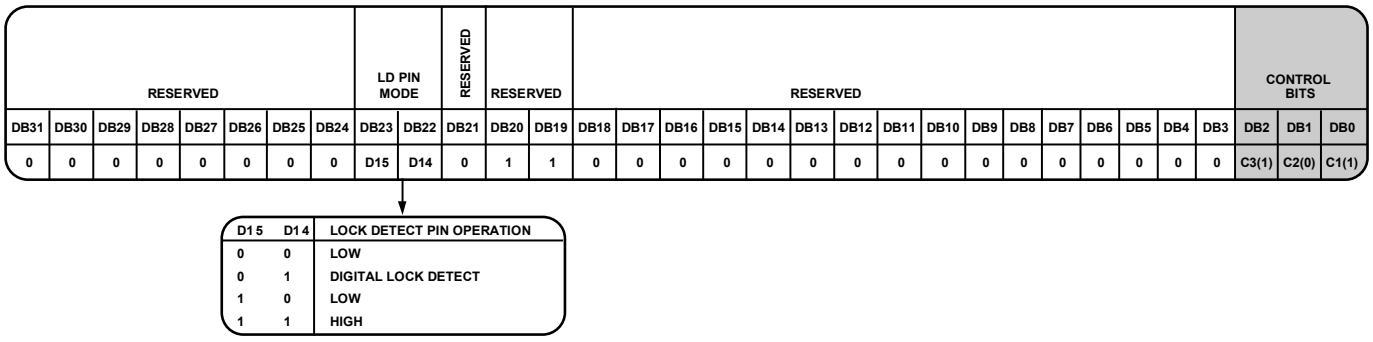


Figure 29. Register 5 (R5)

REGISTER 0

Control Bits

With Bits [C3:C1] set to 0, 0, 0, Register 0 is programmed. Figure shows the input data format for programming this register.

16-Bit INT Value

These sixteen bits set the INT value, which determines the integer part of the feedback division factor. It is used in Equation 1 (see the INT, FRAC, MOD, and R Counter Relationship section). All integer values from 23 to 65,535 are allowed for 4/5 prescaler. For 8/9 prescaler, the minimum integer value is 75.

12-Bit FRAC Value

The 12 FRAC bits set the numerator of the fraction that is input to the Σ-Δ modulator. This, along with INT, specifies the new frequency channel that the synthesizer locks to, as shown in the RF Synthesizer—A Worked Example section. FRAC values from 0 to MOD − 1 cover channels over a frequency range equal to the PFD reference frequency.

REGISTER 1

Control Bits

With Bits [C3:C1] set to 0, 0, 1, Register 1 is programmed. Figure shows the input data format for programming this register.

Phase Adjust

The phase adjust bit, enabled by programming a '1' to DB28, permits adjustments to the output phase of a given output frequency. If enabled, it will not perform a band select or a phase resync function on updating R0. If set to '0' then band select and phase resync, (if enabled in R3) will occur on every update of R0.

Prescaler Value

The dual modulus prescaler (P/P + 1), along with the INT, FRAC, and MOD counters, determines the overall division ratio from the VCO output to the PFD input.

Operating at CML levels, the prescaler takes the clock from the VCO output and divides it down for the counters. It is based on a synchronous 4/5 core. When set to 4/5, the maximum RF frequency allowed is 3 GHz. Therefore, when operating the ADF4351 above 3 GHz, this must be set to 8/9. The prescaler limits the INT value, where P is 4/5, N_{MIN} is 23 and P is 8/9, N_{MIN} is 75.

In the ADF4351, PR1 in Register 1 sets the prescaler values.

12-Bit Phase Value

These bits control what is loaded as the phase word. The word must be less than the MOD value programmed in Register 1. The word is used to program the RF output phase from 0° to 360° with a resolution of 360°/MOD. See the Phase Resync section for more information. In most applications, the phase relationship between the RF signal and the reference is not important. In such applications, the phase value can be used to optimize the fractional and subfractional spur levels. See the Spur Consistency and Fractional Spur Optimization section for more information.

If neither the phase resync nor the spurious optimization functions are being used, it is recommended the PHASE word be set to 1.

12-Bit Interpolator MOD Value

This programmable register sets the fractional modulus. This is the ratio of the PFD frequency to the channel step resolution on the RF output. See the RF Synthesizer—A Worked Example section for more information.

REGISTER 2

Control Bits

With Bits [C3:C1] set to 0, 1, 0, Register 2 is programmed. Figure shows the input data format for programming this register.

Low Noise and Low Spur Modes

The noise modes on the ADF4351 are controlled by DB30 and DB29 in Register 2 (see Figure). The noise modes allow the user to optimize a design either for improved spurious performance or for improved phase noise performance.

When the lowest spur setting is chosen, dither is enabled. This randomizes the fractional quantization noise so it resembles white noise rather than spurious noise. As a result, the part is optimized for improved spurious performance. This operation would normally be used when the PLL closed-loop bandwidth is wide, for fast-locking applications. Wide loop bandwidth is seen as a loop bandwidth greater than 1/10 of the RF_{OUT} channel step resolution (f_{RES}). A wide loop filter does not attenuate the spurs to the same level as a narrow loop bandwidth.

For best noise performance, use the lowest noise setting option. As well as disabling the dither, this setting also ensures that the charge pump is operating in an optimum region for noise performance. This setting is extremely useful where a narrow loop filter bandwidth is available. The synthesizer ensures extremely low noise and the filter attenuates the spurs. The typical performance characteristics give the user an idea of the trade-off in a typical W-CDMA setup for the different noise and spur settings.

MUXOUT

The on-chip multiplexer is controlled by Bits [DB28:DB26] (see Figure).

Reference Doubler

Setting DB25 to 0 feeds the REF_{IN} signal directly to the 10–bit R counter, disabling the doubler. Setting this bit to 1 multiplies the REF_{IN} frequency by a factor of 2 before feeding into the 10-bit R counter. When the doubler is disabled, the REF_{IN} falling edge is the active edge at the PFD input to the fractional

synthesizer. When the doubler is enabled, both the rising and falling edges of REF_{IN} become active edges at the PFD input.

When the doubler is enabled and the lowest spur mode is chosen, the in-band phase noise performance is sensitive to the REF_{IN} duty cycle. The phase noise degradation can be as much as 5 dB for the REF_{IN} duty cycles outside a 45% to 55% range. The phase noise is insensitive to the REF_{IN} duty cycle in the lowest noise mode and when the doubler is disabled.

The maximum allowable REF_{IN} frequency when the doubler is enabled is 30 MHz.

RDIV2

Setting the DB24 bit to 1 inserts a divide-by-2 toggle flip-flop between the R counter and PFD, which extends the maximum REF_{IN} input rate. This function allows a 50% duty cycle signal to appear at the PFD input, which is necessary for cycle slip reduction.

10–Bit R Counter

The 10–bit R counter allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the PFD. Division ratios from 1 to 1023 are allowed.

Double Buffer

DB13 enables or disables double buffering of Bits [DB22:DB20] in Register 4. The Divider Select section explains how double buffering works.

Charge Pump Current Setting

Bits [DB12:DB09] set the charge pump current setting. This should be set to the charge pump current that the loop filter is designed with (see Figure).

LDF

Setting DB8 to 1 enables integer–N digital lock detect, when the FRAC part of the divider is 0; setting DB8 to 0 enables fractional–N digital lock detect.

Lock Detect Precision (LDP)

When DB7 is set to 0, 40 consecutive PFD cycles of 10 ns must occur before digital lock detect is set. When this bit is programmed to 1, 40 consecutive reference cycles of 6 ns must occur before digital lock detect is set. This refers to fractional-N digital lock detect (set DB8 to 0). With integer–N digital lock detect activated (set DB8 to 1), and DB7 set to 0, then five consecutive cycles of 6 ns need to occur before digital lock detect is set. When DB7 is set to 1, five consecutive cycles of 10 ns must occur.

Phase Detector Polarity

DB6 sets the phase detector polarity. When a passive loop filter, or noninverting active loop filter is used, this should be set to 1. If an active filter with an inverting characteristic is used, it should be set to 0.

Power-Down

DB5 provides the programmable power-down mode. Setting this bit to 1 performs a power-down. Setting this bit to 0 returns the synthesizer to normal operation. When in software power-down mode, the part retains all information in its registers. Only if the supply voltages are removed are the register contents lost.

When a power-down is activated, the following events occur:

- The synthesizer counters are forced to their load state conditions.
- The VCO is powered down.
- The charge pump is forced into three-state mode.
- The digital lock detect circuitry is reset.
- The RF_{OUT} buffers are disabled.
- The input register remains active and capable of loading and latching data.

Charge Pump Three-State

DB4 puts the charge pump into three-state mode when programmed to 1. It should be set to 0 for normal operation.

Counter Reset

DB3 is the R counter and N counter reset bit for the ADF4351. When this is 1, the RF synthesizer N counter and R counter are held in reset. For normal operation, this bit should be set to 0.

REGISTER 3

Control Bits

With Bits [C3:C1] set to 0, 1, 1, Register 3 is programmed. Figure shows the input data format for programming this register.

Band Select Clock Mode

Setting DB23 bit to 1 selects a faster logic sequence of band select, suitable for high PFD frequencies, which is necessary for fastlock applications. Setting this bit to 0 is recommended for low PFD values.

Anti-backlash pulse width

Setting DB22 bit to 0 sets the PFD anti-backlash pulse width to 6 ns. This is the recommended mode for fractional-N use. Setting this bit to 1, the 3 ns pulse-width is used and will result in a phase noise and spur improvement in integer-N operation. For fractional-N mode it is not recommended to use this smaller setting.

Charge cancellation mode pulse width

Setting this bit to 1 enables charge pump charge cancellation. This has the effect of reducing PFD spurs in Integer-N mode. In fractional-N mode this should not be used and the relevant result in a phase noise and spur improvement. For fractional-N mode it is not recommended to use this smaller setting.

CSR Enable

Setting DB18 to 1 enables cycle slip reduction. This is a method for improving lock times. Note that the signal at the phase frequency detector (PFD) must have a 50% duty cycle for cycle slip reduction to work. The charge pump current setting must also be set to a minimum. See the Cycle Slip Reduction for Faster Lock Times section for more information.

Clock Divider Mode

Bits [DB16:DB15] must be set to 1, 0 to activate PHASE resync or 0, 1 to activate fast lock. Setting Bits [DB16:DB15] to 0, 0 disables the clock divider. See Figure .

12-Bit Clock Divider Value

The 12-bit clock divider value sets the timeout counter for activation of PHASE resync. See the Phase Resync section for more information. It also sets the timeout counter for fast lock. See the Fast-Lock Timer and Register Sequences section for more information.

REGISTER 4

Control Bits

With Bits [C3:C1] set to 1, 0, 0, Register 4 is programmed. Figure shows the input data format for programming this register.

Feedback Select

DB23 selects the feedback from the VCO output to the N counter. When set to 1, the signal is taken from the VCO directly. When set to 0, it is taken from the output of the output dividers. The dividers enable covering of the wide frequency band (34.375 MHz to 4.4 GHz). When the divider is enabled and the feedback signal is taken from the output, the RF output signals of two separately configured PLLs are in phase. This is useful in some applications where the positive interference of signals is required to increase the power.

Divider Select

Bits [DB22:DB20] select the value of the output divider (see Figure).

Band Select Clock Divider Value

Bits [DB19:DB12] set a divider for the band select logic clock input. The output of the R counter, is by default, the value used to clock the band select logic, but, if this value is too high (>125 kHz), a divider can be switched on to divide the R counter output to a smaller value (see Figure).

VCO Power-Down

DB11 powers the VCO down or up depending on the chosen value.

Mute Till Lock Detect

If DB10 is set to 1, the supply current to the RF output stage is shut down until the part achieves lock as measured by the digital lock detect circuitry.

AUX Output Select

DB9 sets the auxiliary RF output. The selection can be either the output of the RF dividers or fundamental VCO frequency.

AUX Output Enable

DB8 enables or disables auxiliary RF output, depending on the chosen value.

AUX Output Power

Bits [DB7:DB6] set the value of the auxiliary RF output power level (see Figure).

RF Output Enable

DB5 enables or disables primary RF output, depending on the chosen value.

Output Power

Bits [DB4:DB3] set the value of the primary RF output power level (see Figure).

REGISTER 5

Control Bits

With Bits [C3:C1] set to 1, 0, 1, Register 5 is programmed. Figure shows the input data form for programming this register.

Lock Detect Pin Operation

Bits [DB23:DB22] set the operation of the lock detect pin (see Figure).

INITIALIZATION SEQUENCE

The following sequence of registers is the correct sequence for initial power-up of the ADF4351 after the correct application of voltages to the supply pins:

- Register 5
- Register 4
- Register 3
- Register 2
- Register 1
- Register 0

RF SYNTHESIZER—A WORKED EXAMPLE

The following is an example how to program the ADF4351 synthesizer:

$$RF_{OUT} = [INT + (FRAC/MOD)] \times [f_{PFD}]/RF\ divider \quad (3)$$

where:
RF_{OUT} is the RF frequency output.
INT is the integer division factor.
FRAC is the fractionality.
MOD is the modulus.
RF divider is the output divider that divides down the VCO frequency.

$$f_{PFD} = REF_{IN} \times [(1 + D)/(R \times (1+T))] \quad (4)$$

where:
REF_{IN} is the reference frequency input.
D is the RF REF_{IN} doubler bit.
T is the reference divide-by-2 bit (0 or 1).
R is the RF reference division factor.

For example, in a UMTS system, where 2112.6 MHz RF frequency output (RF_{OUT}) is required, a 10 MHz reference frequency input (REF_{IN}) is available, and a 200 kHz channel resolution (f_{RESOUT}) is required on the RF output. Note that the ADF4351 operates in the frequency range of 2.2 GHz to 4.4 GHz. Therefore, the RF divider of 2 should be used (VCO frequency = 4225.2 MHz, RF_{OUT} = VCO frequency/RF divider = 4225.2 MHz/2 = 2112.6 MHz).

It is also important where the loop is closed. In this example, the loop is closed (see Figure).

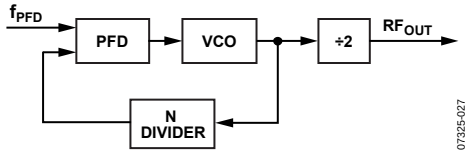


Figure 30. Loop Closed Before Output Divider

Channel resolution (f_{RESOUT}) or 200 kHz is required at the output of the RF divider. Therefore, channel resolution at the output of the VCO (f_{RES}) is to be twice the f_{RESOUT}, that is 400 kHz.

$MOD = REF_{IN}/f_{RES}$
MOD = 10 MHz/400 kHz = 25

From Equation 4,

$$f_{PFD} = [10\ MHz \times (1 + 0)/1] = 10\ MHz \quad (5)$$

$$2112.6\ MHz = 10\ MHz \times (INT + FRAC/25)/2 \quad (6)$$

where:
INT = 422
FRAC = 13

MODULUS

The choice of modulus (MOD) depends on the reference signal (REF_{IN}) available and the channel resolution (f_{RES}) required at the RF output. For example, a GSM system with 13 MHz REF_{IN} sets the modulus to 65. This means the RF output resolution (f_{RES}) is the 200 kHz (13 MHz/65) necessary for GSM. With dither off, the fractional spur interval depends on the modulus values chosen (see Table 6).

REFERENCE DOUBLER AND REFERENCE DIVIDER

The reference doubler on-chip allows the input reference signal to be doubled. This is useful for increasing the PFD comparison frequency. Making the PFD frequency higher improves the noise performance of the system. Doubling the PFD frequency usually improves noise performance by 3 dB. It is important to note that the PFD cannot operate above 32 MHz due to a limitation in the speed of the Σ-Δ circuit of the N-divider.

The reference divide-by-2 divides the reference signal by 2, resulting in a 50% duty cycle PFD frequency. This is necessary for the correct operation of the cycle slip reduction (CSR) function. See the Cycle Slip Reduction for Faster Lock Times section for more information.

12-BIT PROGRAMMABLE MODULUS

Unlike most other fractional-N PLLs, the ADF4351 allows the user to program the modulus over a 12–bit range. This means the user can set up the part in many different configurations for the application, when combined with the reference doubler and the 10-bit R counter.

For example, consider an application that requires 1.75 GHz RF and 200 kHz channel step resolution. The system has a 13 MHz reference signal.

One possible setup is feeding the 13 MHz directly to the PFD and programming the modulus to divide by 65. This results in the required 200 kHz resolution.

Another possible setup is using the reference doubler to create 26 MHz from the 13 MHz input signal. This 26 MHz is then fed into the PFD programming the modulus to divide by 130. This also results in 200 kHz resolution and offers superior phase noise performance over the previous setup.

The programmable modulus is also very useful for multi-standard applications. If a dual-mode phone requires PDC and GSM 1800 standards, the programmable modulus is a great benefit. PDC requires 25 kHz channel step resolution, whereas GSM 1800 requires 200 kHz channel step resolution.

A 13 MHz reference signal can be fed directly to the PFD, and the modulus can be programmed to 520 when in PDC mode (13 MHz/520 = 25 kHz).

The modulus needs to be reprogrammed to 65 for GSM 1800 operation (13 MHz/65 = 200 kHz).

It is important that the PFD frequency remain constant (13 MHz). This allows the user to design one loop filter for both setups without running into stability issues. It is important to remember that the ratio of the RF frequency to the PFD frequency principally affects the loop filter design, not the actual channel spacing.

CYCLE SLIP REDUCTION FOR FASTER LOCK TIMES

As outlined in the Low Noise and Low Spur Mode section, the ADF4351 contains a number of features that allow optimization for noise performance. However, in fast locking applications, the loop bandwidth generally needs to be wide, and therefore, the filter does not provide much attenuation of the spurs. If the cycle slip reduction feature is enabled, the narrow loop bandwidth is maintained for spur attenuation but faster lock times are still possible.

Cycle Slips

Cycle slips occur in integer-N/fractional-N synthesizers when the loop bandwidth is narrow compared to the PFD frequency. The phase error at the PFD inputs accumulates too fast for the PLL to correct, and the charge pump temporarily pumps in the wrong direction. This slows down the lock time dramatically. The ADF4351 contains a cycle slip reduction feature that extends the linear range of the PFD, allowing faster lock times without modifications to the loop filter circuitry.

When the circuitry detects that a cycle slip is about to occur, it turns on an extra charge pump current cell. This outputs a constant current to the loop filter, or removes a constant current from the loop filter (depending on whether the VCO tuning voltage needs to increase or decrease to acquire the new frequency). The effect is that the linear range of the PFD is increased. Loop stability is maintained because the current is constant and is not a pulsed current.

If the phase error increases again to a point where another cycle slip is likely, the ADF4351 turns on another charge pump cell. This continues until the ADF4351 detects the VCO frequency has gone past the desired frequency. The extra charge pump cells are turned off one by one until all the extra charge pump cells have been disabled and the frequency is settled with the original loop filter bandwidth.

Up to seven extra charge pump cells can be turned on. In most applications, it is enough to eliminate cycle slips altogether, giving much faster lock times.

Setting Bit DB18 in the Register 3 to 1 enables cycle slip reduction. Note that the PFD requires a 45% to 55% duty cycle for CSR to operate correctly. If the REF_{IN} frequency does not have a suitable duty cycle, the RDIV2 mode ensures that the input to the PFD has a 50% duty cycle.

SPURIOUS OPTIMIZATION AND FAST LOCK

Narrow loop bandwidths can filter unwanted spurious signals, but these usually have a long lock time. A wider loop bandwidth will achieve faster lock times, but a wider loop bandwidth may lead to increased spurious signals inside the loop bandwidth.

The fast lock feature can achieve the same fast lock time as the wider bandwidth, but with the advantage of a narrow final loop bandwidth to keep spurs low.

FAST-LOCK TIMER AND REGISTER SEQUENCES

If the fast-lock mode is used, a timer value is to be loaded into the PLL to determine the duration of the wide bandwidth mode.

When Bits [DB16:DB15] in Register 3 are set to 0, 1 (fast-lock enable), the timer value is loaded by the 12–bit clock divider value. The following sequence must be programmed to use fast lock:

1. Initialization sequence (see the Initialization Sequence section) occurs only once after powering up the part.
2. Load Register 3 by setting Bits [DB16:DB15] to 0, 1 and the chosen fast-lock timer value [DB14:DB3]. Note that the duration the PLL remains in wide bandwidth is equal to the fast-lock timer/f_{PFD}.

FAST LOCK—AN EXAMPLE

If a PLL has reference frequencies of 13 MHz and f_{PFD} = 13 MHz and a required lock time of 50 µs, the PLL is set to wide bandwidth for 30 µs. This example assumes a modulus of 65 for channel spacing of 200 kHz. We also need to allow for the VCO calibration time, which takes 10 µs (achieved by programming the higher band select speed in Register 3).

If the time set for the PLL lock time in wide bandwidth is 30 µs, then

Fast-Lock Timer Value = (VCO band select time +PLL Lock Time in Wide Bandwidth) × f_{PFD}/*MOD*

Fast-Lock Timer Value = (10 + 30)µs × 13 MHz/65 = 8

Therefore, a value of 8 must be loaded into the clock divider value in Register 3 in Step 1 of the sequence described in the Fast-Lock Timer and Register Sequences section.

FAST LOCK—LOOP FILTER TOPOLOGY

To use fast-lock mode, the damping resistor in the loop filter is reduced to ¼ of its value while in wide bandwidth mode. To achieve the wider loop filter bandwidth, the charge pump current increases by a factor of 16 and to maintain loop stability the damping resistor must be reduced a factor of ¼. To enable fast lock, the SW pin is shorted to the GND pin by settings Bits [DB16:DB15] in Register 3 to 0, 1. The following two topologies are available:

- The damping resistor (R1) is divided into two values (R1 and R1A) that have a ratio of 1:3 (see Figure).
- An extra resistor (R1A) is connected directly from SW, as shown in Figure . The extra resistor is calculated such that the parallel combination of an extra resistor and the damping resistor (R1) is reduced to ¼ of the original value of R1 (see Figure).

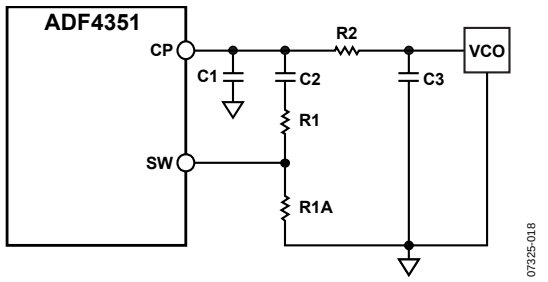


Figure 31. Fast-Lock Loop Filter Topology—Topology 1

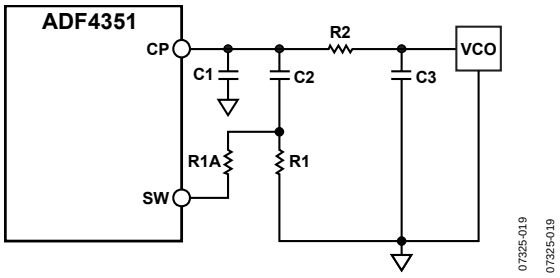


Figure 32. Fast-Lock Loop Filter Topology—Topology 2

SPUR MECHANISMS

This section describes the three different spur mechanisms that arise with a fractional-N synthesizer and how to minimize them in the ADF4351.

Fractional Spurs

The fractional interpolator in the ADF4351 is a third-order Σ-Δ modulator (SDM) with a modulus (MOD) that is programmable to any integer value from 2 to 4095. In low spur mode (dither enabled) the minimum allowable value of MOD is 50. The SDM is clocked at the PFD reference rate (f_{PFD}) that allows PLL output frequencies to be synthesized at a channel step resolution of f_{PFD}/MOD.

In low noise mode (dither disabled) the quantization noise from the Σ-Δ modulator appears as fractional spurs. The interval between spurs is f_{PFD}/L, where L is the repeat length of the code sequence in the digital Σ-Δ modulator. For the third-order modulator used in the ADF4351, the repeat length depends on the value of MOD, as listed in Table 6.

Table 6. Fractional Spurs with Dither Disabled

Condition (Dither Disabled)	Repeat Length	Spur Interval
If MOD is divisible by 2, but not 3	2 × MOD	Channel step/2
If MOD is divisible by 3, but not 2	3 × MOD	Channel step/3
If MOD is divisible by 6	6 × MOD	Channel step/6
Otherwise	MOD	Channel step

In low spur mode (dither enabled), the repeat length is extended to 2^{21} cycles, regardless of the value of MOD, which makes the quantization error spectrum look like broadband noise. This may degrade the in-band phase noise at the PLL output by as much as 10 dB. For lowest noise, dither disabled is a better choice, particularly when the final loop bandwidth is low enough to attenuate even the lowest frequency fractional spur.

Integer Boundary Spurs

Another mechanism for fractional spur creation is the interactions between the RF VCO frequency and the reference frequency. When these frequencies are not integer related (the point of a fractional-N synthesizer) spur sidebands appear on the VCO output spectrum at an offset frequency that corresponds to the beat note or difference frequency between an integer multiple of the reference and the VCO frequency. These spurs are attenuated by the loop filter and are more noticeable on channels close to integer multiples of the reference where the difference frequency can be inside the loop bandwidth, therefore, the name integer boundary spurs.

Reference Spurs

Reference spurs are generally not a problem in fractional-N synthesizers because the reference offset is far outside the loop bandwidth. However, any reference feed-through mechanism that bypasses the loop may cause a problem. Feed through of low levels of on-chip reference switching noise, through the RF_{IN} pin back to the VCO, can result in reference spur levels as high as –90 dBc. PCB layout needs to ensure adequate isolation between VCO traces and the input reference to avoid a possible feed through path on the board.

SPUR CONSISTENCY AND FRACTIONAL SPUR OPTIMIZATION

With dither off, the fractional spur pattern due to the quantization noise of the SDM also depends on the particular phase word with which the modulator is seeded.

The phase word can be varied to optimize the fractional and subfractional spur levels on any particular frequency. Thus, a look-up table of phase values corresponding to each frequency can be constructed for use when programming the ADF4351.

If a look-up table is not used, keep the phase word at a constant value to ensure consistent spur levels on any particular frequency.

PHASE RESYNC

The output of a fractional-N PLL can settle to any one of the MOD phase offsets with respect to the input reference, where MOD is the fractional modulus. The phase resync feature in the ADF4351 produces a consistent output phase offset with respect to the input reference. This is necessary in applications where the output phase and frequency are important, such as digital beam forming. See the Phase Programmability section to program a specific RF output phase when using phase resync.

Phase resync is enabled by setting Bits [DB16:DB15] in Register 3 to 1, 0. When phase resync is enabled, an internal timer generates sync signals at intervals of t_{SYNC} given by the following formula:

$$t_{SYNC} = CLK\_DIV\_VALUE \times MOD \times t_{PFD}$$

where:
t_{PFD} is the PFD reference period.
CLK_DIV_VALUE is the decimal value programmed in Bits [DB14:DB3] of Register 3 and can be any integer in the range of 1 to 4095.
MOD is the modulus value programmed in Bits [DB14:DB3] of Register 1 (R1).

When a new frequency is programmed, the second sync pulse after the LE rising edge is used to resynchronize the output phase to the reference. The t_{SYNC} time is to be programmed to a value that is as least as long as the worst-case lock time. This guarantees the phase resync occurs after the last cycle slip in the PLL settling transient.

In the example shown in Figure , the PFD reference is 25 MHz and MOD = 125 for a 200 kHz channel spacing. t_{SYNC} is set to 400 µs by programming CLK_DIV_VALUE = 80.

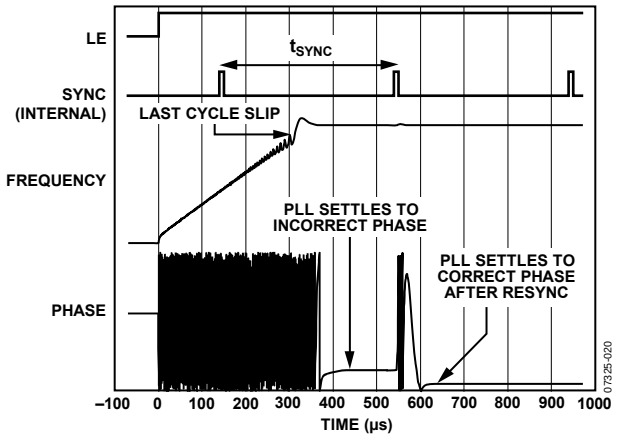


Figure 33. Phase Resync Example

Phase Programmability

The phase word in Register 1 controls the RF output phase. As this word is swept from 0 to MOD, the RF output phase sweeps over a 360° range in steps of 360°/MOD.

APPLICATIONS INFORMATION

DIRECT CONVERSION MODULATOR

Direct conversion architectures are increasingly being used to implement base station transmitters. Figure shows how Analog Devices, Inc., parts can be used to implement such a system.

Figure 34 shows the AD9761 TxDAC® being used with the ADL5375. The use of dual integrated DACs, such as the AD9788 with its specified ±0.02 dB and ±0.001 dB gain and offset matching characteristics, ensures minimum error contribution (over temperature) from this portion of the signal chain.

The local oscillator (LO) is implemented using the ADF4351. The low-pass filter was designed using ADIsimPLL™ for a channel spacing of 200 kHz and a closed-loop bandwidth of 35 kHz.

The LO ports of the ADL5375 can be driven differentially from the complementary $RF_{OUT}A$ and $RF_{OUT}B$ outputs of the ADF4351. This gives better performance than a single-ended LO driver and eliminates the use of a balun to convert from a single-ended LO input to the more desirable differential LO input for the ADL5375. The typical rms phase noise (100 Hz to 5 MHz) of the LO in this configuration is 0.61°rms.

The AD8349 accepts LO drive levels from −10 dBm to 0 dBm. The optimum LO power can be software programmed on the ADF4351, which allows levels from −4 dBm to +5 dBm from each output.

The RF output is designed to drive a 50 Ω load, but must be ac-coupled, as shown in Figure . If the I and Q inputs are driven in quadrature by 2 V p-p signals, the resulting output power from the modulator is approximately 2 dBm.

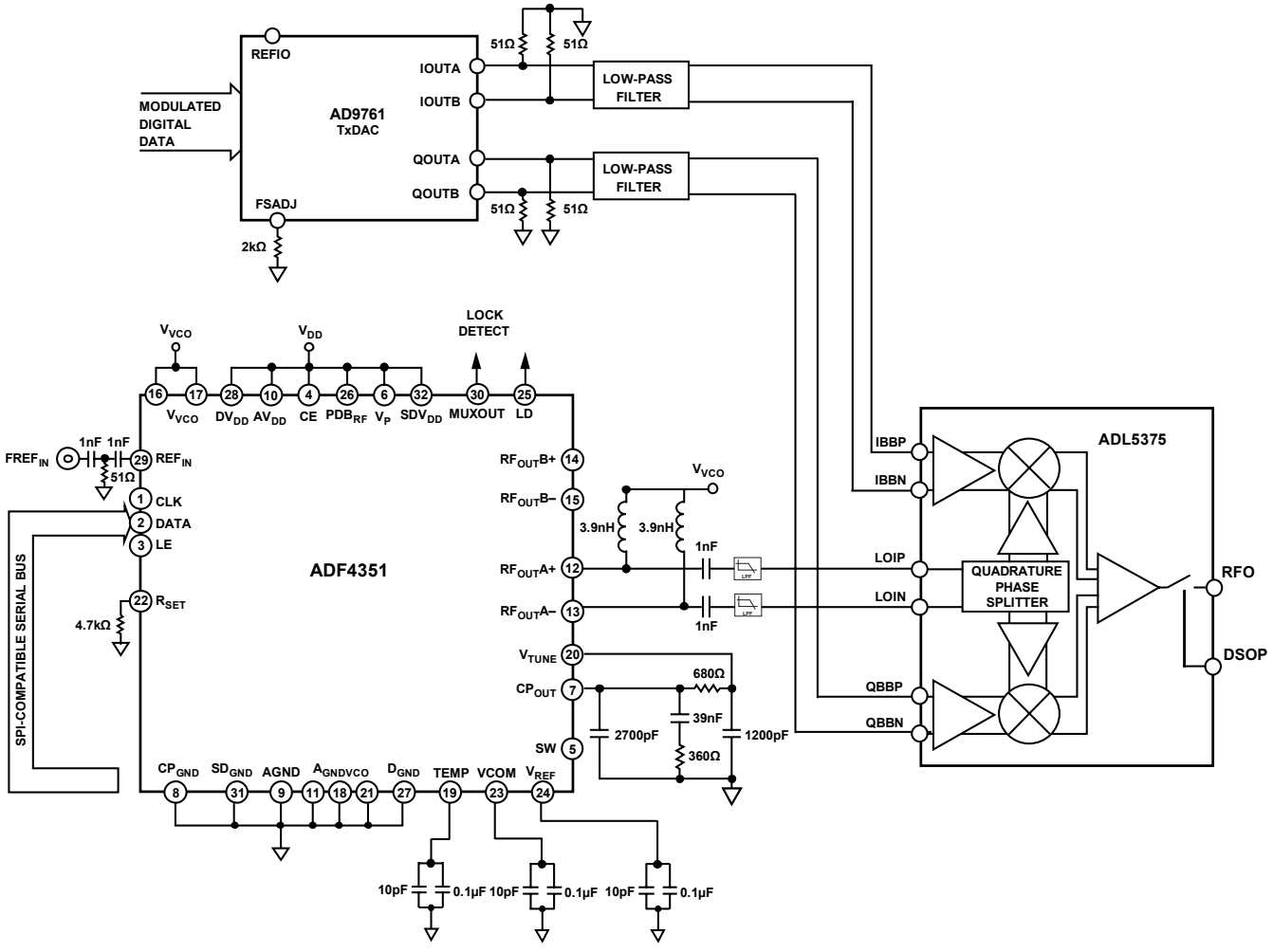


Figure 34. Direct Conversion Modulator

INTERFACING

The ADF4351 has a simple SPI-compatible serial interface for writing to the device. CLK, DATA, and LE control the data transfer. When LE goes high, the 32 bits that have been clocked into the appropriate register on each rising edge of CLK are transferred to the appropriate latch. See Figure 2 for the timing diagram and Table 5 for the register address table.

ADuC812 Interface

Error! Reference source not found. Figure 35 shows the interface between the ADF4351 and the ADuC70xx family of analog microcontrollers. The ADuC70xx family is based on an AMR7 core, although the same interface can be used with any 8051-based microcontroller. The microcontroller is set up for SPI master mode with CPHA = 0. To initiate the operation, the I/O port driving LE is brought low. Each latch of the ADF4351 needs a 32-bit word. This is accomplished by writing four 8-bit bytes from the microcontroller to the device. When the last byte is written, the LE input should be brought high to complete the transfer.

On first applying power to the ADF4351, it needs six writes (one each to R5, R4, R3, R2, R1, R0) for the output to become active.

I/O port lines on the microcontroller are also used to control power-down (CE input) and to detect lock (MUXOUT configured as lock detect and polled by the port input).

When operating in the mode described, the maximum SPI transfer rate of the ADuC7023 is 20Mbps. This means that the maximum rate at which the output frequency can be changed is 833 kHz. If using a faster SPI clock just make sure the SPI timing requirements listed in Table 2 are adhered to.

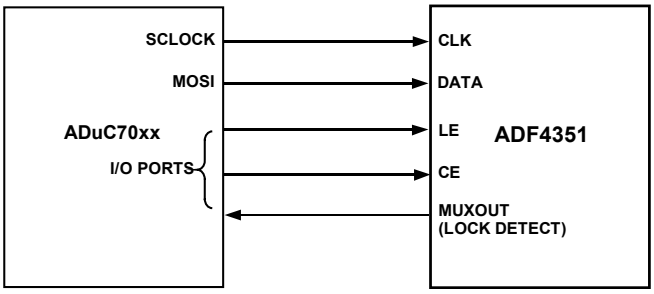


Figure 35. ADuC7020-to-ADF4351 Interface

ADSP-21xx Interface

Figure 36 shows the interface between the ADF4351 and the Blackfin ADSP-BF527 digital signal processor (DSP). The ADF4351 needs a 32-bit serial word for each latch write. The easiest way to accomplish this using the Blackfin family is to use the autobuffered transmit mode of operation with alternate framing. This provides a means for transmitting an entire block of serial data before an interrupt is generated. Set up the word length for 8 bits and use three memory locations for each 32-bit word. To program each 32-bit latch, store the four 8-bit bytes, enable the autobuffered mode, and write to the transmit register of the DSP. This last operation initiates the autobuffer transfer. As in the microcontroller case just make sure the clock speeds are within the maximum limits outlined in table 2.

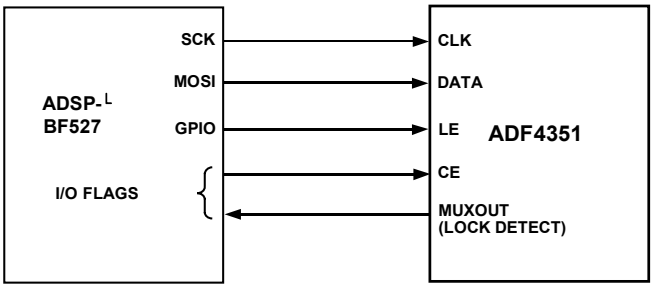


Figure 36. ADSP-BF527-to-ADF4351 Interface

PCB DESIGN GUIDELINES FOR A CHIP SCALE PACKAGE

The lands on the chip scale package (CP-32-2) are rectangular. The PCB pad for these is to be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land is to be centered on the pad. This ensures the solder joint size is maximized. The bottom of the chip scale package has a central thermal pad.

The thermal pad on the PCB is to be at least as large as the exposed pad. On the PCB, there is to be a minimum clearance of 0.25 mm between the thermal pad and the inner edges of the pad pattern. This ensures that shorting is avoided.

Thermal vias can be used on the PCB thermal pad to improve the thermal performance of the package. If vias are used, they are to be incorporated in the thermal pad at 1.2 mm pitch grid. The via diameter is to be between 0.3 mm and 0.33 mm, and the via barrel is to be plated with 1 oz. of copper to plug the via.

OUTPUT MATCHING

There are a number of ways to match the output of the ADF4351 for optimum operation; the most basic is to use a 50 Ω resistor to V_{VCO}. A dc bypass capacitor of 100 pF is connected in series as shown in Figure . Because the resistor is not frequency dependent, this provides a good broadband match. Placing the output power in this circuit into a 50 Ω load typically gives values chosen by Bit D2 and Bit D1 in Register 4 (R4).

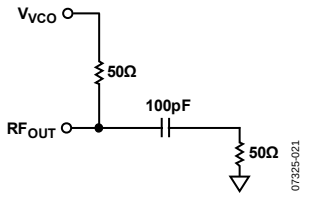


Figure 37. Simple ADF4351 Output Stage

A better solution is to use a shunt inductor (acting as an RF choke) to V_{VCO}. This gives a better match and, therefore, more output power.

Experiments have shown the circuit shown in Figure provides an excellent match to 50 Ω for the W-CDMA UMTS Band 1 (2110 MHz to 2170 MHz). The maximum output power in that case is about 5 dBm. Both single-ended architectures can be examined using the EVAL-ADF4351EB1Z evaluation board.

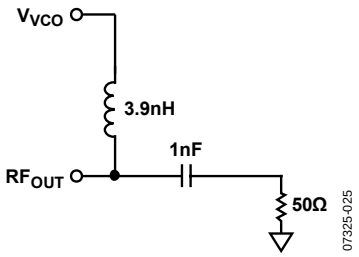


Figure 38.Optimum ADF4351 Output Stage

If differential outputs are not needed, the unused output can be terminated or combined with both outputs using a balun.

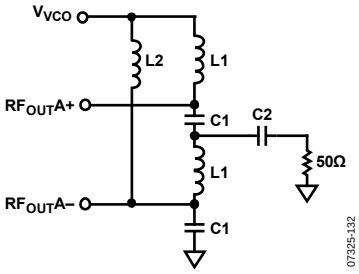


Figure 39. ADF4351 LC Balun

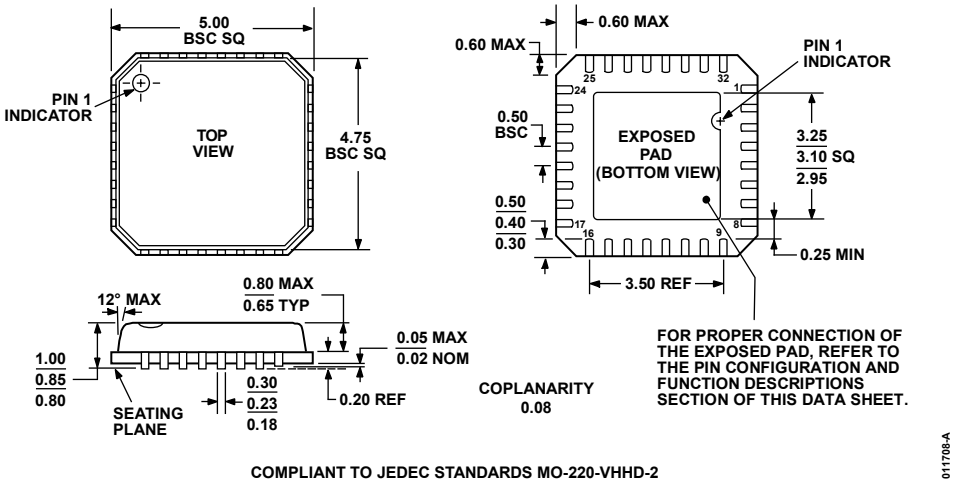
A balun using discrete inductors and capacitors may be implemented with the architecture in Figure .

Component L1 and Component C1 comprise the LC balun, L2 provides a dc path for $RF_{OUT}A–$, and Capacitor C2 is used for dc blocking.

Table 7. LC Balun Components

Frequency Range (MHz)	Inductor L1 (nH)	Capacitor C1 (pF)	RF Choke Inductor (nH)	DC Blocking Capacitor (pF)	Measured Output Power (dBm)
137 to 300	100	10	390	1000	9
300 to 460	51	5.6	180	120	10
400 to 600	30	5.6	120	120	10
600 to 900	18	4	68	120	10
860 to 1240	12	2.2	39	10	9
1200 to 1600	5.6	1.2	15	10	9
1600 to 3600	3.3	0.7	10	10	8
2800 to 3800	2.2	0.5	10	10	8

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-2

Figure 40. 32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
5 mm × 5 mm Body, Very Thin Quad
(CP-32-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADF4351BCPZ[1]	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-2
ADF4351BCPZ-RL7[1]	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-2
EVAL-ADF4351EB1Z[1]		Evaluation Board	

[1] Z = RoHS Compliant Part.

PR09800-0-3/11(PrC)