203-361

# Am27S33/27S33A

4,096-Bit (1024x4) Bipolar PROM

Advanced Micro Devices

## DISTINCTIVE CHARACTERISTICS

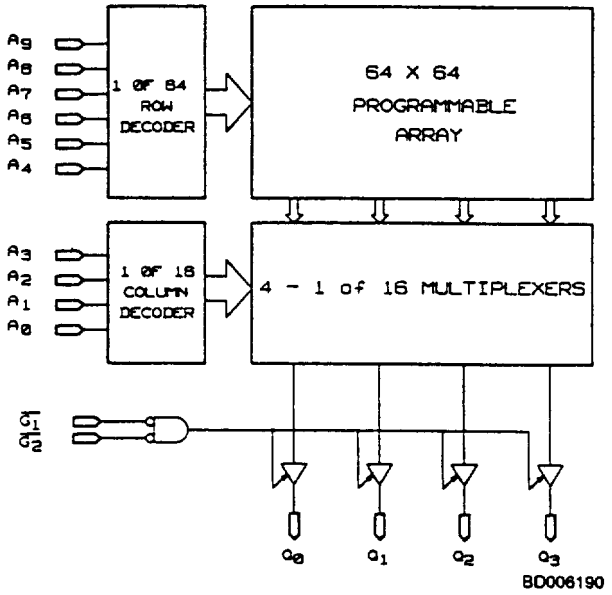
- High speed
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low-current PNP inputs
- High-current open-collector and three-state outputs
- Fast chip select

## GENERAL DESCRIPTION

The Am27S33 (1024 words by 4 bits) is a Schottky TTL Programmable Read-Only Memory (PROM).

This device is available in three-state (Am27S33) output versions. These outputs are compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls, mapping functions, code conversion, or logic replacement. Easy word-depth expansion is facilitated by active LOW ($\overline{G_1}$ & $\overline{G_2}$) output enables.

## BLOCK DIAGRAM




## PRODUCT SELECTOR GUIDE

| Three-State Part Number | Am27S33A | | Am27S33 | |
|---|---|---|---|---|
| Address Access Time | 35 ns | 45 ns | 55 ns | 70 ns |
| Operating Range | C | M | C | M |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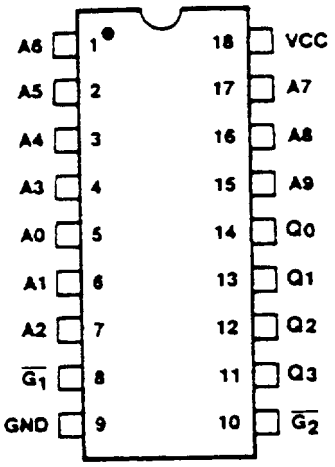
## CONNECTION DIAGRAMS
Top View

DIPs*

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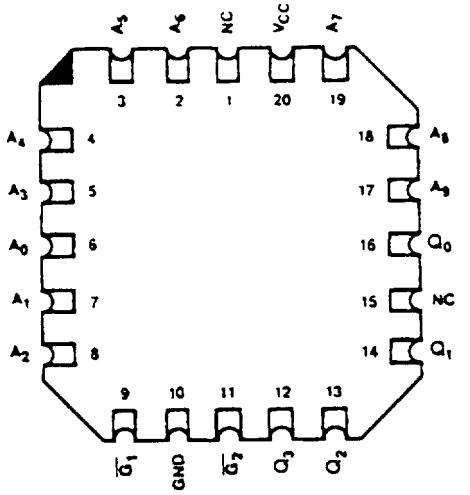
LCC**

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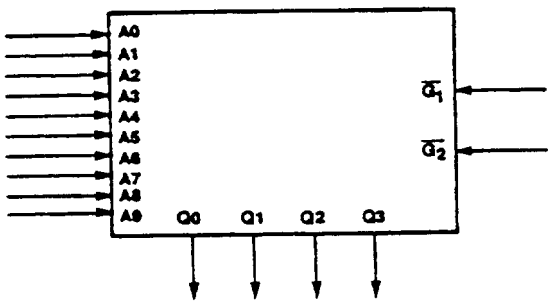
*Also available in 18-pin Flatpack. Pinout identical to DIPs.
**Also available in a 20-pin square PLCC. Pinout identical to LCC.

Note: Pin 1 is marked for orientation.

## LOGIC SYMBOL

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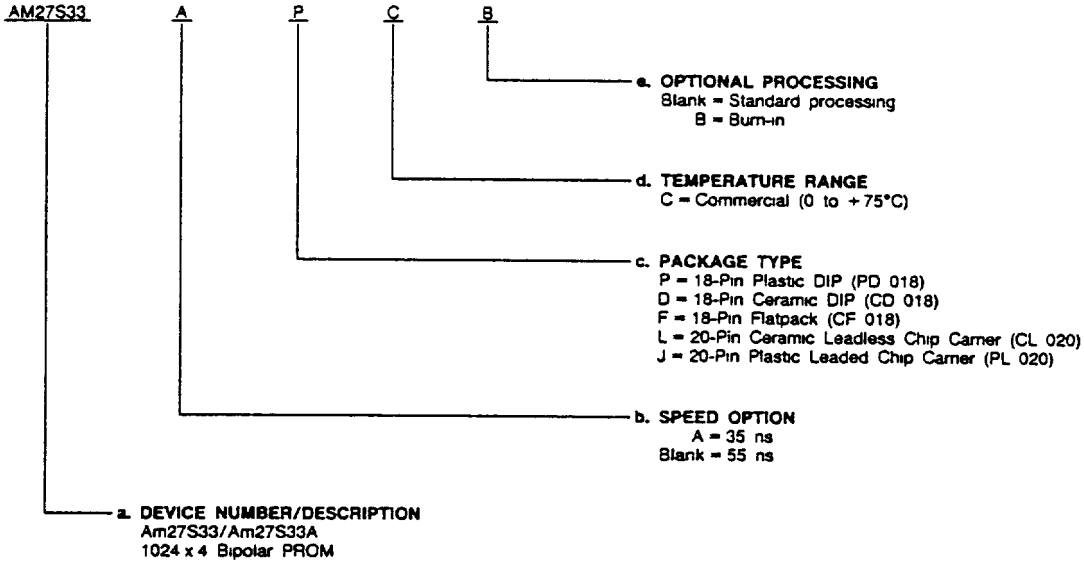
## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
**b. Speed Option** (if applicable)
**c. Package Type**
**d. Temperature Range**
**e. Optional Processing**




| Valid Combinations | |
|---|---|
| AM27S33 | PC, PCB, DC, DCB, FC, FCB, LC, LCB, JC, JCB |
| AM27S33A | |

**Valid Combinations**

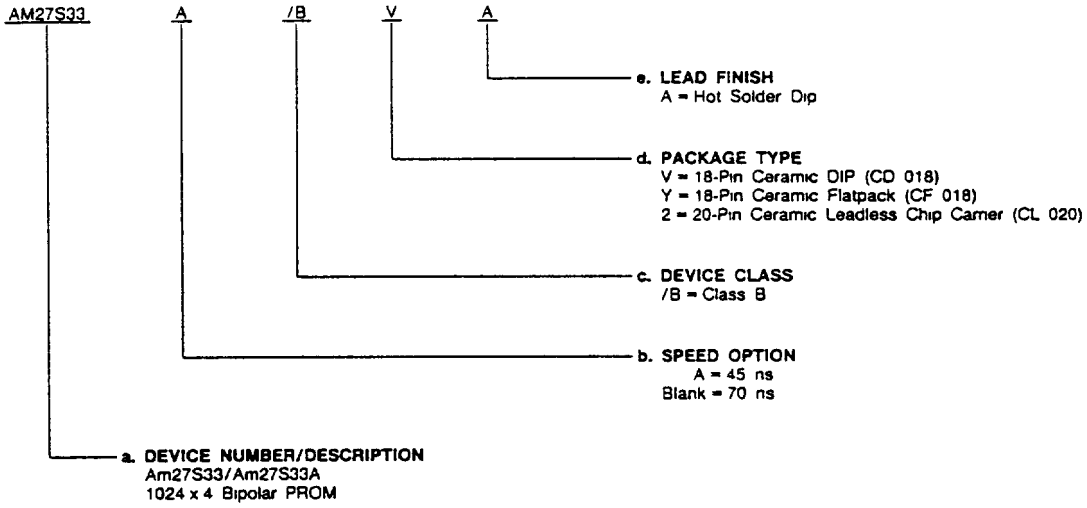
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

5

## MILITARY ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
**b. Speed Option** (if applicable)
**c. Device Class**
**d. Package Type**
**e. Lead Finish**




| Valid Combinations | |
|---|---|
| AM27S33 | /BVA, /BYA, /B2A |
| AM27S33A | |

**Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

**Group A Tests**

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

## MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

## PIN DESCRIPTION

**$A_0 - A_9$ Address Inputs**
The 10-bit field presented at the address inputs selects one of 1024 memory locations to be read from.

**$Q_0 - Q_3$ Data Output Port**
The outputs whose state represents the data read from the selected memory locations.

**$\overline{G_1}, \overline{G_2}$ Output Enable**
Provides direct control of the Q-output buffers. Outputs disabled forces all open-collector outputs to an OFF state and all three-state outputs to a floating or high-impedance state.

$$\text{Enable} = \overline{G_1} \cdot \overline{G_2}$$

$$\text{Disable} = \overline{\overline{G_1} \cdot \overline{G_2}} = G_1 + G_2$$

**$V_{CC}$ Device Power Supply Pin**
The most positive of the logic power supply pins.

**GND Device Power Supply Pin**
The most negative of the logic power supply pins.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... ..... . ..-65 to +150°C
Ambient Temperature with
Power Applied. ..... . .... ..... -55 to +125°C
Supply Voltage. . ..... .... . ..... ...-0 5 V to +7 0 V
DC Voltage Applied to Outputs
(Except During Programming)..... -0.5 V to +$V_{CC}$ Max.
DC Voltage Applied to Outputs
During Programming ..... .... . .... 21 V
Output Current into Outputs During
Programming (Max Duration of 1 sec) . ... ..... 250 mA
DC Input Voltage ..... ..... .....-0 5 V to +5 5 V
DC Input Current .. ... .....-30 mA to +5 mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Ambient Temperature ($T_A$) . ... . .. .0 to +75°C
Supply Voltage ($V_{CC}$) . . +475 V to +5 25 V

Military (M) Devices*
Case Temperature ($T_C$) .... . ..... ...-55 to +125°C
Supply Voltage ($V_{CC}$) ... .. ..... +4.5 V to +5 5 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

*Military Product 100% tested at $T_C$ = +25°C, +125°C, and -55°C.

## DC CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

| Parameter Symbol | Parameter Description | Test Conditions | | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min., $I_{OH}$ = -2.0 mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | 2.4 | | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min., $I_{OL}$ = 16 mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | | 0.45 | V |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs (Note 1) | | | 2.0 | | | V |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs (Note 1) | | | | | 0.8 | V |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = Max., $V_{IN}$ = 0.45 V | | | | | -0 250 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = Max., $V_{IN}$ = 2.7 V | | | | | 25 | µA |
| $I_{SC}$ (Note 1) | Output Short-Circuit Current | $V_{CC}$ = Max., $V_{OUT}$ = 0 0 V (Note 2) | | | -20 | | -90 | mA |
| $I_{CC}$ | Power Supply Current | All inputs = GND,<br>$V_{CC}$ = Max. | | COM'L | | | 140 | mA |
| | | | | MIL | | | 145 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min., $I_{IN}$ = -18 mA | | | | | -1 2 | V |
| $I_{CEX}$ | Output Leakage Current | $V_{CC}$ = Max.,<br>$V_{G_1}$ = 2.4 V | | $V_O$ = $V_{CC}$ | | | 40 | µA |
| | | | (Note 1) | $V_O$ = 2.4 V | | | 40 | |
| | | | | $V_O$ = 0.4 V | | | -40 | |
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0 V @ f = 1 MHz (Note 3)<br>$V_{CC}$ = 5 V, $T_A$ = 25°C | | | | 5 | | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0 V @ f = 1 MHz (Note 3)<br>$V_{CC}$ = 5 V, $T_A$ = 25°C | | | | 8 | | |

Notes: 1. $V_{IL}$ and $V_{IH}$ are input conditions of output tests and are not themselves directly tested. $V_{IL}$ and $V_{IH}$ are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise Do not attempt to test these values without suitable equipment.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

## SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted*)

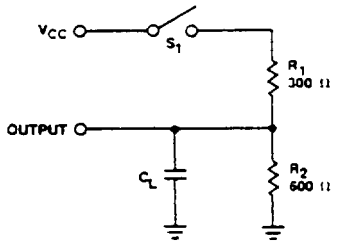
| No. | Parameter Symbol | Parameter Description | Am27S33A | | | | Am27S33 | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | COM'L | | MIL | | COM'L | | MIL | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| 1 | TAVQV | Address Valid to Output Valid Access Time | | 35 | | 45 | | 55 | | 70 | ns |
| 2 | TGVQZ | Delay from Output Enable Valid to Output Hi-Z | | 20 | | 25 | | 25 | | 30 | ns |
| 3 | TGVQV | Delay from Output Enable Valid to Output Valid | | 20 | | 25 | | 25 | | 30 | ns |

See also Switching Test Circuit.

Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3 0 V.

*Subgroups 7 and 8 apply to functional tests.

## SWITCHING TEST CIRCUIT

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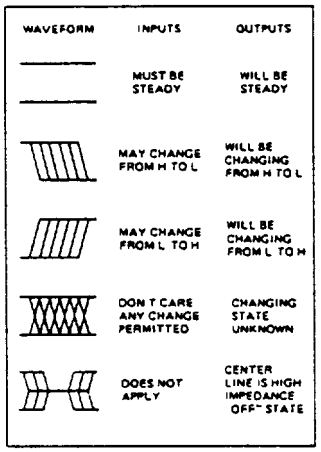
Notes. 1 TAVQV is tested with switch $S_1$ closed and $C_L = 50$ pF
2 For three-state outputs, TGVQV is tested with $C_L = 50$ pF to the 1.5 V level; $S_1$ is open for high impedance to HIGH tests and closed for high impedance to LOW tests TGVQZ is tested with $C_L = 5$ pF HIGH to high-impedance tests are made with $S_1$ open to an output voltage of steady state HIGH −0.5 V; LOW to high-impedance tests are made with $S_1$ closed to the steady state LOW +0.5 V level.

## SWITCHING WAVEFORMS

### KEY TO SWITCHING WAVEFORM

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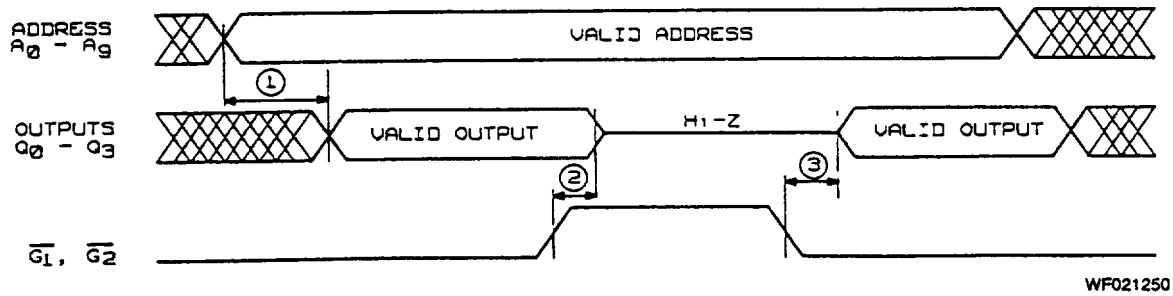


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