AP603

High Dynamic Range 7W 28V HBT Amplifier

Product Features

- 800 – 2200 MHz
- +38.5 dBm P1dB
- -50 dBc ACLR @ 1W P_{AVG}
- -51 dBc IMD3 @ 1W PEP
- 15% Efficiency @ 1W P_{AVG}
- Internal Active Bias
- Internal Temp Compensation
- Capable of handling 7:1 VSWR @ 28 Vcc, 2.14 GHz, 5.5W CW Pout
- Lead-free/RoHS-compliant 5x6 mm power DFN package

Applications

- Mobile Infrastructure
- High Power Amplifier (HPA)

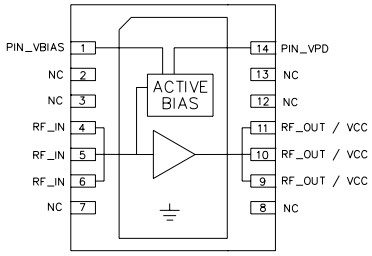
Product Description

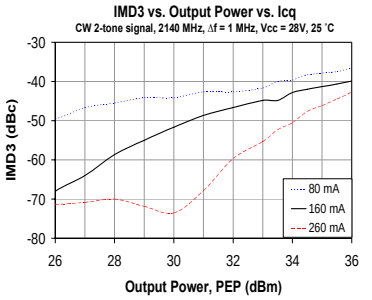
The AP603 is a high dynamic range power amplifier in a lead-free/RoHS-compliant 5x6mm power DFN SMT package. The single stage amplifier has excellent backoff linearity, while being able to achieve high performance for 800-2200 MHz applications with up to +38.5 dBm of compressed 1dB power.

The AP603 uses a high reliability, high voltage InGaP/GaAs HBT process technology. The device incorporates proprietary bias circuitry to compensate for variations in linearity and current draw over temperature. The module does not require any negative bias voltage; an internal active bias allows the AP603 to operate directly off a commonly used high voltage supply (typically +24 to +32V). An added feature allows the quiescent bias to be adjusted externally to meet specific system requirements.

The AP603 is targeted for use as a pre-driver and driver stage amplifier in wireless infrastructure where high linearity and high efficiency is required. This combination makes the device an excellent candidate for next generation multi-carrier 3G mobile infrastructure.

Functional Diagram





Specifications

W-CDMA 3GPP Test Model 1+64 DPCH, 60% clipping, PAR = 8.6 dB @ 0.01% Probability, 3.84 MHz BW, Vcc = +28V, Icq = 160 mA

Parameter	Units	Min	Typ	Max
Operational Bandwidth	MHz	800		2200
Test Frequency	MHz		2140	
Output Channel Power	dBm		+30	
Power Gain	dB		11.8	
Input Return Loss	dB		10	
Output Return Loss	dB		8.2	
ACLR	dBc		-50	
IMD3 @ +30 dBm PEP	dBc		-51	
PIN_VPD Current, Ipd	mA		4	
Operating Current, Icc	mA		246	
Collector Efficiency	%		14.6	
Output P1dB	dBm		+38.2	
Quiescent Current, Icq	mA		160	
Vpd, Vbias	V		+5	
Vcc	V		+28	

Typical Performance

W-CDMA 3GPP Test Model 1+64 DPCH, 60% clipping, PAR = 8.6 dB @ 0.01% Probability, 3.84 MHz BW, Vcc = +28V, Icq = 160 mA

Parameter	Units	Typical		
Test Frequency	MHz	940	1960	2140
Channel Power	dBm	+30	+30	+30
Power Gain	dB	17	13	11.8
Input Return Loss	dB	11	13	10
Output Return Loss	dB	5.5	7.5	8.2
ACLR	dBc	-52	-49	-50
IMD3 @ +30 dBm PEP	dBc	-52	-52	-51
Operating Current, Icc	mA	217	230	246
Collector Efficiency	%	16.6	15.5	14.6
Output P1dB	dBm	+38.5	+38.5	+38.2
Quiescent Current, Icq	mA		160	
Vpd, Vbias	V		+5	
Vcc	V		+28	

Notes:
1. The reference designs shown in this datasheet have the device optimized for WCDMA ACLR performance at +25° C. Biasing for the amplifier is suggested at Vcc = +28V and Icq = 160 mA to achieve the best tradeoff in terms of efficiency and linearity. Increasing Icq will improve upon the device linearity (IMD3 and ACLR), but will decrease the efficiency performance slightly. More information is given in the other parts of this datasheet.
2. The AP603 evaluation board has been tested for ruggedness to be capable of handling:
   7:1 VSWR @ +28 Vcc, 2140 MHz, 5.5W CW Pout,
   5:1 VSWR @ +30 Vcc, 2140 MHz, 5.5W CW Pout,
   3:1 VSWR @ +32 Vcc, 2140 MHz, 5.5W CW Pout.

Absolute Maximum Rating

Parameter	Rating
Storage Temperature, T_{stg}	-55 to +125 ºC
Junction Temperature, T_J For 10^6 hours MTTF	192 ºC
RF Input Power (CW tone), P_{in}	Input P6dB
Breakdown Voltage C-B, BV_{CBO}	80 V @ 0.1 mA
Breakdown Voltage C-E, BV_{CEO}	51 V @ 0.1 mA
Quiescent Bias Current, I_{CQ}	320 mA
Power Dissipation, P_{DISS}	9.5 W

Operation of this device above any of these parameters may cause permanent damage.

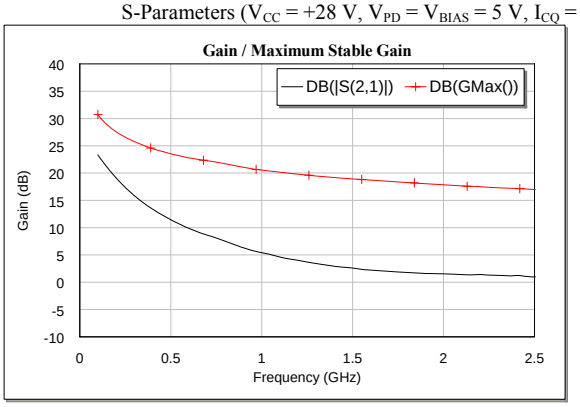
Ordering Information

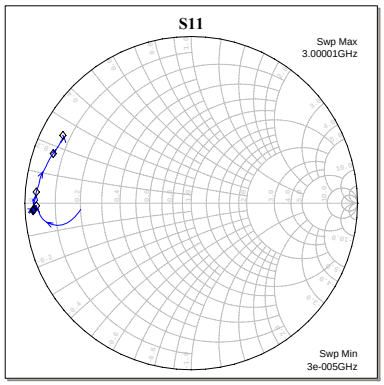
Part No.	Description
AP603-F	High Dynamic Range 28V 7W HBT Amplifier
AP603-PCB900	920-960 MHz Evaluation board
AP603-PCB1960	1930-1990 MHz Evaluation board
AP603-PCB2140	2110-2170 MHz Evaluation board

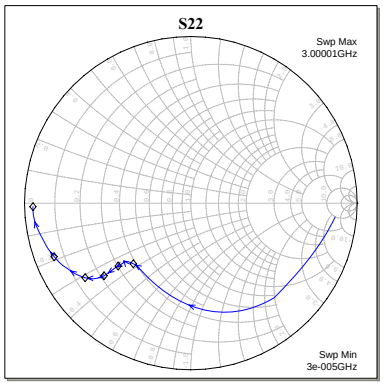
Specifications and information are subject to change without notice

Typical Device Data

S-Parameters (V_{CC} = +28 V, V_{PD} = V_{BIAS} = 5 V, I_{CQ} = 160 mA, T = 25 °C, unmatched 50 ohm system, calibrated to device leads)







The gain for the unmatched device in 50 ohm system is shown as the trace in black color. For a tuned circuit for a particular frequency, it is expected that actual gain will be higher, up to the maximum stable gain. The maximum stable gain is shown in the marked red line. The impedance plots are shown from 50 – 3000 MHz, with markers placed at 0.5 – 3.0 GHz in 0.5 GHz increments.

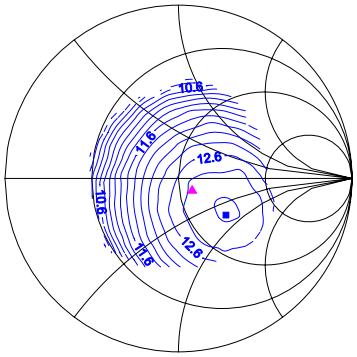
Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
50	-2.63	-169.40	25.54	146.01	-40.50	55.97	-1.32	-45.78
100	-1.78	-170.62	23.33	132.51	-38.11	39.21	-3.07	-67.75
200	-0.92	-173.99	19.08	109.79	-36.04	21.60	-5.00	-104.04
400	-0.64	-177.96	13.40	93.01	-35.59	9.15	-6.06	-129.02
600	-0.53	-178.87	9.88	85.15	-35.72	3.39	-5.82	-136.33
800	-0.52	-178.84	7.52	79.52	-35.90	6.93	-5.38	-138.25
1000	-0.46	-177.79	5.42	74.40	-35.68	5.88	-4.77	-139.20
1200	-0.44	-177.25	4.01	69.71	-35.62	3.23	-4.16	-139.65
1400	-0.38	-176.83	2.93	64.99	-35.48	1.79	-3.62	-139.95
1600	-0.39	-177.55	2.22	59.81	-35.13	-0.56	-3.12	-140.63
1800	-0.48	-179.87	1.77	52.82	-34.75	-4.12	-2.63	-142.14
2000	-0.59	175.92	1.54	44.04	-34.21	-10.23	-2.19	-144.85
2200	-0.73	170.02	1.41	33.03	-33.63	-18.12	-1.74	-149.24
2400	-0.97	163.30	1.23	19.79	-33.13	-29.67	-1.28	-155.12
2600	-1.21	157.14	0.75	3.56	-32.89	-43.94	-0.90	-162.55
2800	-1.28	153.30	0.03	-14.33	-33.04	-61.10	-0.57	-170.87
3000	-1.18	152.21	-0.89	-34.56	-33.44	-81.90	-0.45	-178.70

Device S-parameters are available for download off of the website at: http://www.wj.com

Load-Pull Data

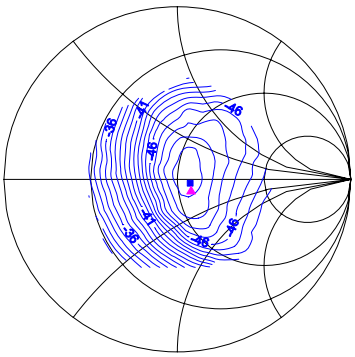
Test condition: Output Power = 29.5 dBm, V_{CC} = +28 V, I_{CQ} = 160 mA, Z_S = 50 Ω
Test signal = W-CDMA (PAR=8.6dB @ 0.01% Probability), 2140 MHz
The reference plane is at the AP603-PCB2140 eval board's SMA connectors.
The plots are shown to detail the optimization of the ACLR performance.

Gain Load-Pull



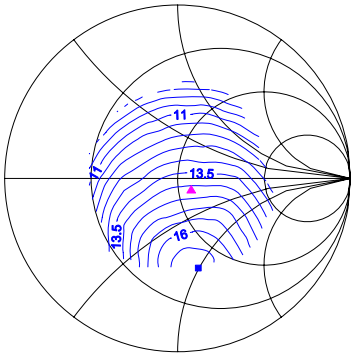
GAIN Max=13.08 dB at 76.9-j37.0

ACLR Load-Pull



ACPR1LO Min=-50.98 dBc at 57.9-j2.6

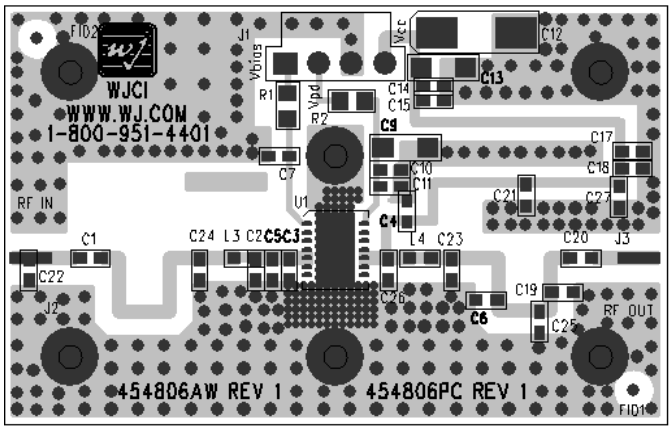
PAE Load-Pull



P.A.EFF Max=16.98 % at 34.4-j49.7

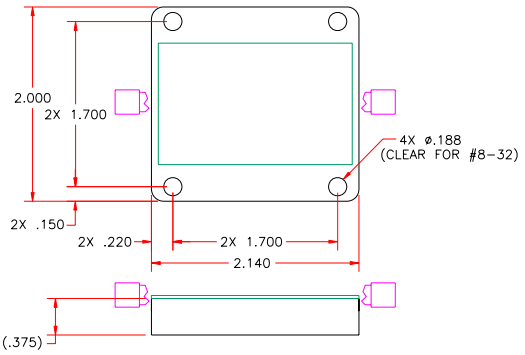
Specifications and information are subject to change without notice

Application Circuit PC Board Layout



PCB Material: 0.0147" Rogers Ultralam 2000, single layer, 1 oz Cu,
ε_r = 2.45, Microstrip line details: width = .042", spacing = .050"

Baseplate Configuration



Notes:
1. Please note that for reliable operation, the evaluation board will have to be mounted to a much larger heat sink during operation and in laboratory environments to dissipate the power consumed by the device. The use of a convection fan is also recommended in laboratory environments.
2. The area around the module underneath the PCB should not contain any soldermask in order to maintain good RF grounding.
3. For proper and safe operation in the laboratory, the power-on sequencing is recommended.

Evaluation Board Bias Procedure

The following bias procedure is recommended to ensure proper functionality of AP603 in a laboratory environment. The sequencing is not required in the final system application.

Bias.	Voltage (V)
Vcc	+28
Vbias	+5
Vpd	+5

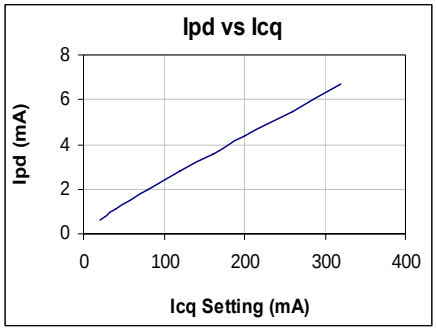
Turn-on Sequence:

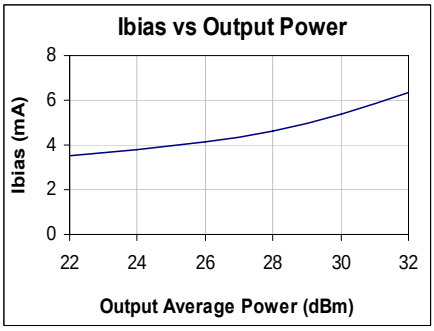
1. Attach input and output loads onto the evaluation board.
2. Turn on power supply Vcc = +28V.
3. Turn on power supply Vbias = +5V. At this point, the only current drawn by the device is leakage current (< 25μA).
4. Turn on power supply Vpd = +5V. Power supply Vcc should now be drawing typical Icq = 160mA.
5. Turn on RF power.

Turn-off Sequence:

1. Turn off RF power.
2. Turn off power supply Vpd = +5V.
3. Turn off power supply Vbias = +5V.
4. Turn off power supply Vcc = +28V.

Notes:
1. Icq can be adjusted with the resistor R2 from the Vpd (+5V) supply and the PIN_VPD (pin14) of the amplifier. Increasing R2 results in a lower Icq. Icq should not be increased above 320mA.
2. Vpd is used as a reference for the internal active bias circuitry. It can be used to turn on/off the amplifier. Ipd depends on the Icq quiescent current setting. Ipd can be up to 8mA at a quiescent current setting of 320mA.
3. Vbias should be maintained fixed at +5V. Ibias will change based on RF input power level. It can be up to 8mA on the AP603.

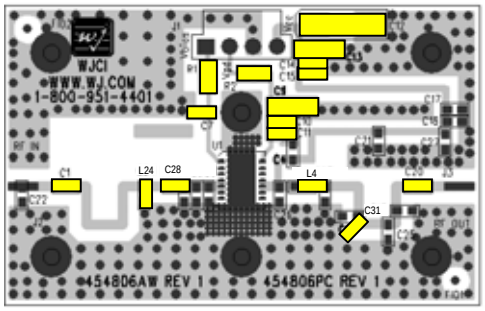


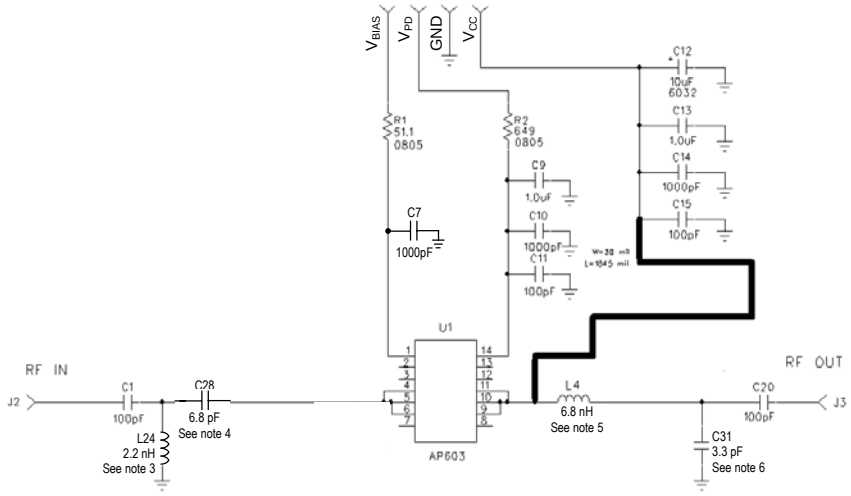


869-894 MHz Reference Design

Typical WCDMA Performance at 25 °C at a channel power of +30 dBm

Frequency	880 MHz
W-CDMA Channel Power	+30 dBm
Power Gain	18 dB
Input Return Loss	11 dB
Output Return Loss	7.5 dB
ACLR	-52 dBc
IMD3 @ +30 dBm PEP	-52 dBc
Operating Current, Icc	220 mA
Collector Efficiency	16.5 %
Output P1dB	+38.5 dBm
Quiescent Current, Icq	160 mA
Vpd, Vbias	+5 V
Vcc	+28 V

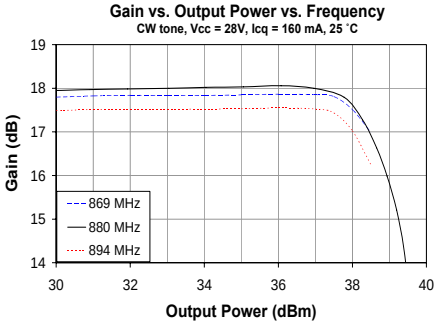


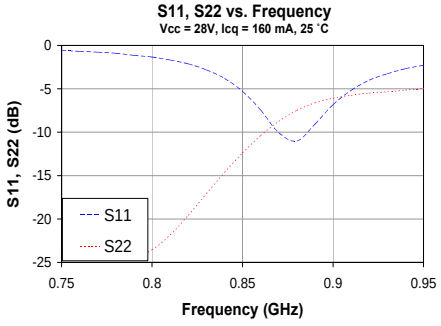


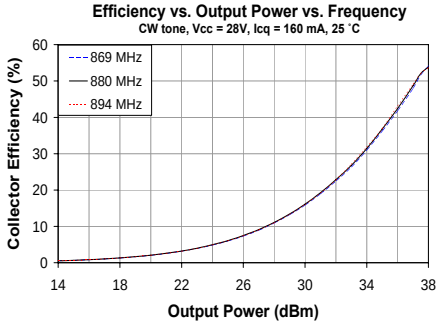
Notes:
1. The primary RF microstrip line is 50 Ω.
2. Components shown on the silkscreen but not on the schematic are not used.
3. The center of L24 is placed at 0.090" (3.5° @ 880 MHz) from the center of C5.
4. The center of C28 is placed at 0.220" (8.4° @ 880 MHz) from the edge of the AP603 (U1).
5. The center of L4 is placed at 0.200" (7.7° @ 880 MHz) from the edge of the AP603 (U1).
6. The center of C31 is placed at 0.360" (13.8° @ 880 MHz) from the center of L4.
7. The bold-faced RF trace is for the DC bias feed. The stub's length is approximately a ¼ λ.
8. The main RF trace is cut at component C28 and L4 for this particular reference design.

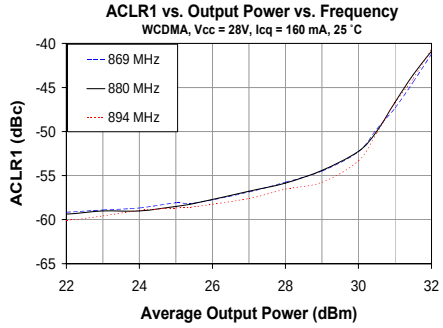
869-894 MHz Application Circuit Performance Plots

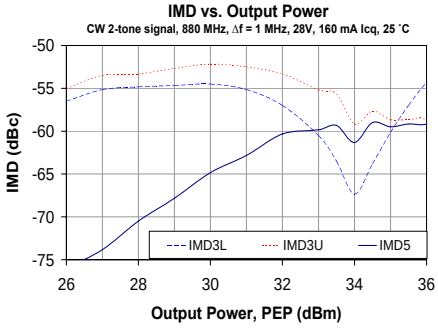
W-CDMA 3GPP Test Model 1+64 DPCH, 60% clipping, PAR = 8.6 dB @ 0.01% Probability, 3.84 MHz BW

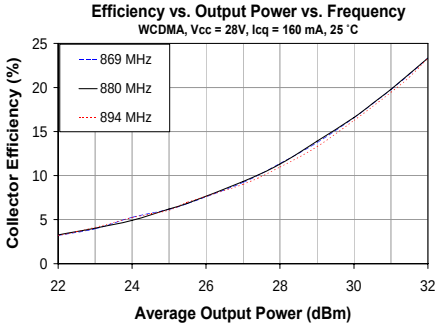










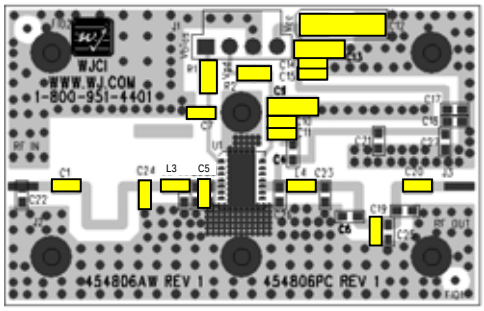


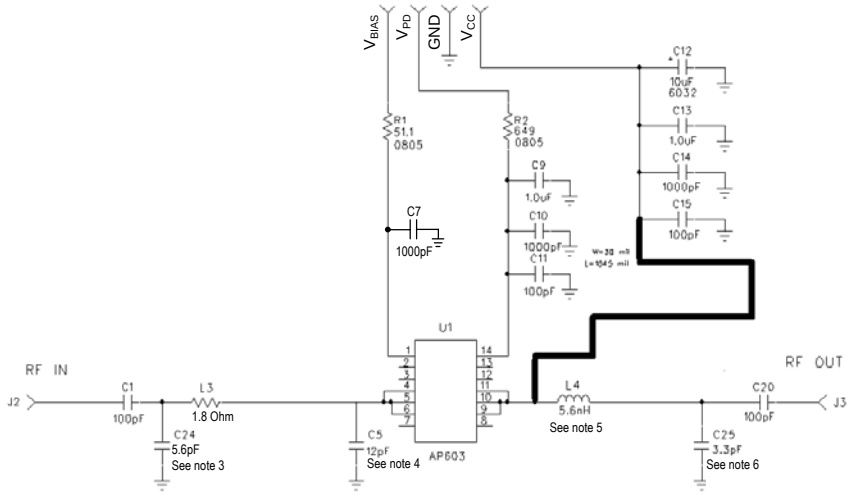
Unconditionally stable circuit version of this application circuit is available for download off of the website at: http://www.wj.com

920-960 MHz Application Circuit (AP603-PCB900)

Typical WCDMA Performance at 25 °C at a channel power of +30 dBm

Frequency	940 MHz
W-CDMA Channel Power	+30 dBm
Power Gain	17 dB
Input Return Loss	11 dB
Output Return Loss	5.5 dB
ACLR	-52 dBc
IMD3 @ +30 dBm PEP	-52 dBc
Operating Current, Icc	217 mA
Collector Efficiency	16.6 %
Output P1dB	+38.5 dBm
Quiescent Current, Icq	160 mA
Vpd, Vbias	+5 V
Vcc	+28 V



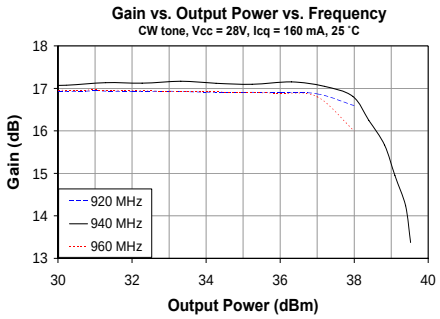


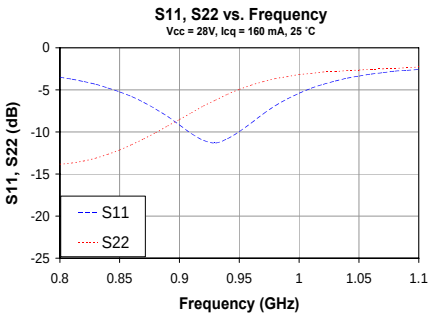
Notes:

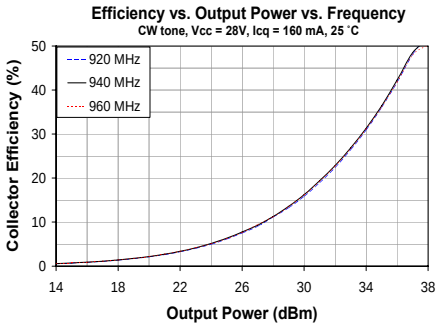
1. The primary RF microstrip line is 50 Ω.
2. Components shown on the silkscreen but not on the schematic are not used.
3. The center of C24 is placed at 0.245" (10.0° @ 940 MHz) from the center of C5.
4. The center of C5 is placed at .060" (2.5° @ 940 MHz) from the edge of the AP603 (U1).
5. The center of L4 is placed at 0.170" (7.0° @ 940 MHz) from the edge of the AP603 (U1). L4 is required to be an AVX 0805 type.
6. The center of C25 is placed at 0.480" (19.7° @ 940 MHz) from the center of L4.
7. The bold-faced RF trace is for the DC bias feed. The stub's length is approximately a ¼ λ.
8. The main RF trace is cut at component L3 and L4 for this particular reference design.

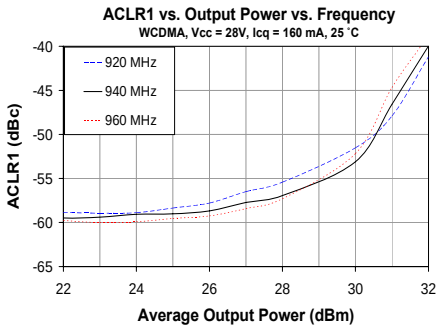
920-960 MHz Application Circuit Performance Plots

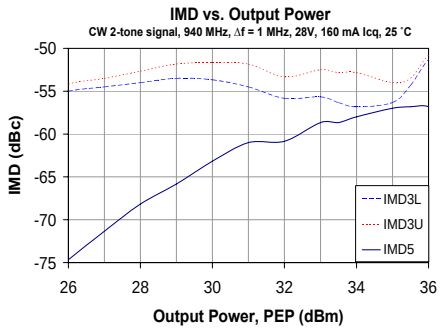
W-CDMA 3GPP Test Model 1+64 DPCH, 60% clipping, PAR = 8.6 dB @ 0.01% Probability, 3.84 MHz BW

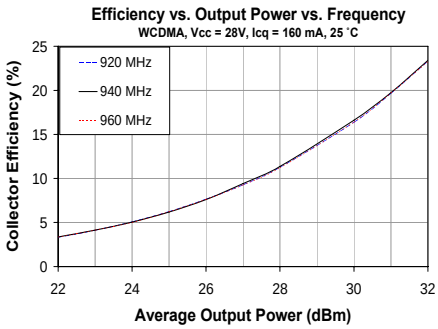








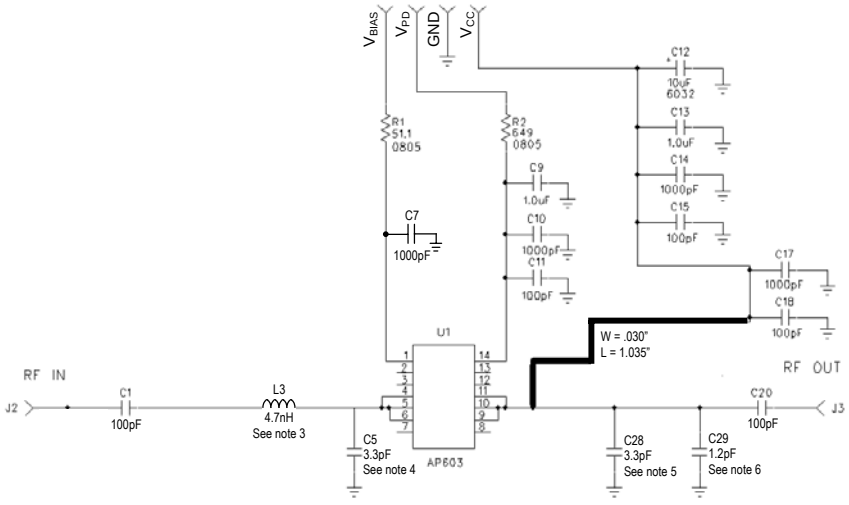


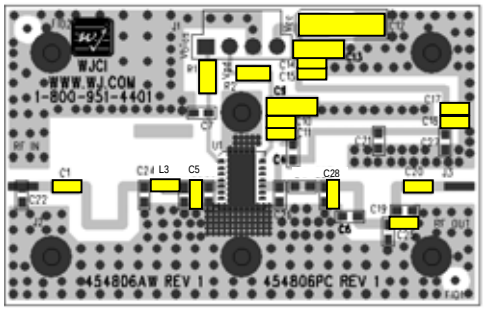


1930-1990 MHz Application Circuit (AP603-PCB1960)

Typical WCDMA Performance at 25 °C at a channel power of +30 dBm

Frequency	1960 MHz
W-CDMA Channel Power	+30 dBm
Power Gain	13 dB
Input Return Loss	13 dB
Output Return Loss	7.5 dB
ACLR	-49 dBc
IMD3 @ +30 dBm PEP	-52 dBc
Operating Current, Icc	230 mA
Collector Efficiency	15.5 %
Output P1dB	+38.5 dBm
Quiescent Current, Icq	160 mA
Vpd, Vbias	+5 V
Vcc	+28 V

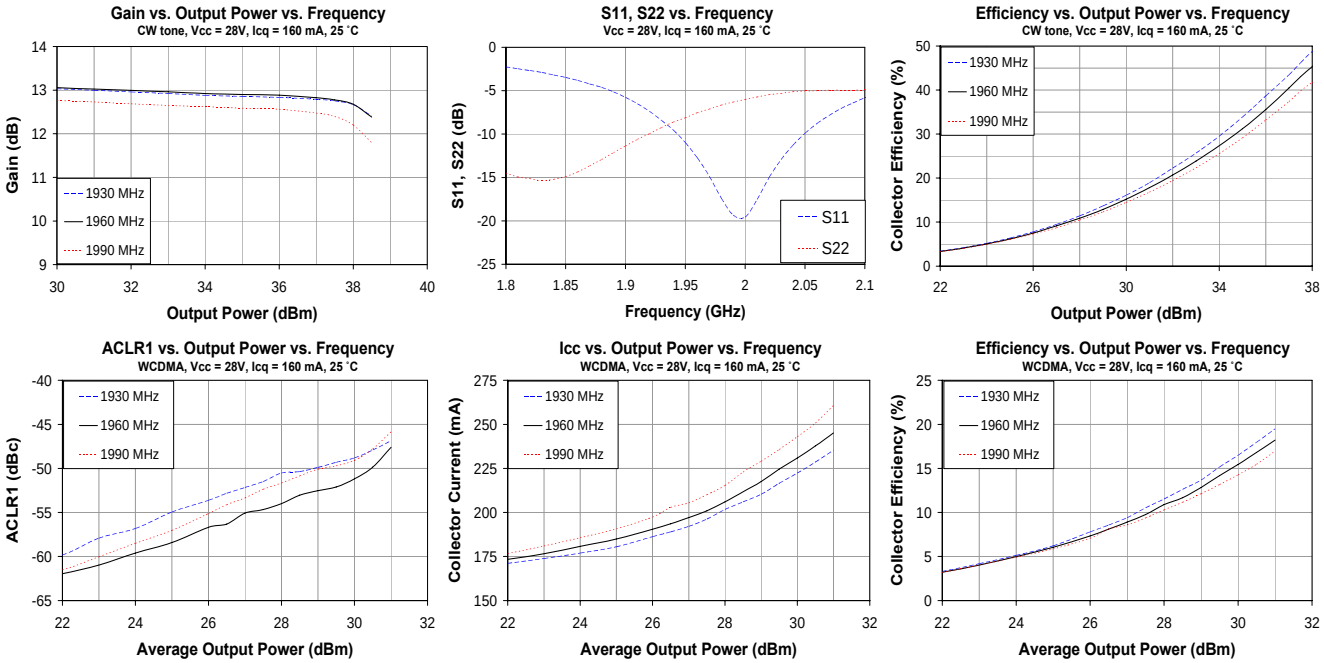




Notes:
1. The primary RF microstrip line is 50 Ω.
2. Components shown on the silkscreen but not on the schematic are not used.
3. The center of L3 is placed at 0.115" (9.8° @ 1960 MHz) from the center of C5.
4. The center of C5 is placed at 0.100" (8.5° @ 1960 MHz) from the edge of the AP603 (U1).
5. The center of C28 is placed at 0.300" (25.6° @ 1960 MHz) from the edge of the AP603 (U1).
6. The center of C29 is placed at 0.420" (35.9° @ 1960 MHz) from the center of C28.
7. The bold-faced RF trace is for the DC bias feed. The stub's length is approximately a ¼ λ.

1930-1990 MHz Application Circuit Performance Plots

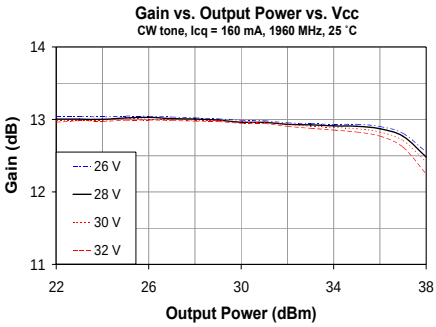
W-CDMA 3GPP Test Model 1+64 DPCH, 60% clipping, PAR = 8.6 dB @ 0.01% Probability, 3.84 MHz BW

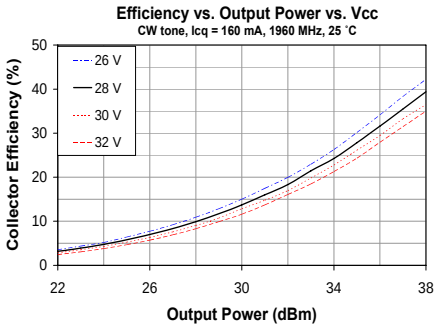


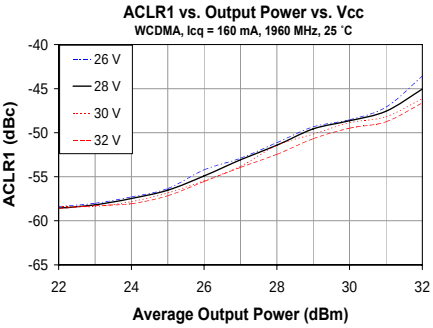
Unconditionally stable version of this application circuit is available for download off of the website at: http://www.wj.com

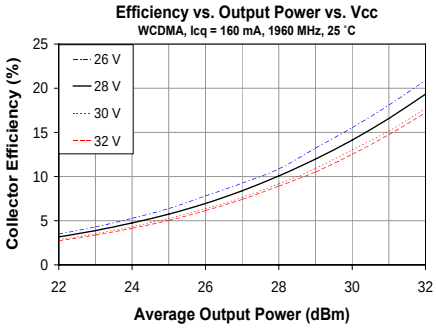
1930-1990 MHz Application Circuit Performance Plots

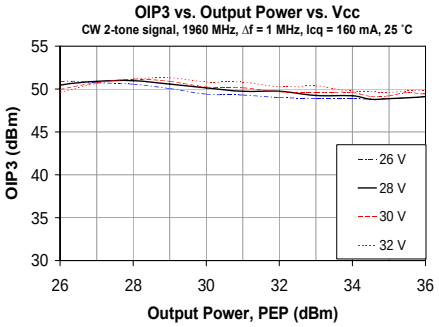
W-CDMA 3GPP Test Model 1+64 DPCH, 60% clipping, PAR = 8.6 dB @ 0.01% Probability, 3.84 MHz BW

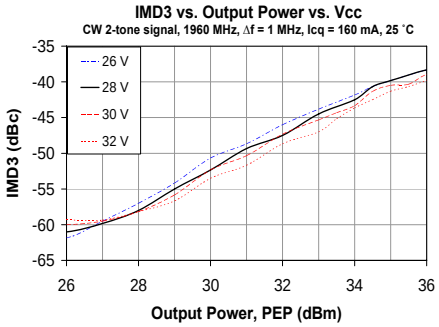


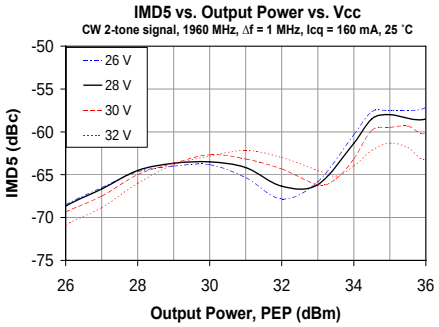








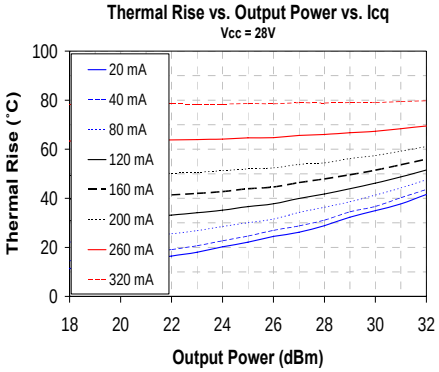


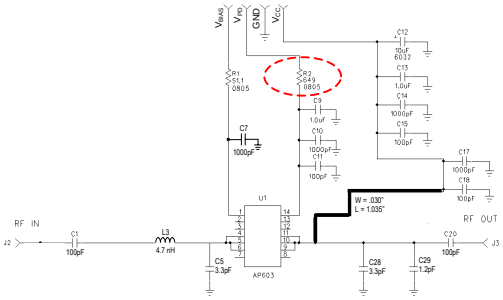


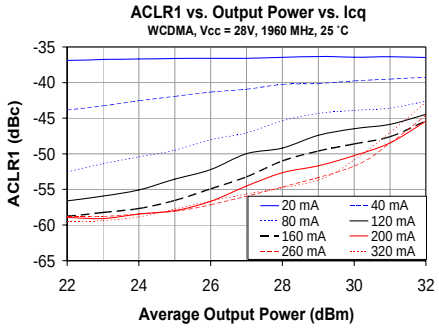
1930-1990 MHz Application Note: Changing Icq Biasing Configurations

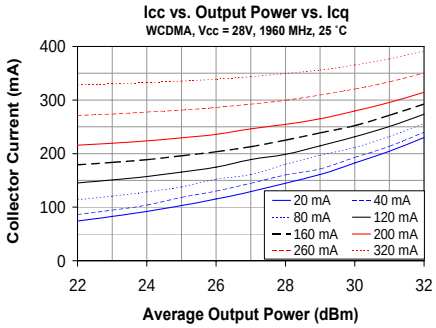
The AP603 can be configured to be operated with lower bias current by varying the bias-adjust resistor – R2. The recommended circuit configurations shown previously in this datasheet have the device operating with a 160 mA as the quiescent current (I_{CQ}). This biasing level represents the best tradeoff in terms of linearity and efficiency. Lowering I_{CQ} will improve upon the efficiency of the device, but degraded linearity. Increasing I_{CQ} has nominal improvement upon the linearity, but will degrade the device's efficiency. Measured data shown in the plots below represents the AP603 measured and configured for 1.96 GHz applications. It is expected that variation of the bias current for other frequency applications will produce similar performance results.

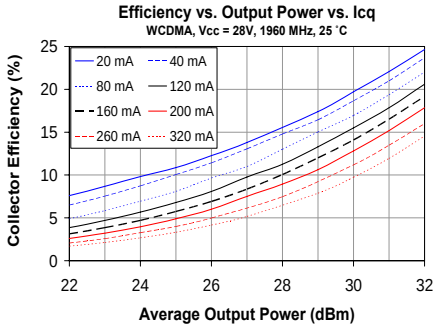
Icq (mA)	R2 (Ω)	V_{PD} (V)	PIN_V_{PD} (V)
20	4.32k	5	2.46
40	2.33k	5	2.52
80	1.24k	5	2.61
120	852	5	2.68
160	**649**	**5**	**2.74**
200	521	5	2.80
260	398	5	2.89
320	313	5	2.98

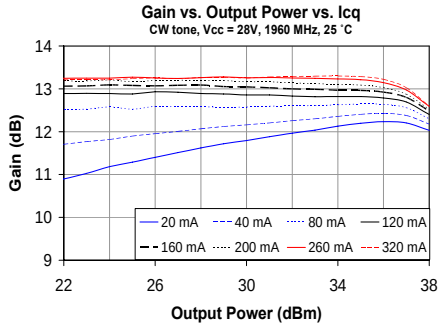


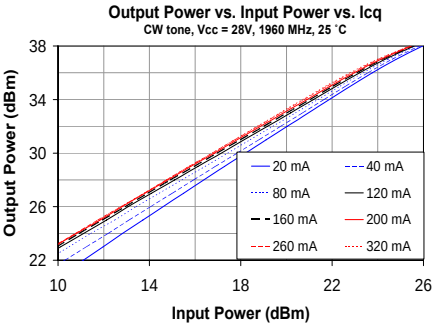


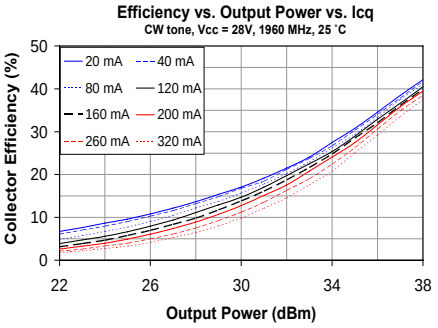


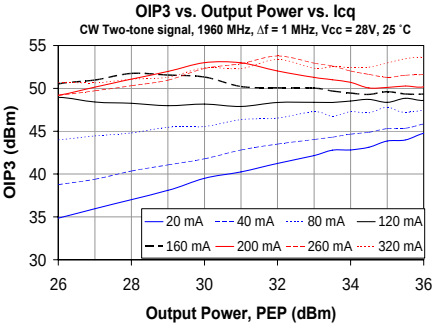


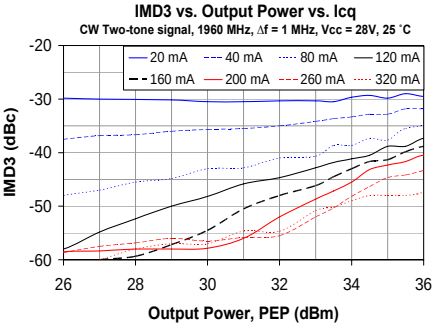


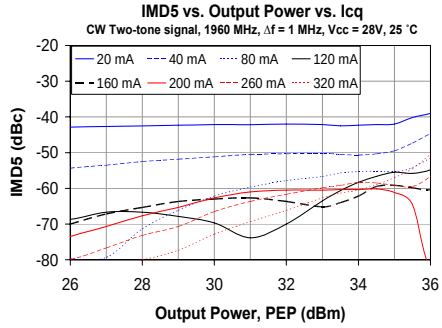








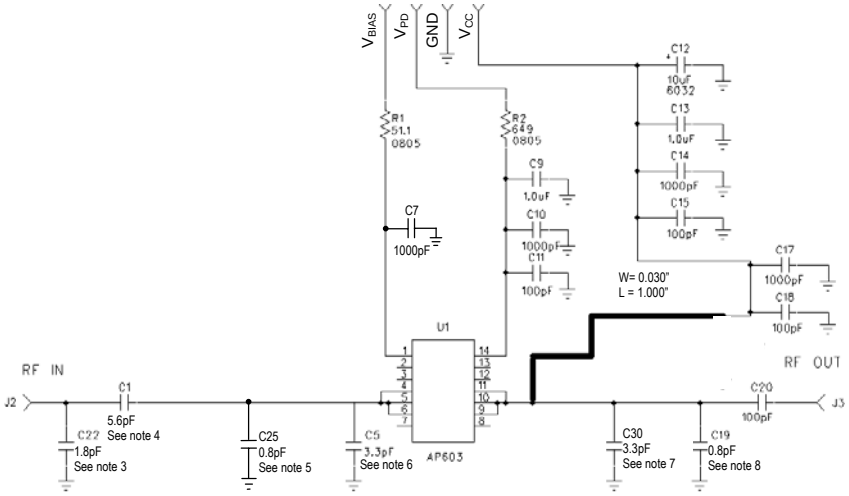


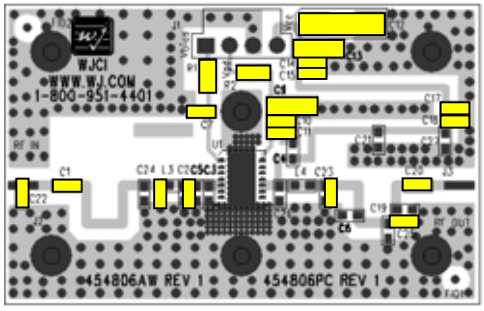


2010-2025 MHz Application Circuit

Typical Performance at 25 °C at an output power of +30 dBm

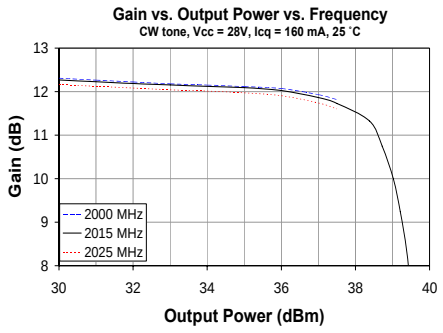
Frequency	2015 MHz
Total Output Power	+30 dBm
Power Gain	12.3 dB
Input Return Loss	11 dB
Output Return Loss	14 dB
IMD3 @ +30 dBm PEP	-48 dBc
Operating Current, Icc	230 mA
Collector Efficiency	15.5 %
Output P1dB	+38.2 dBm
Quiescent Current, Icq	160 mA
Vpd, Vbias	+5 V
Vcc	+28 V

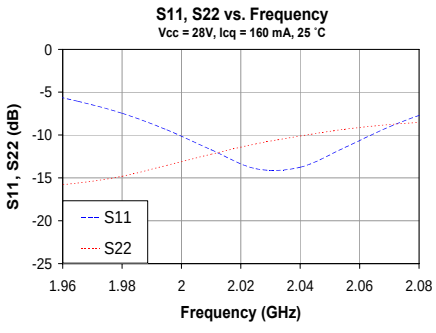


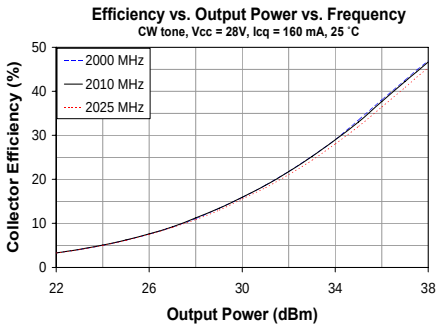


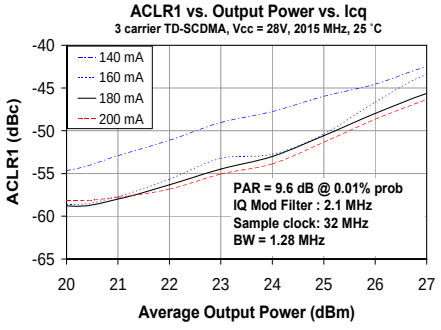
Notes:
1. The primary RF microstrip line is 50 Ω.
2. Components shown on the silkscreen but not on the schematic are not used.
3. The center of C22 is placed at 0.185" (16.3° @ 2015 MHz) from the center of C1.
4. The center of C1 is placed at 0.705" (61.9° @ 2015 MHz) from the center of C25.
5. The center of C25 is placed at 0.140" (12.3° @ 2015 MHz) from the center of C5.
6. The center of C5 is placed at 0.125" (11.0° @ 2015 MHz) from the edge of the AP603 (U1).
7. The center of C30 is placed at 0.250" (41.2° @ 2015 MHz) from the edge of the AP603 (U1).
8. The center of C19 is placed at 0.490" (43.0° @ 2015 MHz) from the center of C23.
9. The bold-faced RF trace is for the DC bias feed. The stub's length is approximately a ¼ λ.

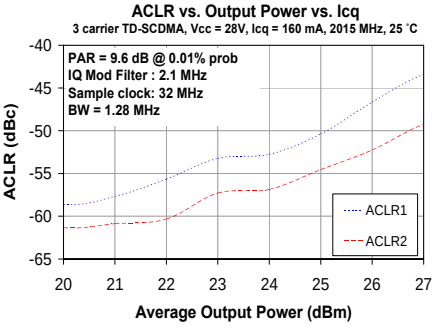
2010-2025 MHz Application Circuit Performance Plots

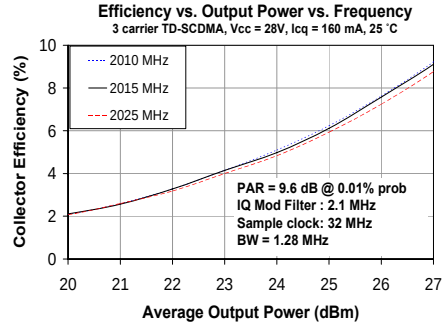








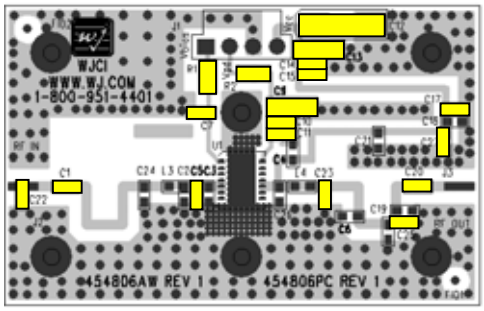


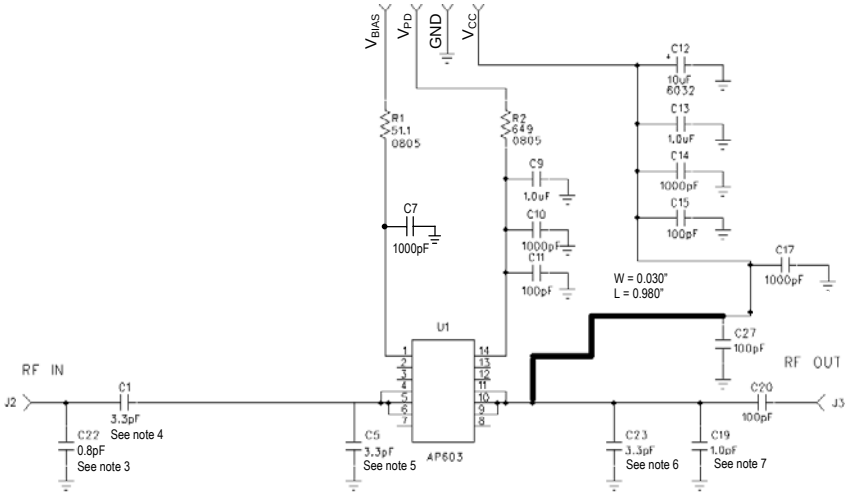


2110-2170 MHz Application Circuit (AP603-PCB2140)

Typical WCDMA Performance at 25 °C at a channel power of +30 dBm

Frequency	2140 MHz
W-CDMA Channel Power	+30 dBm
Power Gain	11.8 dB
Input Return Loss	10 dB
Output Return Loss	8.2 dB
ACLR	-50 dBc
IMD3 @ +30 dBm PEP	-51 dBc
Operating Current, Icc	246 mA
Collector Efficiency	14.6 %
Output P1dB	+38.2 dBm
Quiescent Current, Icq	160 mA
Vpd, Vbias	+5 V
Vcc	+28 V

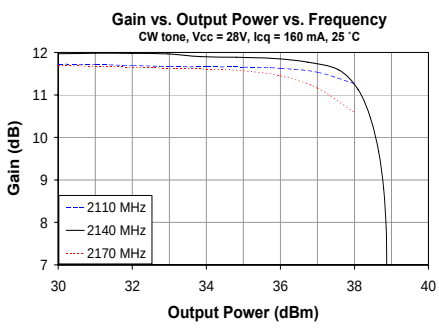


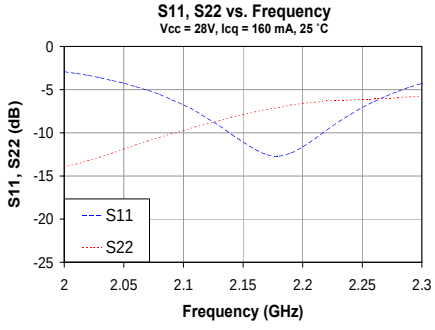


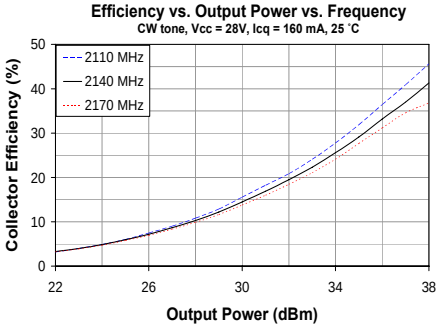
Notes:
1. The primary RF microstrip line is 50 Ω.
2. Components shown on the silkscreen but not on the schematic are not used.
3. The center of C22 is placed at 0.185" (17.3° @ 2140 MHz) from the center of C1.
4. The center of C1 is placed at 0.860" (80.2° @ 2140 MHz) from the center of C5.
5. The center of C5 is placed at 0.085" (7.9° @ 2140 MHz) from the edge of the AP603 (U1).
6. The center of C23 is placed at 0.245" (22.9° @ 2140 MHz) from the edge of the AP603 (U1).
7. The center of C19 is placed at 0.475" (44.3° @ 2140 MHz) from the center of C23.
8. The bold-faced RF trace is for the DC bias feed. The stub's length is approximately a ¼ λ.

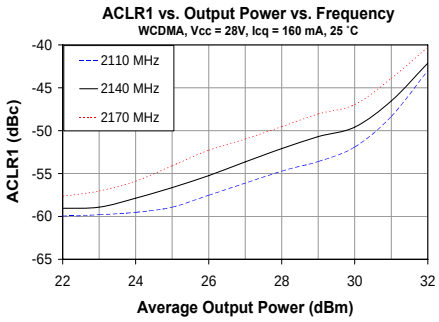
2110-2170 MHz Application Circuit Performance Plots

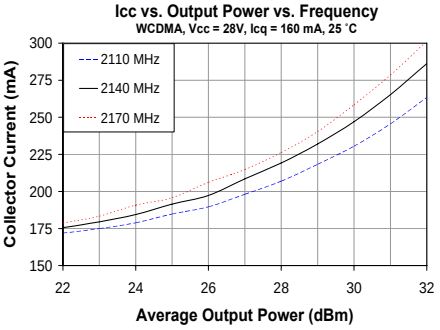
W-CDMA 3GPP Test Model 1+64 DPCH, 60% clipping, PAR = 8.6 dB @ 0.01% Probability, 3.84 MHz BW

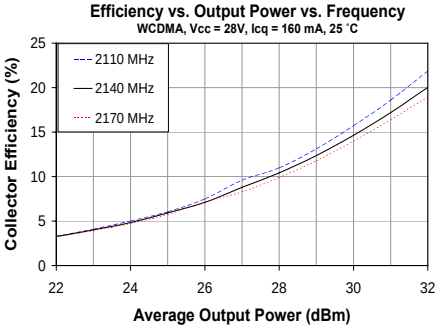










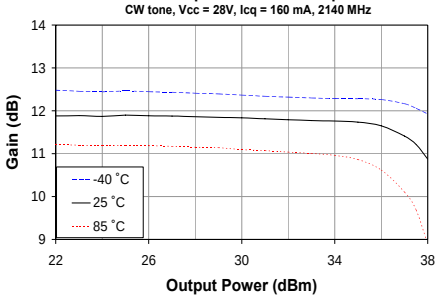


Unconditionally stable circuit version of this application circuit is available for download off of the website at: http://www.wj.com

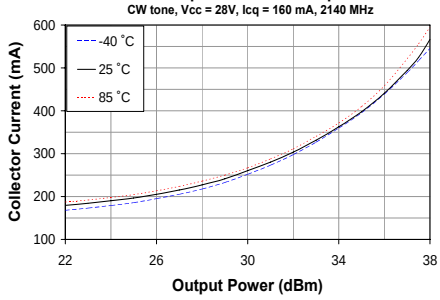
2110-2170 MHz Application Circuit Performance Plots

W-CDMA 3GPP Test Model 1+64 DPCH, 60% clipping, PAR = 8.6 dB @ 0.01% Probability, 3.84 MHz BW

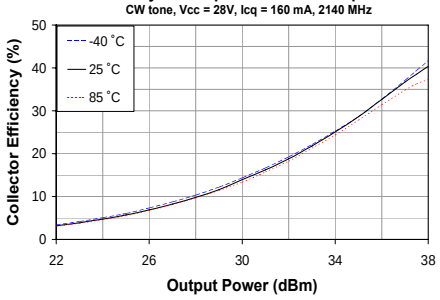
Gain vs. Output Power vs. Temperature
CW tone, Vcc = 28V, Icq = 160 mA, 2140 MHz



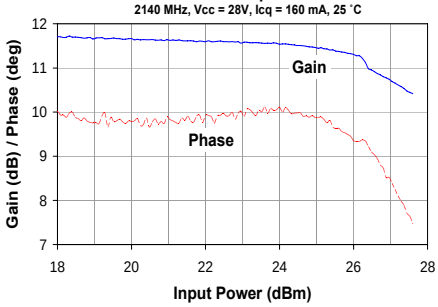
Icc vs. Output Power vs. Temperature
CW tone, Vcc = 28V, Icq = 160 mA, 2140 MHz



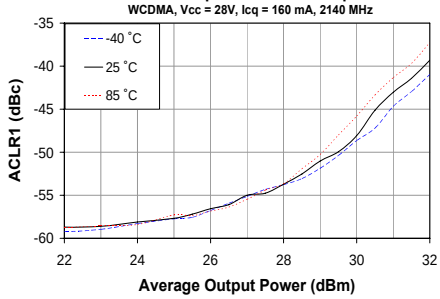
Efficiency vs. Output Power vs. Temperature
CW tone, Vcc = 28V, Icq = 160 mA, 2140 MHz



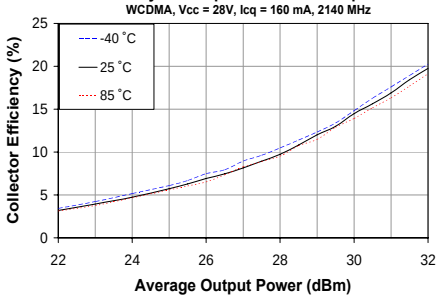
AM-PM vs. Input Power
2140 MHz, Vcc = 28V, Icq = 160 mA, 25 °C



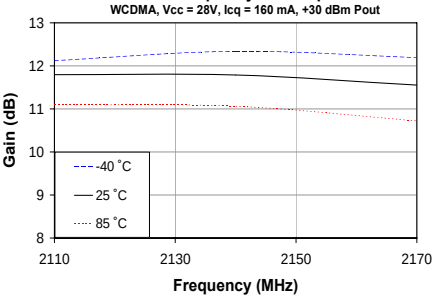
ACLR1 vs. Output Power vs. Temperature
WCDMA, Vcc = 28V, Icq = 160 mA, 2140 MHz



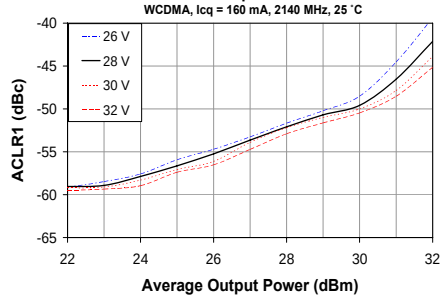
Efficiency vs. Output Power vs. Temperature
WCDMA, Vcc = 28V, Icq = 160 mA, 2140 MHz



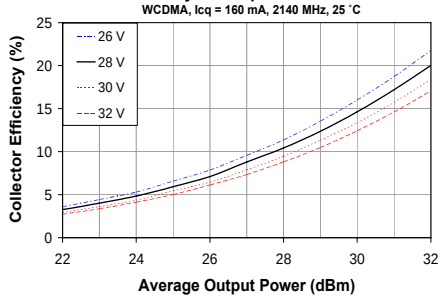
Gain vs. Frequency vs. Temperature
WCDMA, Vcc = 28V, Icq = 160 mA, +30 dBm Pout



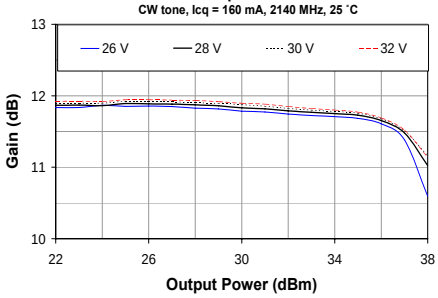
ACLR1 vs. Output Power vs. Vcc
WCDMA, Icq = 160 mA, 2140 MHz, 25 °C



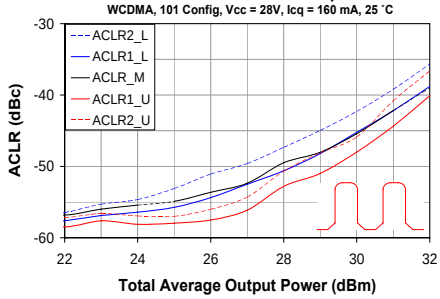
Efficiency vs. Output Power vs. Vcc
WCDMA, Icq = 160 mA, 2140 MHz, 25 °C



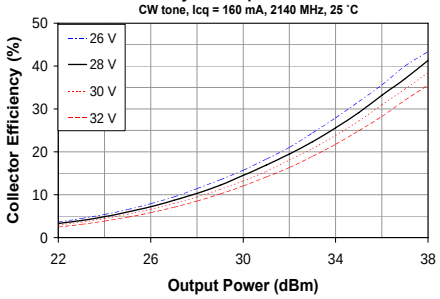
Gain vs. Output Power vs. Vcc
CW tone, Icq = 160 mA, 2140 MHz, 25 °C



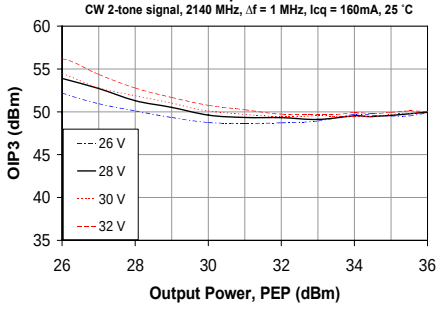
2-Carrier WCDMA ACLR vs. Output Power
WCDMA, 101 Config, Vcc = 28V, Icq = 160 mA, 25 °C



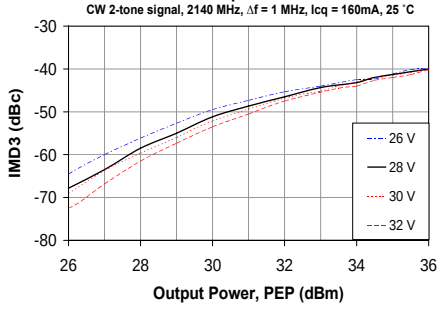
Efficiency vs. Output Power vs. Vcc
CW tone, Icq = 160 mA, 2140 MHz, 25 °C



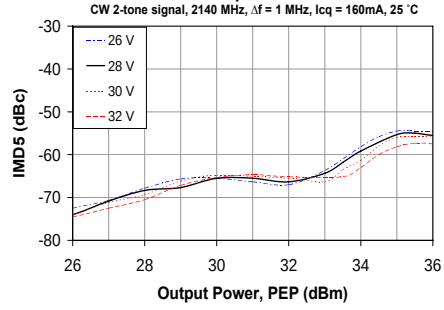
OIP3 vs. Output Power vs. Vcc
CW 2-tone signal, 2140 MHz, Δf = 1 MHz, Icq = 160mA, 25 °C



IMD3 vs. Output Power vs. Vcc
CW 2-tone signal, 2140 MHz, Δf = 1 MHz, Icq = 160mA, 25 °C



IMD5 vs. Output Power vs. Vcc
CW 2-tone signal, 2140 MHz, Δf = 1 MHz, Icq = 160mA, 25 °C

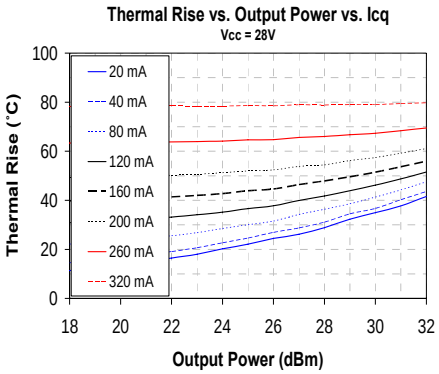


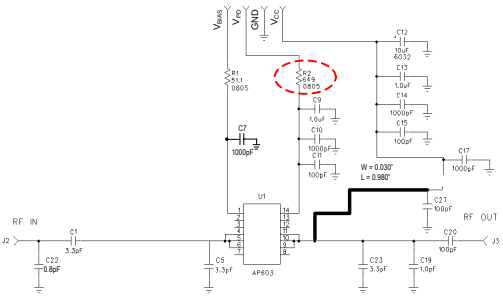
Specifications and information are subject to change without notice

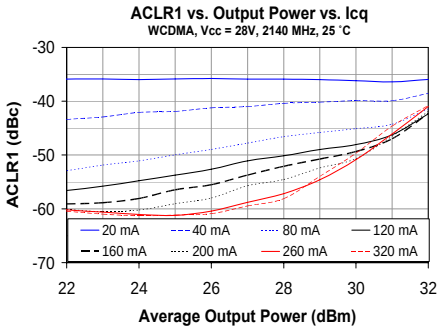
2110-2170 MHz Application Note: Changing Icq Biasing Configurations

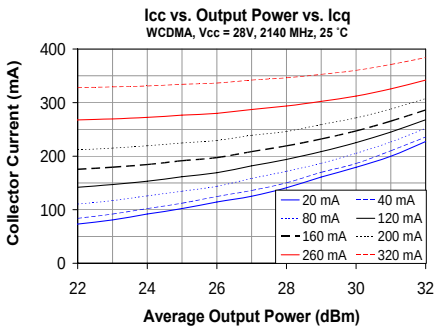
The AP603 can be configured to be operated with lower bias current by varying the bias-adjust resistor – R2. The recommended circuit configurations shown previously in this datasheet have the device operating with a 160 mA as the quiescent current (I_{CQ}). This biasing level represents the best tradeoff in terms of linearity and efficiency. Lowering I_{CQ} will improve upon the efficiency of the device, but degraded linearity. Increasing I_{CQ} has nominal improvement upon the linearity, but will degrade the device's efficiency. Measured data shown in the plots below represents the AP603 measured and configured for 2.14 GHz applications. It is expected that variation of the bias current for other frequency applications will produce similar performance results.

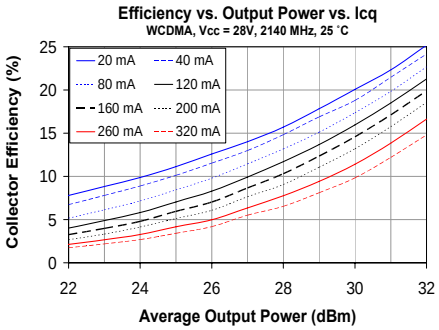
Icq (mA)	R2 (Ω)	V_{PD} (V)	PIN_V_{PD} (V)
20	4.32k	5	2.46
40	2.33k	5	2.52
80	1.24k	5	2.61
120	852	5	2.68
160	**649**	**5**	**2.74**
200	521	5	2.80
260	398	5	2.89
320	313	5	2.98

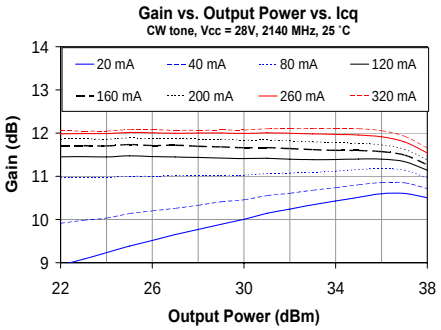


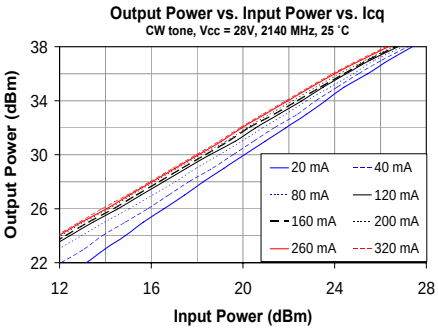


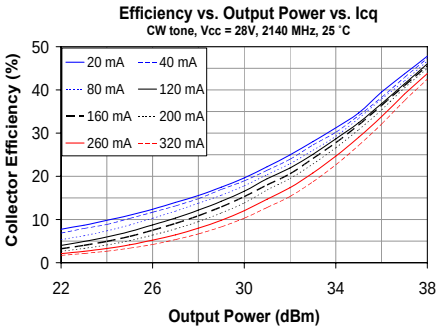


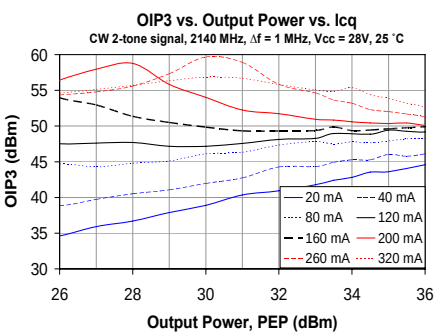


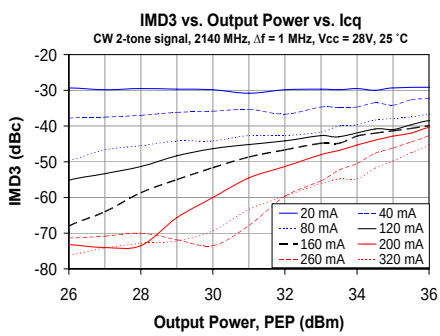


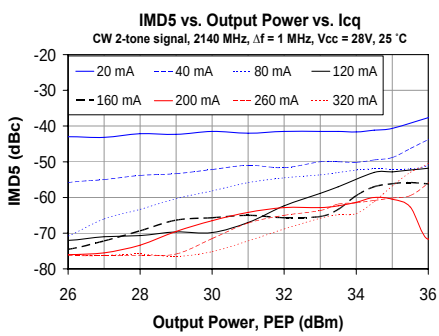










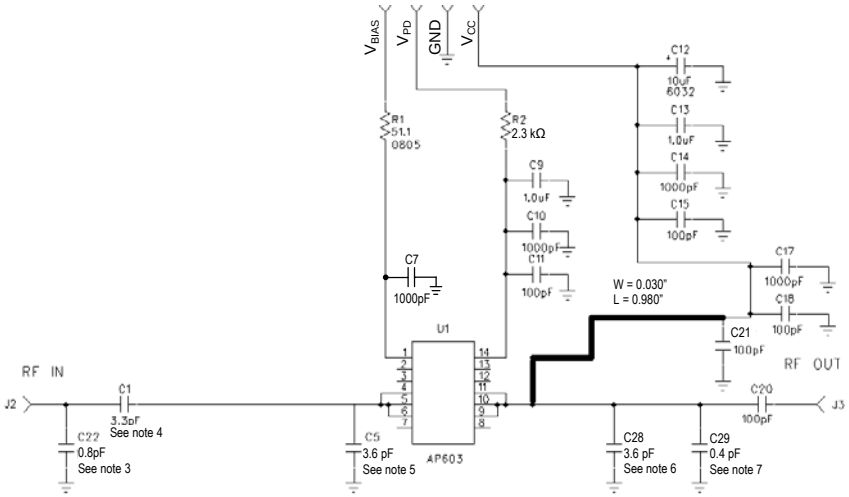


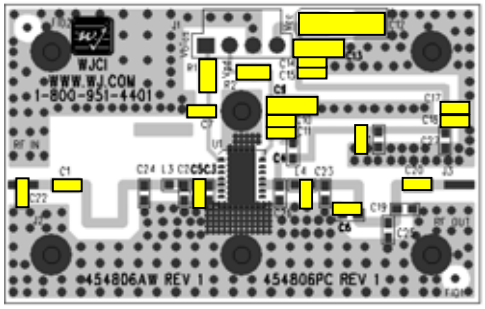
2110-2170 MHz High Efficiency Reference Design

Targeted for Linearized Power Amplifiers

Typical WCDMA Performance at 25 °C at a channel power of +32 dBm

Frequency	2140 MHz
W-CDMA Channel Power	+32 dBm
Power Gain	11.5 dB
Input Return Loss	20 dB
Output Return Loss	11 dB
ACLR	-34 dBc
Operating Current, Icc	170 mA
Collector Efficiency	32.5 %
Output P1dB	+38.5 dBm
Quiescent Current, Icq	40 mA
Vpd, Vbias	+5 V
Vcc	+28 V

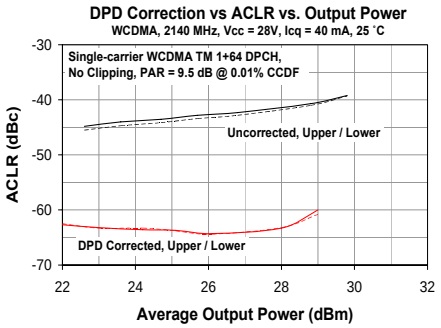


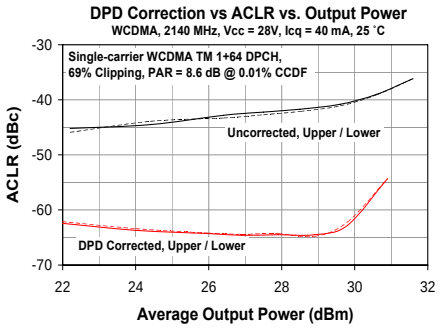


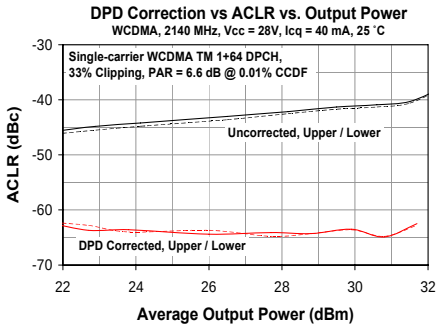
Notes:

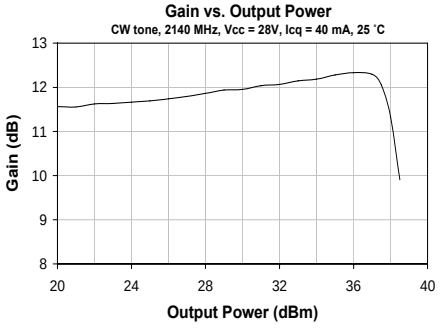
1. The primary RF microstrip line is 50 Ω.
2. Components shown on the silkscreen but not on the schematic are not used.
3. The center of C22 is placed at 0.185" (17.3° @ 2140 MHz) from the center of C1.
4. The center of C1 is placed at 0.875" (81.6° @ 2140 MHz) from the center of C5.
5. The center of C5 is placed at 0.070" (6.5° @ 2140 MHz) from the edge of the AP603 (U1).
6. The center of C28 is placed at 0.190" (17.7° @ 2140 MHz) from the edge of the AP603 (U1).
7. The center of C29 is placed at 0.300" (28.0° @ 2140 MHz) from the center of C28.
8. The bold-faced RF trace is for the DC bias feed. The stub's length is approximately a ¼ λ.

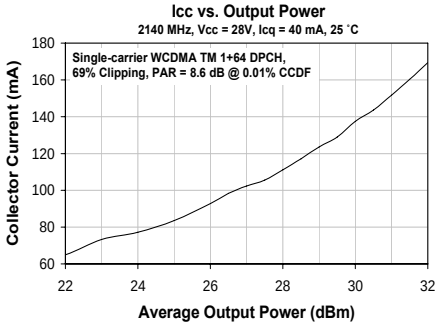
2110-2170 MHz High Efficiency Application Circuit Performance Plots

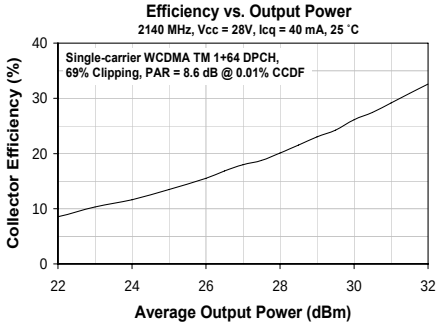








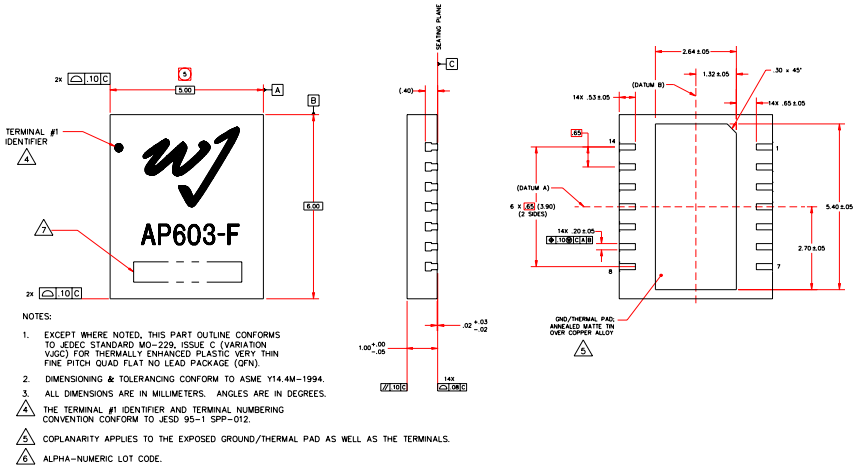




AP603-F Mechanical Information

This package is lead-free and RoHS-compliant. It is compatible with both lead-free (maximum 260 °C reflow temperature) and leaded (maximum 245 °C reflow temperature) soldering processes. The plating material on the pins is annealed matte tin over copper.

Outline Drawing



NOTES:

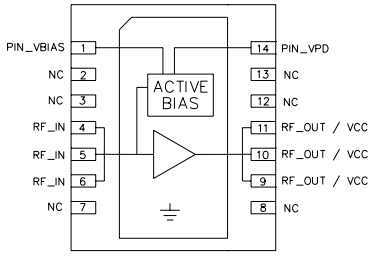
1. EXCEPT WHERE NOTED, THIS PART OUTLINE CONFORMS TO JEDEC STANDARD MO-229, ISSUE C (VARIATION VJCC) FOR THERMALLY ENHANCED PLASTIC VERY THIN FINE PITCH QUAD FLAT NO LEAD PACKAGE (QFN).
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.4M-1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION CONFORM TO JESD 95-1 SPP-012.
5. COPLANARITY APPLIES TO THE EXPOSED GROUND/THERMAL PAD AS WELL AS THE TERMINALS.
6. ALPHA-NUMERIC LOT CODE.

Product Marking

The component will be laser marked with an "AP603-F" product label with an alphanumeric lot code on the top surface of the package.

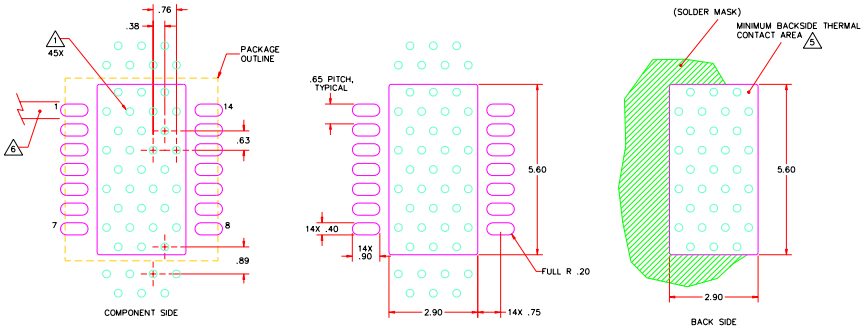
Tape and reel specifications for this part will be located on the website in the "Application Notes" section.

Functional Pin Layout



Pin	Function
1	PIN_VBIAS
2, 3, 7, 8, 12, 13	N/C
4, 5, 6	RF IN
9, 10, 11	RF Output / Vcc
14	PIN_VPD
Backside paddle	GND

Mounting Configuration / Land Pattern



NOTES:

1. GROUND/THERMAL VIAS ARE CRITICAL FOR THE PROPER PERFORMANCEOF THIS DEVICE. VIAS SHOULD USE A .35mm (#80/.0135") DIAMETER DRILL AND HAVE A FINAL PLATED THRU DIAMETER OF .25mm (.010").
2. ADD AS MUCH COPPER AS POSSIBLE TO INNER AND OUTER LAYERS NEAR THE PART TO ENSURE OPTIMAL THERMAL PERFORMANCE.
3. TO ENSURE RELIABLE OPERATION, DEVICE GROUND PADDLE-TO-GROUND PAD SOLDER JOINT IS CRITICAL.
4. ADD MOUNTING SCREWS NEAR THE PART TO FASTEN THE BOARD TO A HEATSINK. ENSURE THAT THE GROUND/THERMAL VIA REGION CONTACTS THE HEATSINK.
5. DO NOT PUT SOLDER MASK ON THE BACK SIDE OF THE PC BOARD IN THE REGION WHERE THE BOARD CONTACTS THE HEATSINK.
6. RF TRACE WIDTH DEPENDS UPON THE PC BOARD MATERIAL AND CONSTRUCTION.
7. USE 1 OZ. COPPER MINIMUM.
8. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
9. A HEATSINK UNDERNEATH THE AREA OF THE PCB FOR THE MOUNTED DEVICE IS STRICTLY REQUIRED FOR PROPER THERMAL OPERATION. DAMAGE TO THE DEVICE CAN OCCUR WITHOUT THE USE OF ONE.

MSL / ESD Rating

Caution! ESD sensitive device.

ESD Rating: Class 1B
Value: Passes ≥ 500V to <1000V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class IV
Value: Passes ≥ 1000V to <2000V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating: Level 3 at +260 °C convection reflow
Standard: JEDEC Standard J-STD-020

Thermal Specifications

Parameter	Rating
Thermal Resistance, Θ_{JC} Referenced from peak junction to the center of the bottomside ground paddle	8.7 °C / W
Junction Temperature, T_J For 10^6 hours MTTF	192 °C
Max Junction Temperature, $T_{J,max}$ For catastrophic failure	250 °C