Features
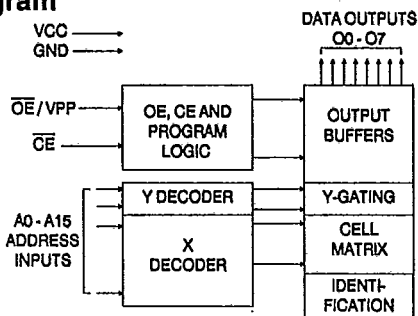
- Low Power CMOS Operation
  100 μA max. Standby
  40 mA max. Active at 5 MHz
- Fast Read Access Time - 120ns
- Wide Selection of JEDEC Standard Packages Including OTP
  28 -Lead 600 mil Cerdip and OTP Plastic DIP
  32-Pad LCC and OTP PLCC
- 5V± 10% Supply
- High Reliability CMOS Technology
  2000V ESD Protection
  200mA Latchup Immunity
- Fast Programming - 4ms/byte (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Full Military, Commercial and Industrial Temperature Ranges

512K (64K x 8) UV Erasable CMOS EPROM

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Block Diagram

Description

The AT27C512 chip is a low-power, high performance 524,288 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized 64K x 8. It requires only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 120ns, eliminating the need for speed reducing WAIT states on high performance microprocessor systems.

Atmel's 1.5 micron CMOS technology provides optimum speed, low power and high noise immunity. Power consumption is typically only 15mA in Active Mode and less than 10μA in Standby. In addition to the speed, power and reliability advantages of the CMOS process, the CMOS technology is an extension of Atmel's high quality and highly manufacturable floating poly EPROM technology.

Pin Configurations

Pin Name	Function
A0-A15	Addresses
O0-O7	Outputs
CE	Chip Enable
OE /Vpp	Output Enable
NC	No Connect
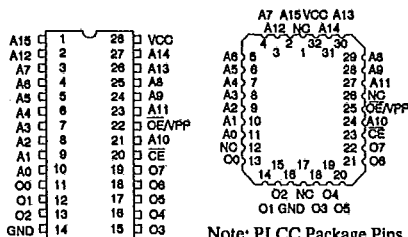
Note: PLCC Package Pins 1 and 17 are DON'T CONNECT.

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Description (Continued)

The AT27C512 comes in a choice of industry standard JEDEC-approved packages including; 28-pin DIP in ceramic or one time programmable (OTP) plastic, and 32-pad ceramic leadless chip carrier (LCC), or OTP plastic J-leaded chip carrier (PLCC). All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

With high density 64K byte storage capability, the AT27C512 allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's 27C512 has additional features to ensure high quality and efficient production use. The Fast Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 4ms/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Erasure Characteristics

The entire memory array of the AT27C512 is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 μW/cm² intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15W•sec/cm². To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V[1]
Voltage on A9 with Respect to Ground	-2.0V to +14.0V[1]
Vpp Supply Voltage with Respect to Ground	-2.0V to +14.0V[1]
Integrated UV Erase Dose	7258 w•sec/cm²

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is Vcc+0.75V dc which may overshoot to +7.0V for pulses of less than 20ns.

Operating Modes

MODE \ PIN	$\overline{CE}$	$\overline{OE}$/Vpp	Ai	Vcc	Outputs
Read	V_{IL}	V_{IL}	Ai	Vcc	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X[1]	Vcc	High Z
Standby	V_{IH}	X	X	Vcc	High Z
Fast Program[2]	V_{IL}	Vpp	Ai	Vcc	D_{IN}
PGM Verify	V_{IL}	V_{IL}	Ai	Vcc	D_{OUT}
PGM Inhibit	V_{IH}	Vpp	X	Vcc	High Z
Product Identification[4]	V_{IL}	V_{IL}	A9 = V_H [3] A0 = V_{IH} or V_{IL} A1-A15 = V_{IL}	Vcc	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. V_H = 12.0 ± 0.5V.

4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

AT27C512

D.C. and A.C. Operating Conditions for Read Operation

		AT27C512			
		-12	**-15**	**-20**	**-25**
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.		-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 5%	5V ± 10%	5V ± 10%	5V ± 10%

D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	$V_{IN} = -0.1V$ to $V_{CC} + 1V$			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = -0.1V$ to $V_{CC} + 0.1V$			10	μA
I_{SB}	V_{CC} [1] Standby Current	I_{SB1} (CMOS) $\overline{CE} = V_{CC}-0.3$ to $V_{CC}+1.0V$	Com.		100	μA
			Ind.,Mil.		200	μA
		I_{SB2} (TTL) $\overline{CE} = 2.0$ to $V_{CC}+1.0V$	Com.		2	mA
			Ind.,Mil.		3	mA
I_{CC}	V_{CC} Active Current	$f = 5MHz, I_{OUT} = 0mA$, $\overline{CE} = V_{IL}$	Com.		40	mA
			Ind.,Mil.		50	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	$V_{CC}+1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1mA$			.45	V
V_{OH}	Output High Voltage	$I_{OH} = -100\mu A$		$V_{CC}-0.3$		V
		$I_{OH} = -2.5mA$		3.5		V
		$I_{OH} = -400\mu A$		2.4		V

Notes: 1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$, and removed simultaneously or after $\overline{OE}/V_{PP}$.

A.C. Characteristics for Read Operation

				AT27C512								
				-12		**-15**		**-20**		**-25**		
Symbol	Parameter	Condition		Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} [4]	Address to Output Delay	$\overline{CE} = \overline{OE}/V_{PP}$ $= V_{IL}$	Com.		120		150		200		250	ns
			Ind., Mil.				150		200		250	ns
t_{CE} [3]	$\overline{CE}$ to Output Delay	$\overline{OE}/V_{PP} = V_{IL}$			120		150		200		250	ns
t_{OE} [3,4]	$\overline{OE}/V_{PP}$ to Output Delay	$\overline{CE} = V_{IL}$			65		70		75		100	ns
t_{DF} [2,5]	$\overline{OE}/V_{PP}$ or $\overline{CE}$ High to Output Float	$\overline{CE} = V_{IL}$			50		50		55		60	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}/V_{PP}$, whichever occurred first	$\overline{CE} = \overline{OE}/V_{PP}$ $= V_{IL}$		0		0		0		0		ns

Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

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A.C. Waveforms for Read Operation [1]
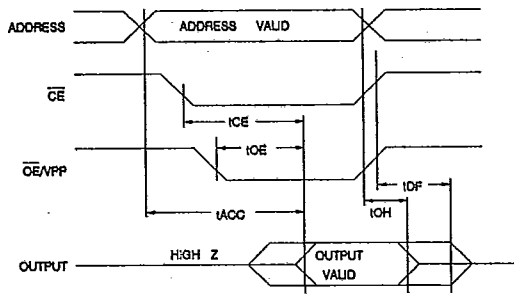
Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC driving levels are 0.45V and 2.4V, unless otherwise specified.
2. t_{DF} is specified from $\overline{OE}$/V_{PP} or $\overline{CE}$, whichever occurs first. Output float is defined as the point when data is no longer driven.
3. $\overline{OE}$/V_{PP} may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. $\overline{OE}$/V_{PP} may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
5. This parameter is only sampled and is not 100% tested.
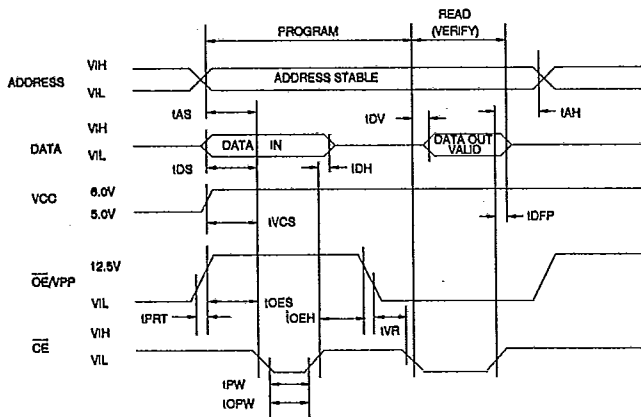
Input Test Waveforms and Measurement Levels

t_R, t_F < 20ns (10% to 90%)
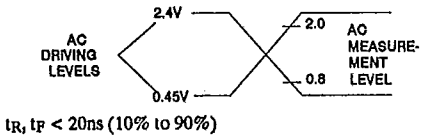
Output Test Load
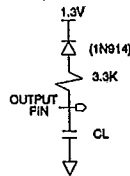
Note: C_L=100pF including jig capacitance.

Pin Capacitance (f = 1MHz T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]

Notes:
1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

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D.C. Programming Characteristics

$T_A=25\pm5^\circ C$, $V_{CC}=6.0\pm0.25V$, $\overline{OE}/V_{PP}=12.5\pm0.5V$

Sym-bol	Parameter	Test Conditions	Limits Min	Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	μA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC}+1$	V
V_{OL}	Output Low Volt.	$I_{OL}=2.1mA$		.45	V
V_{OH}	Output High Volt.	$I_{OH}=-400\mu A$	2.4		V
I_{CC2}	Vcc Supply Current (Program and Verify)			40	mA
I_{PP2}	$\overline{OE}/V_{PP}$ Current	$\overline{CE}=V_{IL}$		25	mA
V_{ID}	A9 Product Iden-tification Voltage		11.5	12.5	V

A.C. Programming Characteristics

$T_A=25\pm5^\circ C$, $V_{CC}=6.0\pm0.25V$, $\overline{OE}/V_{PP}=12.5\pm0.5V$

Sym-bol	Parameter	Test Conditions* (see Note 1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		μs
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time		2		μs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time		2		μs
t_{DS}	Data Setup Time		2		μs
t_{AH}	Address Hold Time		0		μs
t_{DH}	Data Hold Time		2		μs
t_{DFP}	$\overline{CE}$ High to Out-put Float Delay	(Note 2)	0	130	ns
t_{VCS}	Vcc Setup Time		2		μs
t_{PW}	$\overline{CE}$ Initial Program Pulse Width	(Note 3)	0.95	1.05	ms
t_{OPW}	$\overline{CE}$ Overprogram Pulse Width	(Note 4)	2.85	78.75	ms
t_{DV}	Data Valid from $\overline{CE}$	(Note 2)		1	μs
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time		2		μs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming		50		ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) 20ns
Input Pulse Levels .... 0.45V to 2.4V
Input Timing Reference Level .... 0.8V to 2.0V
Output Timing Reference Level .... 0.8V to 2.0V

Notes:

1. Vcc must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Initial Program Pulse width tolerance is 1msec±5%.
4. The length of the overprogram pulse may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.
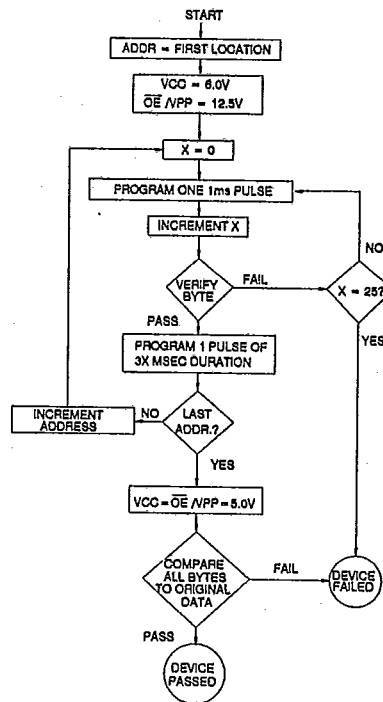
Atmel's 27C512 Integrated Product Identification Code:

Codes	Pins									Hex Data
	A0	O7	O6	O5	O4	O3	O2	O1	O0	
Manufacturer	0	0	0	0	1	1	1	1	1	1F
Device Type	1	0	0	0	0	1	1	0	1	0D

Fast Programming Algorithm

Two $\overline{CE}$ pulse widths are used to program; initial and over-program. Ai are set to address the desired byte. Vcc is raised to 6.0V. The first $\overline{CE}$ pulse is 1ms. The programmed byte is then verified. If the byte programmed successfully, then an overprogram $\overline{CE}$ pulse is applied for 3ms. If the byte fails to program after the first 1ms pulse, then up to 25 successive 1ms pulses are applied with a verification after each pulse. When the byte passes verification, the overprogram pulse width is 3X (times) the number of 1ms pulses required earlier (75ms max).

If the part fails to verify after 25 1ms pulses have been applied, it is considered as failed. After the first byte is programmed, the Ai are set to the next address repeating the algorithm until all required addresses are programmed. Then Vcc is lowered to 5.0V. All bytes subsequently are read to compare with the original data to determine if the device passes or fails.

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Ordering Information

tACC (ns)	ICC (mA) Active	ICC (mA) Standby	Ordering Code	Package	Operation Range
120	40	0.1	AT27C512-12DC AT27C512-12LC	28DW6 32LW	Commercial (0°C to 70°C)
150	40	0.1	AT27C512-15DC AT27C512-15LC AT27C512-15PC AT27C512-15JC	28DW6 32LW 28P6 32J	Commercial (0°C to 70°C)
150	50	0.2	AT27C512-15DI AT27C512-15LI AT27C512-15PI AT27C512-15JI	28DW6 32LW 28P6 32J	Industrial (-40°C to 85°C)
			AT27C512-15DM AT27C512-15LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27C512-15DM/883 AT27C512-15LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
170	50	0.2	AT27C512-17DM/883 AT27C512-17LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	40	0.1	AT27C512-20DC AT27C512-20LC AT27C512-20PC AT27C512-20JC	28DW6 32LW 28P6 32J	Commercial (0°C to 70°C)
200	50	0.2	AT27C512-20DI AT27C512-20LI AT27C512-20PI AT27C512-20JI	28DW6 32LW 28P6 32J	Industrial (-40°C to 85°C)
			AT27C512-20DM AT27C512-20LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27C512-20DM/883 AT27C512-20LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	40	0.1	AT27C512-25DC AT27C512-25LC AT27C512-25PC AT27C512-25JC	28DW6 32LW 28P6 32J	Commercial (0°C to 70°C)
250	50	0.2	AT27C512-25DI AT27C512-25LI AT27C512-25PI AT27C512-25JI	28DW6 32LW 28P6 32J	Industrial (-40°C to 85°C)
			AT27C512-25DM AT27C512-25LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27C512-25DM/883 AT27C512-25LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

Package Type	
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

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