National Semiconductor

February 1988

CD4723BM/CD4723BC Dual 4-Bit Addressable Latch
CD4724BM/CD4724BC 8-Bit Addressable Latch

General Description

The CD4723B is a dual 4-bit addressable latch with common control inputs, including two address inputs (A0, A1), an active low enable input ($\overline{E}$), and an active high clear input (CL). Each latch has a data input (D) and four outputs (Q0–Q3). The CD4724B is an 8-bit addressable latch with three address inputs (A0–A2), an active low enable input ($\overline{E}$), active high clear input (CL), a data input (D) and eight outputs (Q0–Q7).

Data is entered into a particular bit in the latch when that is addressed by the address inputs and the enable ($\overline{E}$) is low. Data entry is inhibited when enable ($\overline{E}$) is high.

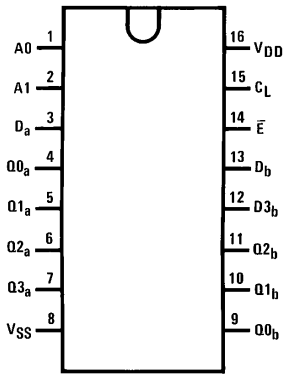
When clear (CL) and enable ($\overline{E}$) are high, all outputs are low. When clear (CL) is high and enable ($\overline{E}$) is low, the channel demultiplexing occurs. The bit that is addressed has an active output which follows the data input while all unaddressed bits are held low. When operating in the addressable latch mode ($\overline{E}$ = CL = low), changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode ($\overline{E}$ = high, CL = low).

Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Serial to parallel capability
- Storage register capability
- Random (addressable) data entry
- Active high demultiplexing capability
- Common active high clear

Connection Diagrams

CD4723B
Dual-In-Line Package



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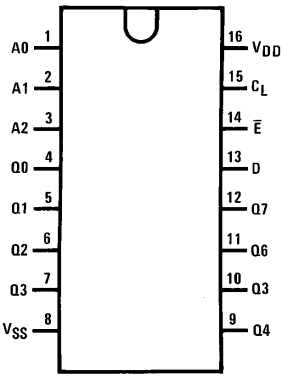
Top View

CD4724B
Dual-In-Line Package



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Top View

Order Number CD4723B or CD4724B

Truth Table

Mode Selection				
$\overline{E}$	CL	Addressed Latch	Unaddressed Latch	Mode
L	L	Follows Data	Holds Previous Data	Addressable Latch
H	L	Hold Previous Data	Holds Previous Data	Memory
L	H	Follows Data	Reset to ''0''	Demultiplexer
H	H	Reset to '0''	Reset to ''0''	Clear

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	$-0.5V$ to $+18$ V_{DC}
Input Voltage (V_{IN})	$-0.5V$ to V_{DD} $+0.5$ V_{DC}
Storage Temperature (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	3.0V to 15 V_{DC}
Input Voltage (V_{IN})	0V to V_{DD} V_{DC}
Operating Temperature Range (T_A)	
CD4723BM/CD4724BM	$-55°C$ to $+125°C$
CD4723BC/CD4724BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4723BM/CD4724BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		5.0		0.02	5.0		150	μA
		$V_{DD} = 10V$		10		0.02	10		300	μA
		$V_{DD} = 15V$		20		0.02	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| \leq 1$ μA								
		$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| \leq 1$ μA								
		$V_{DD} = 5V$	4.95		4.95	5.0		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$		3.0		4.5	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$	7.0		7.0	5.5		7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 4.6V$	-0.64		-0.51	-0.88		-0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	-1.6		-1.3	-2.25		-0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	-4.2		-3.4	-8.8		-2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		-0.1		-10^{-5}	-0.1		-1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OL} and I_{OH} are tested one output at a time.

DC Electrical Characteristics CD4723BC/CD4724BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		20		0.02	20		150	μA
		$V_{DD} = 10V$		40		0.02	40		300	μA
		$V_{DD} = 15V$		80		0.02	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| \leq 1\ \mu A$								
		$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| \leq 1\ \mu A$								
		$V_{DD} = 5V$	4.95		4.95	5.0		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$		3.0		4.5	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$	7.0		7.0	5.5		7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 4.6V$	−0.52		−0.44	−0.88		−0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−1.3		−1.1	−2.25		−0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.30		-10^{-5}	−0.30		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.30		10^{-5}	0.30		1.0	μA

Note 1: ''Absolute Maximum Ratings'' are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of ''Recommended Operating Conditions'' and Electrical Characteristics'' provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OL} and I_{OH} are tested one output at a time.

AC Electrical Characteristics*

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, Input $t_r = t_f = 20$ ns, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Data to Output	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		200 75 50	400 150 100	ns ns ns
t_{PLH}, t_{PHL}	Propagation Delay Enable to Output	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		200 80 60	400 160 120	ns ns ns
t_{PHL}	Propagation Delay Clear to Output	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		175 80 65	350 160 130	ns ns ns
t_{PLH}, t_{PHL}	Propagation Delay Address to Output	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		225 100 75	450 200 150	ns ns ns
t_{THL}, t_{TLH}	Transition Time (Any Output)	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		100 50 40	200 100 80	ns ns ns
T_{WH}, T_{WL}	Minimum Data Pulse Width	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		100 50 40	200 100 80	ns ns ns
t_{WH}, t_{WL}	Minimum Address Pulse Width	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		200 100 65	400 200 125	ns ns ns
t_{WH}	Minimum Clear Pulse Width	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		75 40 25	150 75 50	ns ns ns
t_{SU}	Minimum Setup Time Data to E	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		40 20 15	80 40 30	ns ns ns
t_H	Minimum Hold Time Data to E	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		60 30 25	120 60 50	ns ns ns
t_{SU}	Minimum Setup Time Address to E	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		−15 0 0	50 30 20	ns ns ns
t_H	Minimum Hold Time Address to E	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		−50 −20 −15	15 10 5	ns ns ns
C_{PD}	Power Dissipation Capacitance	Per Package (Note 4)		100		pF
C_{IN}	Input Capacitance	Any Input		5.0	7.5	pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and Electrical Characteristics" provide conditions for actual device operation.

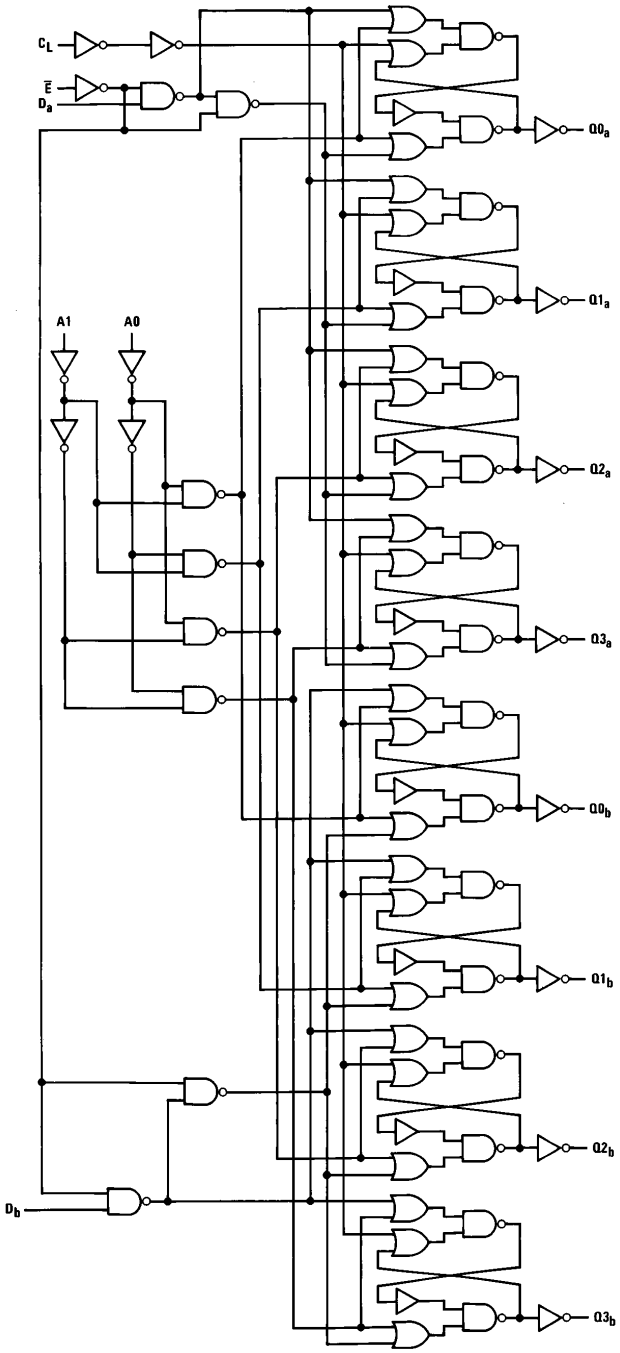
Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OL} and I_{OH} are tested one output at a time.

Note 4: Dynamic power dissipation (P_D) is given by: $P_D = (C_{PD} + C_L) V_{CC}^2 f + P_Q$; where C_L = load capacitance; f = frequency of operation; for further details, see Application Note AN-90, "54C/74C Family Characteristics".

Logic Diagrams

CD4723B



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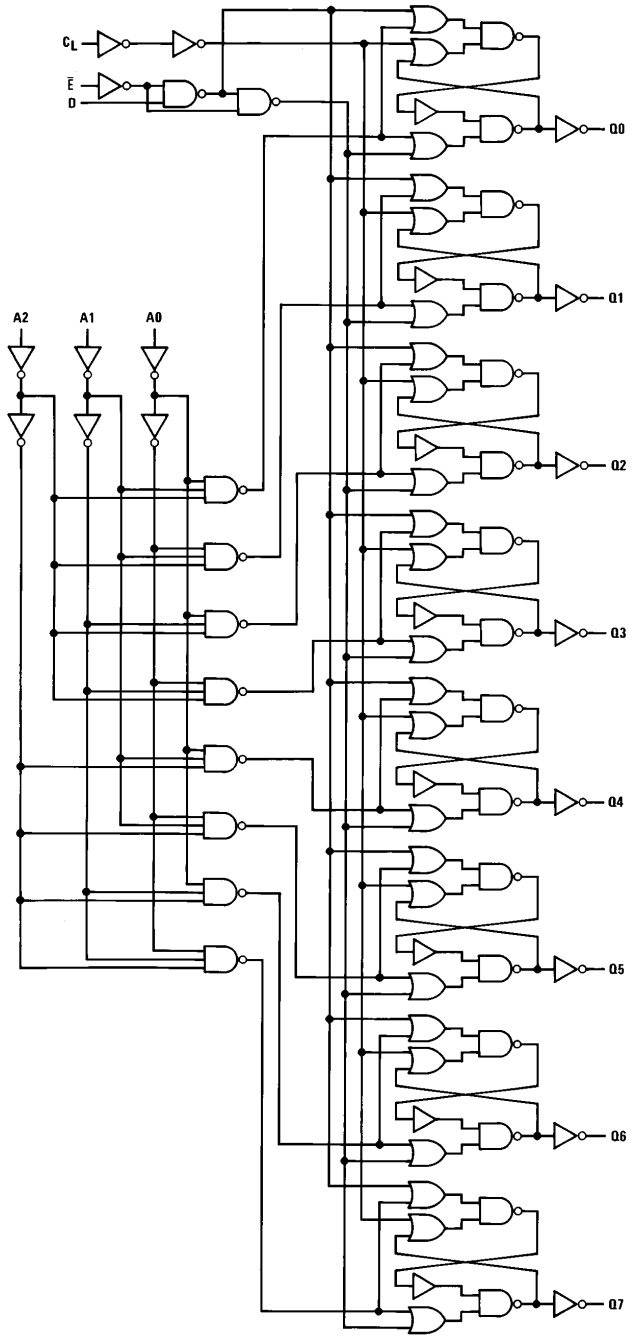
Logic Diagrams (Continued)

CD4724B



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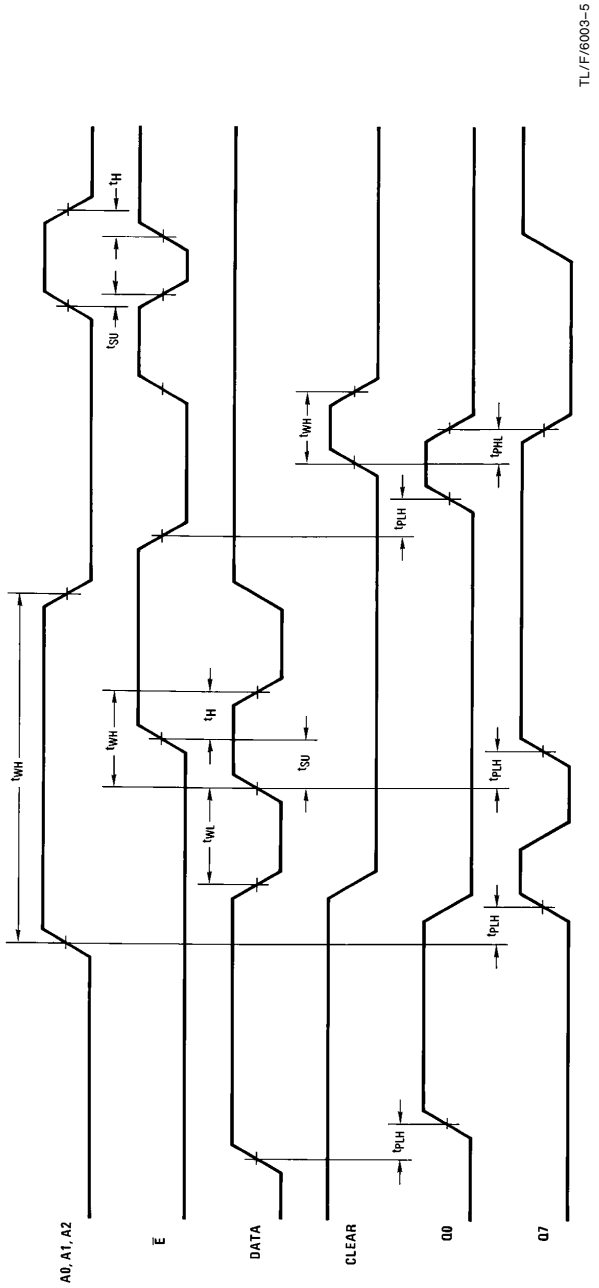
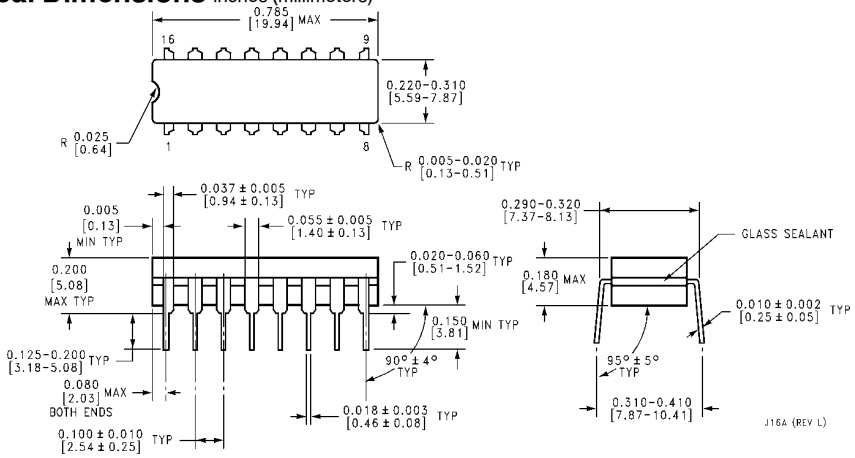
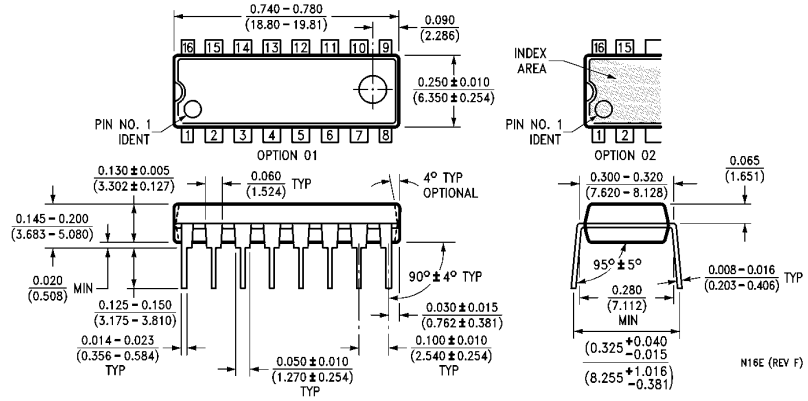
Switching Time Waveforms



Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number CD4723BMJ, CD4723BCJ, CD4724BMJ or CD4724BCJ
NS Package Number J16A



Molded Dual-In-Line Package (N)
Order Number CD4723BMN, CD4723BCN, CD4724BMN or CD4724BCN
NS Package Number N16E

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