CLC425 Ultra Low Noise Wideband Op Amp

Check for Samples: CLC425

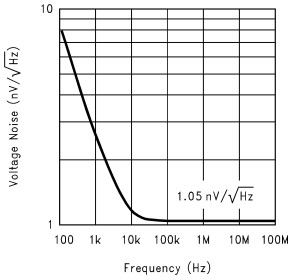
FEATURES

- **1.9GHz gain-bandwidth product**
- **1.05nV/√Hz input voltage noise**
- **0.8pA/√Hz @ I_{CC} ≤ 5mA**
- **100µV input offset voltage, 2µV/°C drift**
- **350V/µs slew rate**
- **15mA to 5mA adjustable supply current**
- **Gain range ±10 to ±1,000V/V**
- **Evaluation boards & simulation macromodel**
- **0.9dB NF @ R_s = 700Ω**

APPLICATIONS

- **Instrumentation sense amplifiers**
- **Ultrasound pre-amps**
- **Magnetic tape & disk pre-amps**
- **Photo diode transimpedance amplifiers**
- **Wide band active filters**
- **Low noise figure RF amplifiers**
- **Professional audio systems**
- **Low noise loop filters for PLLs**

Equivalent Input Voltage Noise



DESCRIPTION

The CLC425 combines a wide bandwidth (**1.9GBW**) with a very low input noise (1.05nV/√Hz, 1.6pA/√Hz) and low dc errors (100µV V_{OS}, 2µV/°C drift) to provide a very precise, wide dynamic range op amp offering closed-loop gains of ≥10.

Singularly suited for very wideband high gain operation, the CLC425 employs a traditional voltage feedback topology providing all the benefits of balanced inputs, such as low offsets and drifts, as well as a 96dB open loop gain, a 100dB CMRR and a 95dB PSRR.

The CLC425 also offers great flexibility with its externally adjustable supply current, allowing designers to easily choose the optimum set of power, bandwidth, noise and distortion performance. Operating from ±5V power supplies, the CLC425 defaults to a 15mA quiescent current, or by adding one external resistor, the supply current can be adjusted to less than 5mA.

The CLC425 combination of ultra low noise, wide gain bandwidth, high slew rate and low dc errors will enable applications in areas such as medical diagnostic ultrasound, magnetic tape & disk storage, communications and opto-electronics to achieve maximum high frequency signal-to-noise ratios.

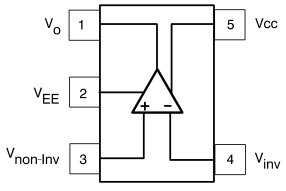
Enhanced Solutions (Military/Aerospace)

SMD Number: 5962-93259

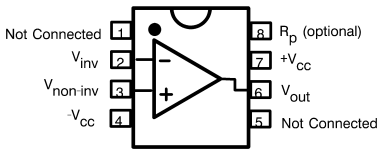
Space level versions also available.

For more information, visit http://www.ti.com

Connection Diagram



See Package Number DCK0005A



See Package Numbers D0008A and P0008E

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage (V_{CC})	±7V
I_{OUT} Output is short circuit protected to ground, but maximum reliability will be maintained if I_{OUT} does not exceed...	125mA
Common Mode Input Voltage	±V_{CC}
Maximum Junction Temperature	+150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Solder Duration (+300°C)	10 sec
ESD rating (human body model)	1000V

(1) “Absolute Maximum Ratings” are those values beyond which the safety of the device are not ensured. They are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” specifies conditions of device operation.

OPERATING RATINGS

Thermal Resistance		
Package	(θ_{JC})	(θ_{JA})
MDIP	70°C/W	125°C/W
SOIC	65°C/W	145°C/W
SOT-23	115°C/W	185°C/W

ELECTRICAL CHARACTERISTICS

A_V= +20, V_{CC} = ±5V, R_g = 26.1Ω, R_L = 100Ω, R_f = 499Ω; unless specified

Symbol	Parameter	Conditions	Typ	Min/Max (1)			Units
Ambient Temperature		CLC425AJ	+25°C	−40°C	+25°C	+85°	
Frequency Domain Response							
GBW	Gain Bandwidth Product	V_{OUT} < 0.4V_{PP}	1.9	1.5	1.5	1.0	GHz
SSBW	-3dB Bandwidth	V_{OUT} < 0.4V_{PP}	95	75	75	50	MHz
LSBW		V_{OUT} < 5.0V_{PP}	40	30	30	20	MHz
	Gain Flatness	V_{OUT}< 0.4V_{PP}					
GFP	Peaking	DC to 30MHz	0.3	0.7	0.5	0.7	dB
GFR	Rolloff	DC to 30MHz	0.1	0.7	0.5	0.7	dB
LPD	Linear Phase Deviation	DC to 30MHz	0.7	1.5	1.5	2.5	deg
Time Domain Response							
TRS	Rise and Fall Time	0.4V Step	3.7	4.7	4.7	7.0	ns
TSS	Settling Time to 0.2%	2V Step	22	30	30	40	ns
OS	Overshoot	0.4V Step	5	12	10	12	%
SR	SlewRate	2V Step	350	250	250	200	V/µs
Distortion And Noise Response							
HD2	2nd Harmonic Distortion	1V_{PP}, 10MHz	−53	48	48	46	dBc
HD3	3rd Harmonic Distortion	1V_{PP}, 10MHz	−75	65	65	60	dBc
IMD	3rd Order Intermodulation Intercept	10MHz	35				dBm
	Equivalent Input Noise						
VN	Voltage	1MHz to 100MHz	1.05	1.25	1.25	1.8	nV/√Hz
ICN	Current	1MHz to 100MHz	1.6	4.0	2.5	2.5	pA/√Hz
NF	Noise Figure	R_s = 700Ω	0.9				dB
Static, DC Performance							
AOL	Open Loop Gain	DC	96	77	86	86	dB
VIO	Input Offset Voltage (2)		±100	±1000	±800	±1000	µV
DVIO	Average Drift		±2	8	-	4	µV/°C
IB	Input Bias Current (2)	Non-Inverting	12	40	20	20	µA
DIB	Average Drift		−100	−250	-	−120	nA/°C
IIO	Input Offset Current		±0.2	3.4	2.0	2.0	µA
DIIO	Average Drift		±3	±50	-	±25	nA/C°
PSRR	Power Supply Rejection Ratio	DC	95	82	88	86	dB
CMRR	Common Mode Rejection Ratio	DC	100	88	92	90	dB
ICC	Supply Current (2)	RL = ∞	15	18	16	16	mA
Miscellaneous Performance							
RINC	Input Resistance	Common-Mode	2	0.6	1.6	1.6	MΩ
RIND		Differential-Mode	6	1	3	3	kΩ
CINC	Input Capacitance	Common-Mode	1.5	2	2	2	pF
CIND		Differential-Mode	1.9	3	3	3	pF
ROUT	Output Resistance	Closed Loop	5	50	10	10	mΩ
VO	Output Voltage Range	R_L = ∞	±3.8	±3.5	±3.7	±3.7	V
VOL		R_L = 100Ω	±3.4	±2.8	±3.2	±3.2	V
CMIR	Input Voltage Range	Common Mode	±3.8	±3.4	±3.5	±3.5	V
IOP	Output Current	Source	80	70	70	70	mA
ION		Sink	90	45	55	55	mA

(1) Max/min ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.
(2) AJ-level: spec. is 100% tested at +25°C, sample at 85°C.

TYPICAL PERFORMANCE CHARACTERISTICS

Non-Inverting Frequency Response

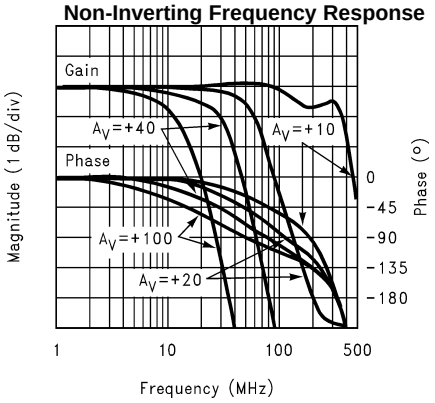


Figure 1.

Inverting Frequency Response

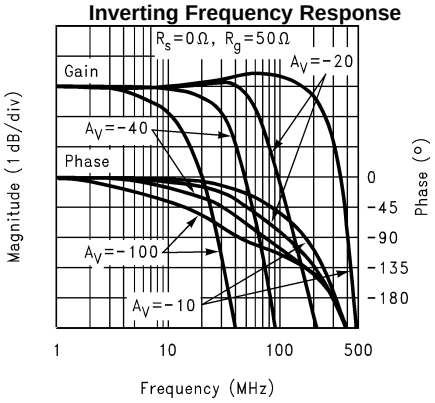


Figure 2.

Frequency Response vs. I_{CC} (A_V = +20)

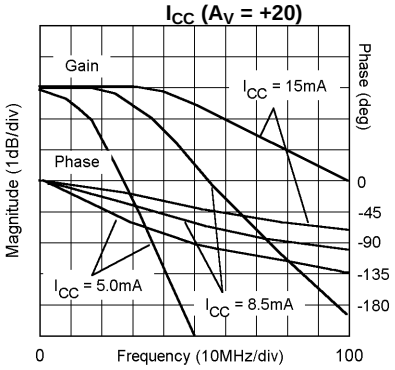


Figure 3.

Open Loop Gain and Phase vs. I_{CC}

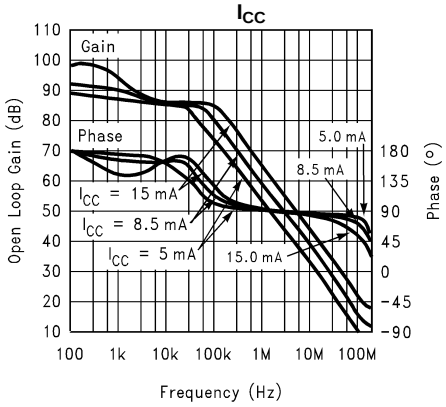


Figure 4.

Open Loop Gain and Phase vs. R_L

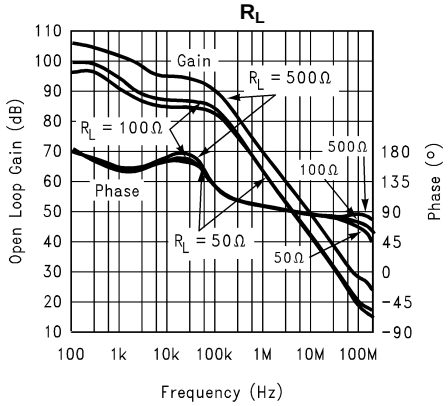


Figure 5.

Open Loop Gain and Phase vs. Temp

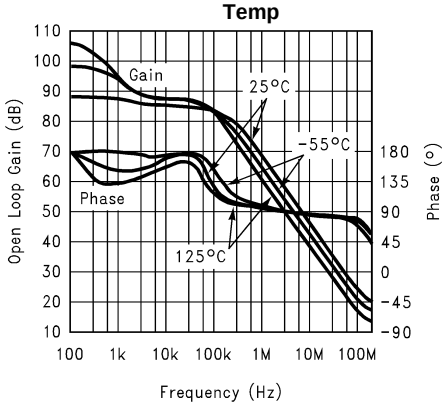


Figure 6.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Non-Inverting Response (I_{CC} = 5.0mA)

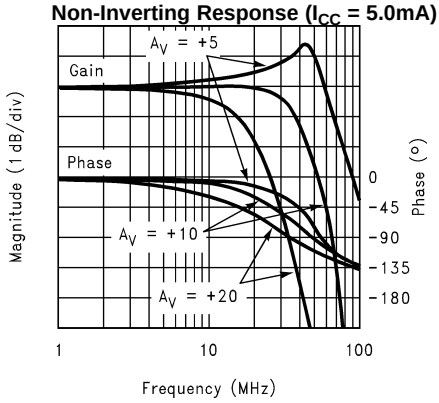


Figure 7.

Frequency Response for Various R_Ls

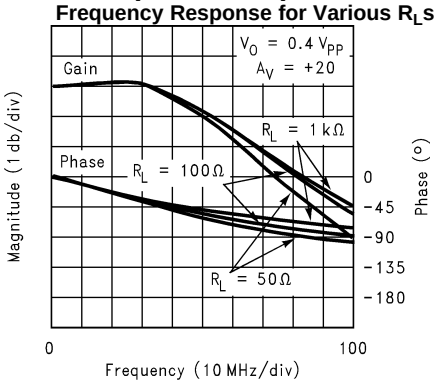


Figure 8.

Gain Flatness & Linear Phase Deviation

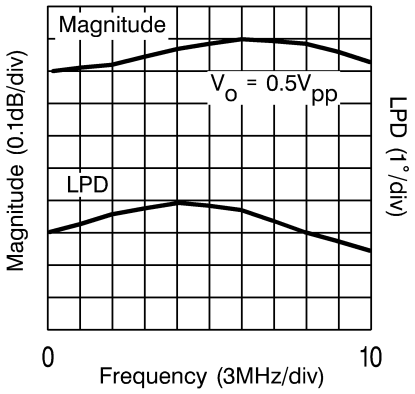


Figure 9.

Equivalent Input Noise

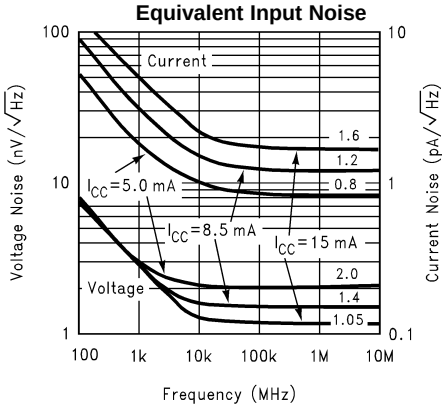


Figure 10.

Maximum Output Swing vs. Frequency

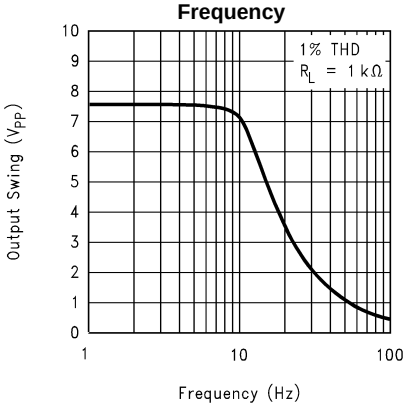


Figure 11.

Closed-Loop Output Impedance

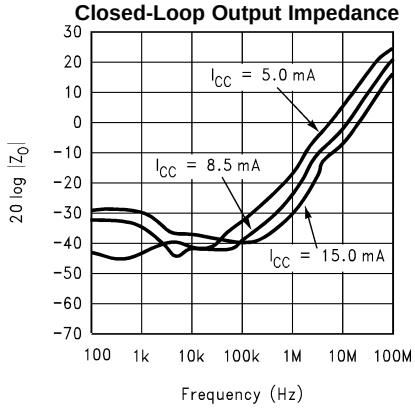


Figure 12.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

CMRR vs. Common-Mode Input Voltage

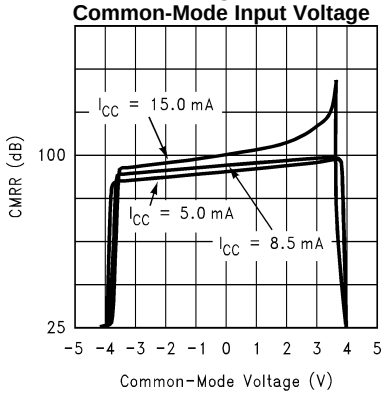


Figure 13.

Common-Mode Input Transimpedance

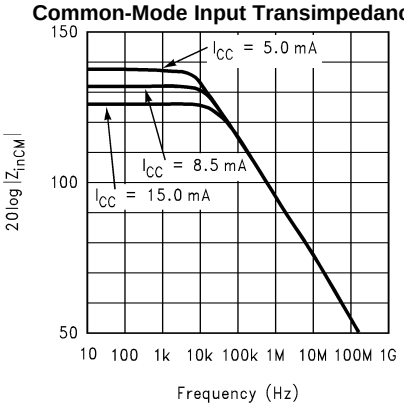


Figure 14.

Differential Input Impedance

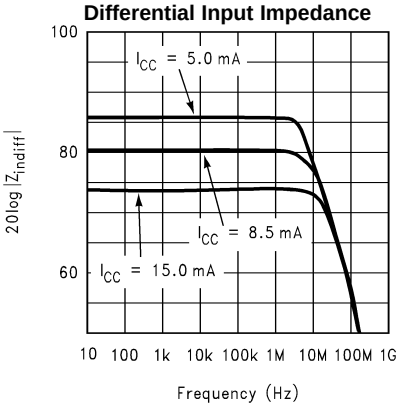


Figure 15.

Pulse Response ($V_O1 = V_{PP}$)

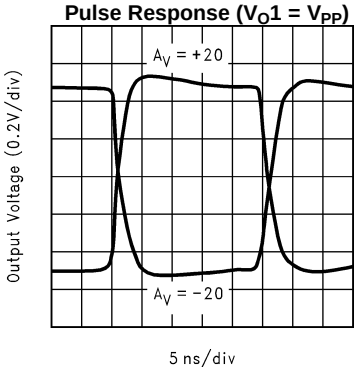


Figure 16.

Large Signal Pulse Response ($V_O1 = V_{PP}$)

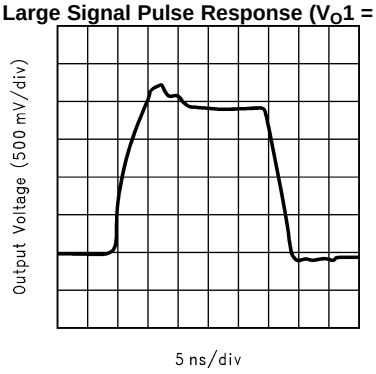


Figure 17.

Settling Time vs. Gain

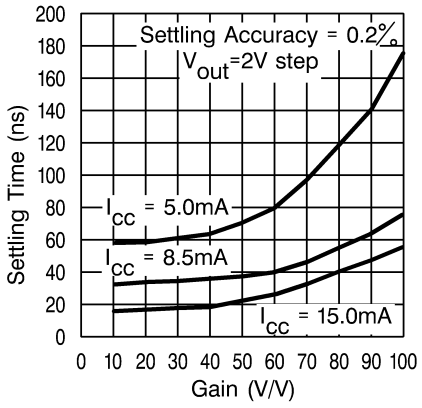


Figure 18.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Short Term Settling Time

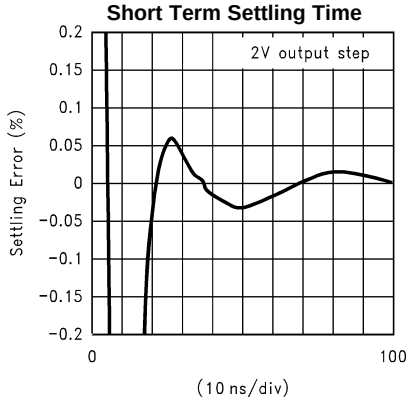


Figure 19.

Long Term Settling Time

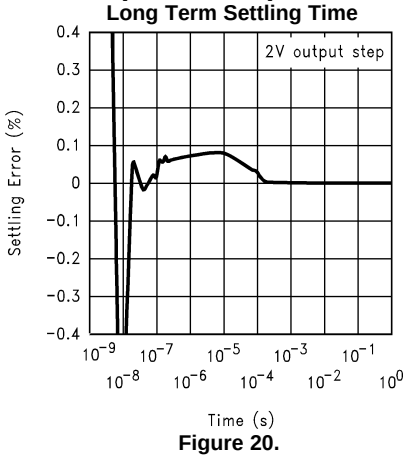


Figure 20.

Settling Time vs. C_L and R_S

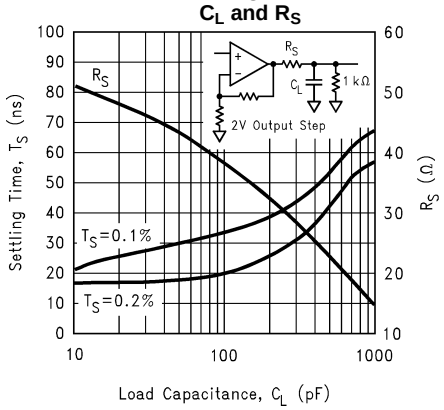


Figure 21.

Supply Current Range vs. R_p

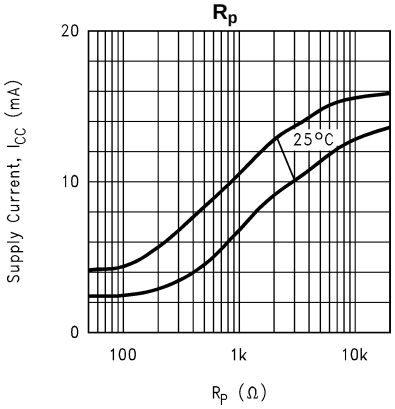


Figure 22.

Gain-Bandwidth Product vs. I_{CC}

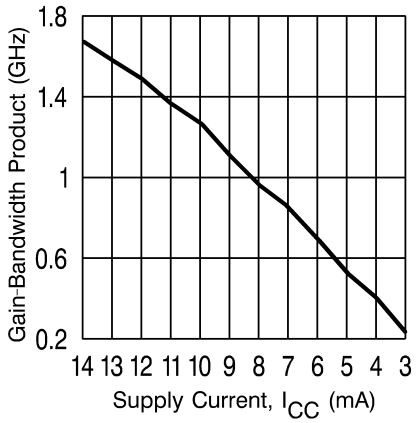


Figure 23.

Differential Gain and Phase (4.43MHz)

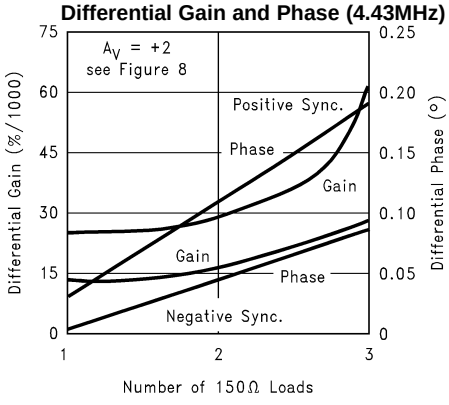


Figure 24.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

2nd and 3rd Harmonic Distortion ($V_O1 = V_{PP}$)

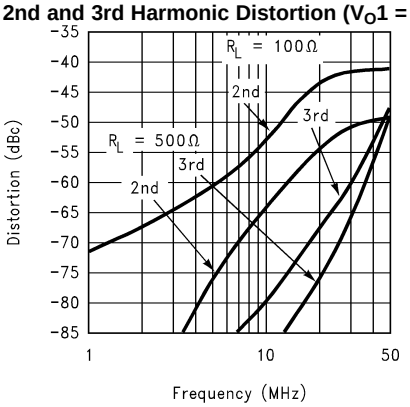


Figure 25.

Distortion vs. Gain & I_{CC} ($V_O1 = V_{PP}$ f_O = 3MHz)

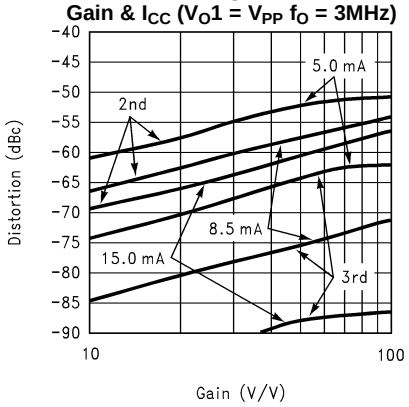


Figure 26.

2-Tone, 3rd Order Intermodulation Intercept

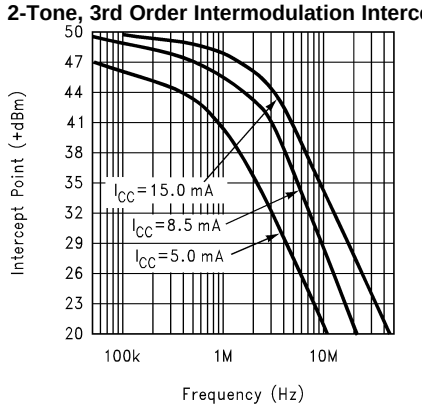


Figure 27.

Output Voltage vs. Load

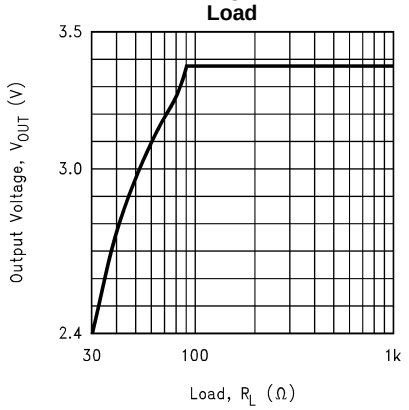


Figure 28.

CMRR and PSRR

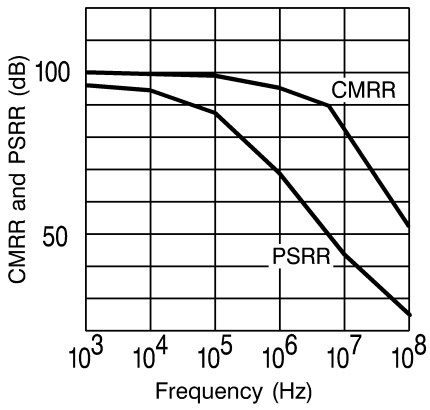


Figure 29.

Typical DC Errors vs. Temperature

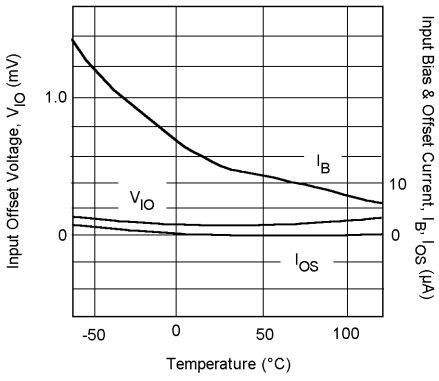


Figure 30.

APPLICATION INFORMATION

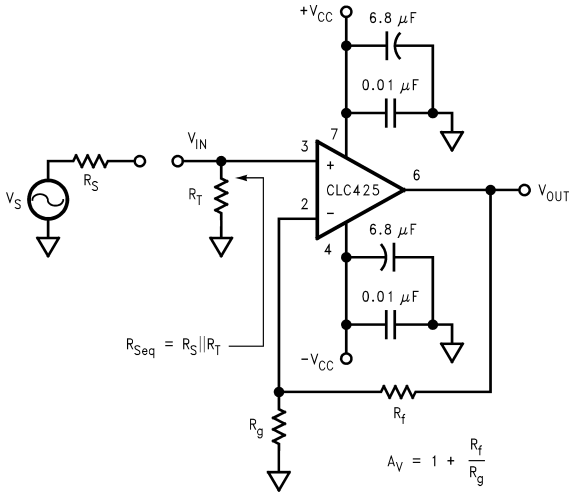


Figure 31. Non-Inverting Amplifier Configuration

Introduction

The CLC425 is a very wide gain bandwidth, ultra low noise voltage feedback operational amplifier which enables application areas such as medical diagnostic ultrasound, magnetic tape & disk storage and fiber-optics to achieve maximum high frequency signal-to-noise ratios. The set of characteristic plots located in the “Typical Performance” section illustrates many of the performance trade offs. The following discussion will enable the proper selection of external components in order to achieve optimum device performance.

Bias Current Cancellation

In order to cancel the bias current errors of the non-inverting configuration, the parallel combination of the gain setting (R_g) and feedback (R_f) resistors should equal the equivalent source resistance (R_{seq}) as defined in Figure 31. Combining this constraint with the non-inverting gain equation also seen in Figure 31, allows both R_f and R_g to be determined explicitly from the following equations:

$$R_f = A_V R_{seq} \text{ and } R_g = R_f/(A_V - 1). \quad (1)$$

When driven from a 0Ω source, such as that from the output of an op amp, the non-inverting input of the CLC425 should be isolated with at least a 25Ω series resistor.

As seen in Figure 32, bias current cancellation is accomplished for the inverting configuration by placing a resistor (R_b) on the non-inverting input equal in value to the resistance seen by the inverting input ($R_f \| (R_g + s)$). R_b is recommended to be no less than 25Ω for best CLC425 performance. The additional noise contribution of R_b can be minimized through the use of a shunt capacitor.

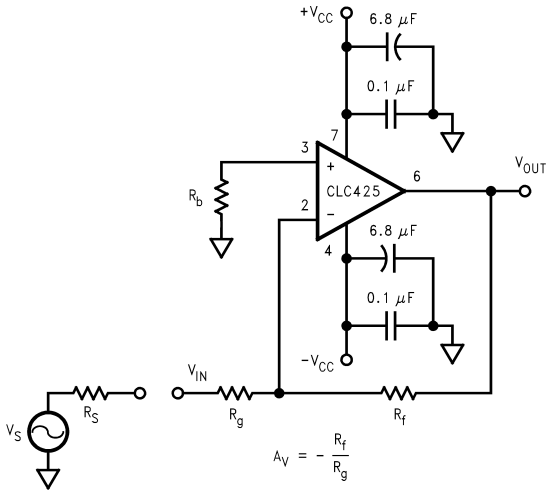


Figure 32. Inverting Amplifier Configuration

Total Input Noise vs. Source Resistance

In order to determine maximum signal-to-noise ratios from the CLC425, an understanding of the interaction between the amplifier's intrinsic noise sources and the noise arising from its external resistors is necessary.

Figure 33 describes the noise model for the non-inverting amplifier configuration showing all noise sources. In addition to the intrinsic input voltage noise (e_n) and current noise ($i_n = i_{n+} = i_{n-}$) sources, there also exists thermal voltage noise:

($e_t = \sqrt{Hz}\ 4kTR$)

associated with each of the external resistors. Equation 2 provides the general form for total equivalent input voltage noise density (e_{ni}). Equation 3 is a simplification of Equation 2 that assumes

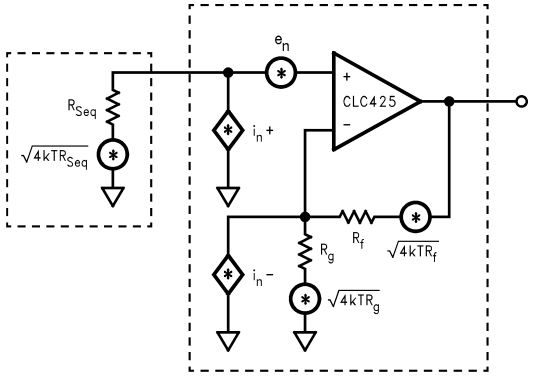


Figure 33. Non-inverting Amplifier Noise Model

$$e_{ni} = \sqrt{e_n^2 + \left(i_{n+} R_{Seq}\right)^2 + 4kTR_{Seq} + \left(i_{n-}\left(R_f \| R_g\right)\right)^2 + 4kT\left(R_f \| R_g\right)} \quad (2)$$

$R_f \| R_g = R_{seq}$ for bias current cancellation. Figure 34 illustrates the equivalent noise model using this assumption. Figure 35 is a plot of e_{ni} against equivalent source resistance (R_{seq}) with all of the contributing voltage noise source of Equation 2 shown. This plot gives the expected e_{ni} for a given (R_{seq}) which assumes $R_f \| R_g = R_{seq}$ for bias current cancellation. The total equivalent output voltage noise (e_{n0}) is e_{ni} x A_v.

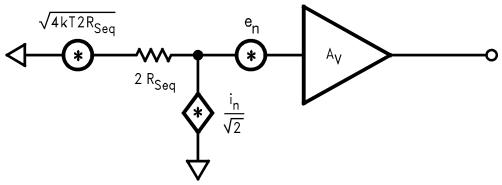


Figure 34. Noise Model with R_f‖R_g = R_{seq}

$$e_{ni} = \sqrt{e_n^2 + 2(i_n R_{Seq})^2 + 4kT(2R_{Seq})} \quad (3)$$

As seen in Figure 35, e_{ni} is dominated by the intrinsic voltage noise (e_n) of the amplifier for equivalent source resistances below 33.5Ω. Between 33.5Ω and 6.43kΩ, e_{ni} is dominated by the thermal noise (e_t= $\sqrt{Hz}$ 4kTR_{seq}) of the external resistor. Above 6.43kΩ, e_{ni} is dominated by the amplifier's current noise ($\sqrt{Hz}$ 2$i_n R_{seq}$). The point at which the CLC425's voltage noise and current noise contribute equally occurs for R_{seq}=464Ω (i.e., $e_n/\sqrt{Hz}$ 2i_n). As an example, configured with a gain of +20V/V giving a -3dB of 90MHz and driven from an R_{seq}= 25Ω, the CLC425 produces a total equivalent input noise voltage (e_{ni} × $\sqrt{Hz}$ 1.57 x 90MHz) of 16.5μV_{rms}.

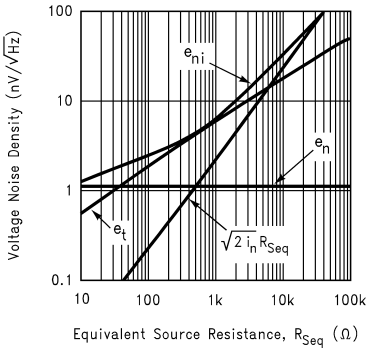


Figure 35. Voltage Noise Density vs. Source Resistance

If bias current cancellation is not a requirement, then R_f‖R_g does not need to equal R_{seq}. In this case, according to Equation 1, $R_f R_g$ should be as low as possible in order to minimize noise. Results similar to Equation 1 are obtained for the inverting configuration of Figure 32 if R_{seq} is replaced by R_b and R_g is replaced by R_g+R_s. With these substitutions, Equation 1 will yield an e_{ni} referred to the non-inverting input. Referring e_{ni} to the inverting input is easily accomplished by multiplying e_{ni} by the ratio of non-inverting to inverting gains.

Noise Figure

Noise Figure (NF) is a measure of the noise degradation caused by an amplifier.

$$NF = 10LOG\left\{\frac{S_i / N_i}{S_o / N_o}\right\} = 10LOG\left\{\frac{e_{ni}^2}{e_t^2}\right\} \quad (4)$$

The Noise Figure formula is shown inEquation 3. The addition of a terminating resistor R_T, reduces the external thermal noise but increases the resulting NF. The NF is increased because R_T reduces the input signal amplitude thus reducing the input SNR.

$$NF = 10LOG\left(\frac{e_n^2 + i_n^2\left(R_{Seq} + \left(R_f \| R_g\right)^2\right) + 4kTR_{Seq} + 4kT\left(R_f \| R_g\right)}{4kTR_{Seq}}\right) \quad (5)$$

The noise figure is related to the equivalent source resistance (R_{seq}) and the parallel combination of R_f and R_g. To minimize noise figure, the following steps are recommended:

- Minimize R_f‖R_g
- Choose the Optimum R_S ($_{OPT}$)

R_{OPT} is the point at which the NF curve reaches a minimum and is approximated by:

$R_{OPT} \cong e_n/i_n$

Figure 36 is a plot of NF vs R_s with R_fR_g=9.09(A_v= +10). The NF curves for both Unterminated and Terminated systems are shown. The Terminated curve assumes R_s=R_T. The table indicates the NF for various source resistances including R_s=R_{OPT}.

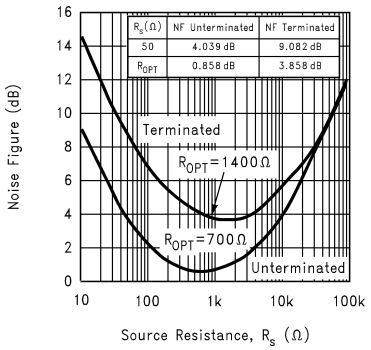


Figure 36. Noise Figure vs. Source Resistance

Supply Current Adjustment

The CLC425's supply current can be externally adjusted downward from its nominal value by adding an optional resistor (R_p) between pin 8 and the negative supply as shown in Figure 37. Several of the plots found within the plot pages demonstrate the CLC425's behavior at different supply currents. The plot labeled "I_{cc} vs R_p" provides the means for selecting R_p and shows the results of standard IC process variation which is bounded by the 25°C curve.

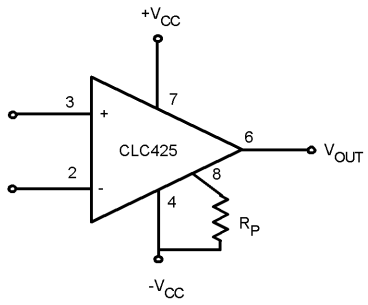


Figure 37. External Supply Current Adjustment

Non-Inverting Gains Less Than 10V/V

Using the CLC425 at lower non-inverting gains requires external compensation such as the shunt compensation as shown in Figure 38. The quiescent supply current must also be reduced to 5mA with R_p for stability. The compensation capacitors are chosen to reduce frequency response peaking to less than 1dB. The plot in the "Typical Performance" section labeled "differential gain and Phase" shows the video performance of the CLC425 with this compensation circuitry.

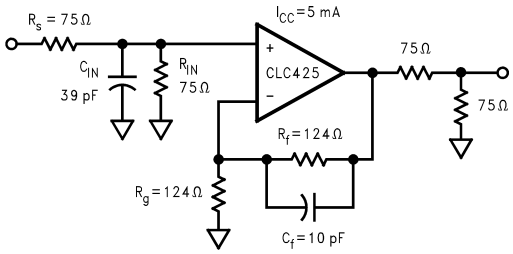


Figure 38. External Shunt Compensation

Inverting Gains Less Than 10V/V

The lag compensation of Figure 39 will achieve stability for lower gains. Placing the network between the two input terminals does not affect the closed-loop nor noise gain, but is best used for the inverting configuration because of its affect on the non-inverting input impedance.

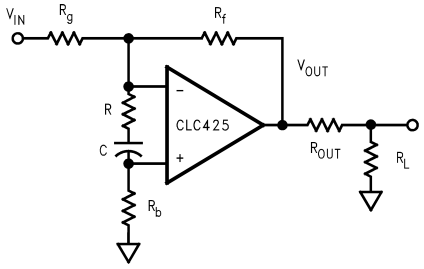


Figure 39. External Lag Compensation

Single-Supply Operation

The CLC425 can be operated with single power supply as shown in Figure 40. Both the input and output are capacitively coupled to set the dc operating point.

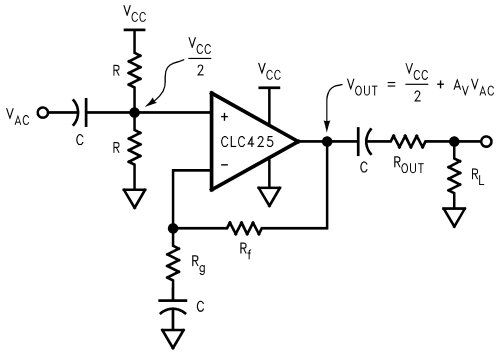


Figure 40. Single Supply Operation

Low Noise Transimpedance Amplifier

The circuit of Figure 41 implements a low-noise transimpedance amplifier commonly used with photo-diodes. The transimpedance gain is set by R_f. The simulated frequency response is shown in Figure 42 and shows the influence C_f has over gain flatness. Equation 4 provides the total input current noise density (i_{ni}) equation for the basic transimpedance configuration and is plotted against feedback resistance (R_f) showing all contributing noise sources in Figure 43. This plot indicates the expected total equivalent input current noise density (i_{ni}) for a given feedback resistance (R_f). The total equivalent output voltage noise density (e_{no}) is i_{ni} x R_f.

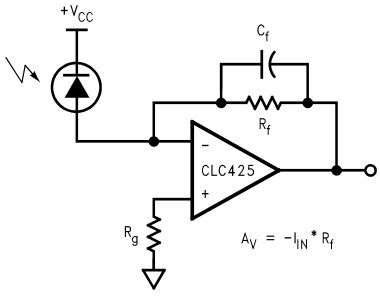


Figure 41. Transimpedance Amplifier Configuration

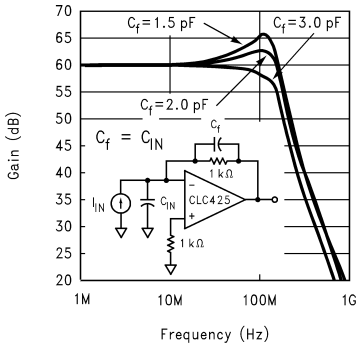


Figure 42. Transimpedance Amplifier Frequency Response

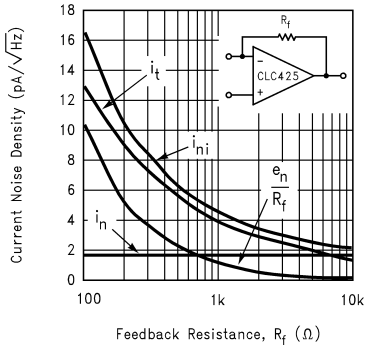


Figure 43. Current Noise Density vs. Feedback Resistance

$$i_{ni} = \sqrt{i_n^2 + \left(\frac{e_n}{R_f}\right)^2 + \frac{4kT}{R_f}} \quad (6)$$

Very Low Figure Amplifier

The circuit of Figure 44 implements a very low Noise Figure amplifier using a step-up transformer combined with a CLC425 and a CLC404. The circuit is configured with a gain of 35.6dB. The circuit achieves measured Noise Figures of less than 2.5dB in the 10-40MHz region, 3rd order intercepts exceed +30dB for frequencies less than 40MHz and gain flatness of 0.5dB is measured in the 1-50MHz passbands. Application Note OA-14 provides greater detail on these low Noise Figure techniques.

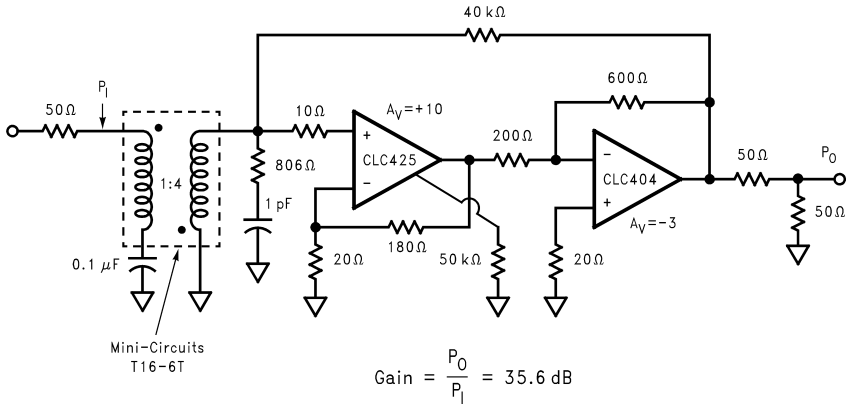


Figure 44. Very Noise Figure Amplifier

Low Noise Integrator

The CLC425 implements a deBoo integrator shown in Figure 45. Integration linearity is maintained through positive feedback. The CLC425's low input offset voltage and matched inputs allowing bias current cancellation provide for very precise integration. Stability is maintained through the constraint on the circuit elements.

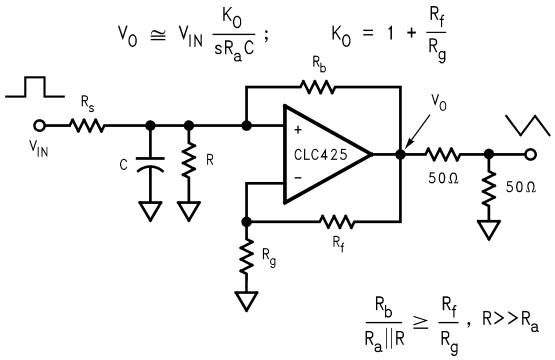


Figure 45. Low Noise Integrator

High-Gain Sallen-Key Active Filters

The CLC425 is well suited for high gain Sallen-Key type of active filters. Figure 46 shows the 2nd order Sallen-Key low pass filter topology. Using component predistortion methods as discussed in OA-21 enables the proper selection of components for these high-frequency filters.

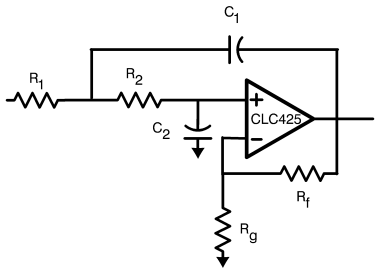
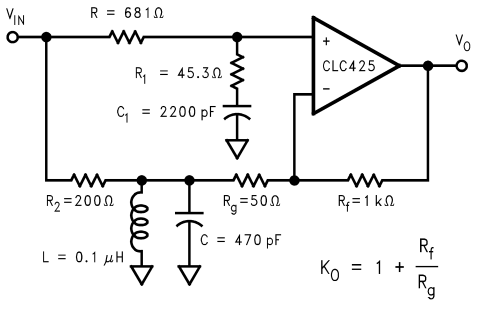


Figure 46. Sallen-Key Active Filter Topology

Low Noise Magnetic Media Equalizer

The CLC425 implements a high-performance low noise equalizer for such applications as magnetic tape channels as shown in Figure 47. The circuit combines an integrator with a bandpass filter to produce the low noise equalization. The circuit's simulated frequency response is illustrated in Figure 48.



$$\frac{V_O}{V_{IN}} = K_O \left(\frac{sC_1R_1 + 1}{sC_1(R_1 + R) + 1} - \left(\frac{R_f}{R_f + R_g} \right) \frac{sLR_g}{s^2LCR_2R_g + sL(R_2 + R_g) + R_2R_g} \right)$$

Figure 47. Low Noise Magnetic Media Equalizer

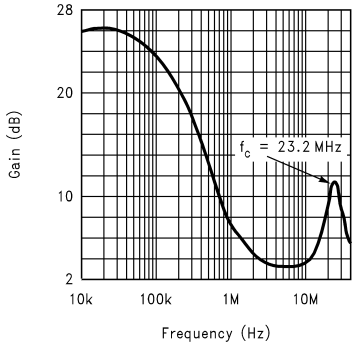


Figure 48. Equalizer Frequency Response

Low-Noise Phase-Locked Loop Filter

The CLC425 is extremely useful as a Phase-Locked Loop filter in such applications as frequency synthesizers and data synchronizers. The circuit of Figure 49 implements one possible PLL filter with the CLC425.

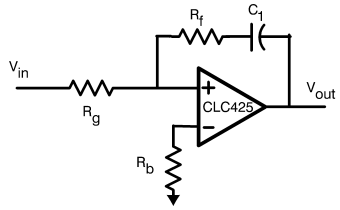


Figure 49. Phase-Locked Loop Filter

Decreasing the Input Noise Voltage

The input noise voltage of the CLC425 can be reduced from its already low 1.05nV/$\sqrt{Hz}$ by slightly increasing the supply current. Using a 50kΩ resistor to ground on pin 8, as shown in the circuit of Figure 44, will increase the quiescent current to ≈17mA and reduce the input noise voltage to

<0.95nV/$\sqrt{Hz}$

Printed Circuit Board Layout

Generally, a good high-frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillation, see OA-15 for more information. National suggests the CLC730013-DIP, CLC730027-SOIC, or CLC730068-SOT evaluation board as a guide for high frequency layout and as an aid in device testing and characterization.

REVISION HISTORY

Changes from Revision G (April 2013) to Revision H	Page
• Changed layout of National Data Sheet to TI format	16

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