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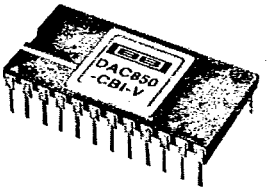
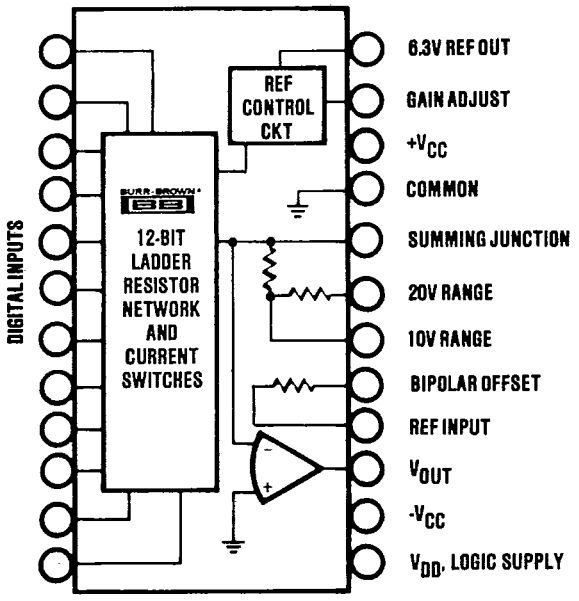


DAC850
DAC851

Integrated Circuit
DIGITAL-TO-ANALOG CONVERTER

FEATURES

- LOW COST HIGH RELIABILITY SINGLE-CHIP REPLACEMENT FOR DAC85 AND DAC87
- 12-BIT RESOLUTION
- HIGH ACCURACY: ±1/2LSB max nonlinearity
  −25°C to +85°C (DAC850)
  −55°C to +125°C (DAC851)
- GUARANTEED MONOTONICITY
- HERMETIC PACKAGES
- GUARANTEED SPECIFICATIONS WITH ±12V AND ±15V SUPPLIES



DESCRIPTION

The DAC850 and DAC851 are 12-bit single-chip (current output model) digital-to-analog converters for use in wide temperature high reliability applications.

The DAC850 and DAC851 are packaged in hermetically-sealed dual in-line packages. The DAC850 is specified with a linearity error of ±1/2LSB over −25°C to +85°C and the DAC851 has a linearity error of ±3/4LSB over −55°C to +125°C. Both converters have guaranteed monotonicity over their specification temperature range. The current output configuration of these D/A converters is a single-chip integrated circuit containing a subsurface zener reference diode, high-speed current switches, and laser-trimmed thin-film resistors.

The DAC850 and DAC851 provide output voltage ranges of ±2.5V, ±5V, ±10V, 0 to +5 and 0 to +10V (V models) or output current ranges of ±1.175mA or 0 to -2.35mA (I models).

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SPECIFICATIONS

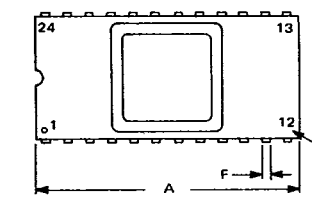
ELECTRICAL

At 25°C and $\pm V_{CC}$ = 12V or 15V unless otherwise noted.

MODEL	DAC850-CBI MIN	DAC850-CBI TYP	DAC850-CBI MAX	DAC851-CBI MIN	DAC851-CBI TYP	DAC851-CBI MAX	UNITS
INPUT							
DIGITAL INPUT							
Resolution			12			12	Bits
Logic Levels (LSTTL Compatible)[1]							
Logic "1" (at +20µA)	+2		+5.5	+2		+5.5	VDC
Logic "0" (at 0.36mA)	0		+0.8	0		+0.8	VDC
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error		±1/4	±1/2		±1/4	±1/2	LSB
Differential Linearity Error		±1/2	+1, −3/4		±1/2	+1, −3/4	LSB
Gain Error[2]		±0.1	±0.2		±0.1	±0.2	%
Offset Error[2]		±0.05	±0.15		±0.05	±0.15	% of FSR[3]
Power Supply Sensitivity							
+15V and +5V Supplies		±0.0001	±0.001		±0.0001	±0.001	% of FSR/%V_{CC}
−15V Supply		±0.003	±0.006		±0.003	±0.006	% of FSR/%V_{CC}
DRIFT[4] (over spec. temp range)							
Bipolar Drift							
(± full scale drift for the bipolar connection)		±5	±17		±15	±30	ppm of FSR/°C
Total Error[5]: Unipolar		±0.1	±0.20		±0.15	±0.30	% of FSR
Bipolar		±0.06	±0.12		±0.15	±0.30	% of FSR
Gain		±10	±20		±10	±25	ppm/°C
Offset: Unipolar		±1	±3		±1	±3	ppm of FSR/°C
Bipolar		±5	±10		±5	±15	ppm of FSR/°C
Differential Linearity (over spec. temp range)		±1/2	±1		±1/2	±1	LSB
Linearity Error (over spec. temp. range)			±1/2			±1/2	LSB
Monotonicity Temp. Range, min	−25		+85	−55		+125	°C
CONVERSION SPEED							
V Model (settling time to ±0.01% of FSR)							
For FSR Change: 20V Range, 2kΩ Load		3	5		3	5	µsec
10V Range, 2kΩ Load		2.5	4		2.5	4	µsec
For 1LSB Change, Major Carry, 2kΩ Load		1.5			1.5		µsec
Slew Rate, 2kΩ Load	10	15		10	15		V/µsec
I Model (settling time to ±0.01% of FSR)							
For FSR Change: 10Ω to 100Ω Load		300			300		nsec
1kΩ Load		1			1		µsec
OUTPUT							
ANALOG OUTPUT							
V Model							
Ranges ($\pm V_{CC}$ = 15V)		±2.5, ±5, ±10, 0 to +5, 0 to +10			±2.5, ±5, ±10, 0 to +5, 0 to +10		V
Output Current[6]		±5			±5		mA
Output Impedance (DC)		0.05			0.05		Ω
Short Circuit to Common, Duration		Indefinite			Indefinite		
I Model							
Ranges	±0.88, 0 to −1.76	±1.175, 0 to −2.35	±1.47, 0 to −2.94	±0.88, 0 to −1.76	±1.175, 0 to −2.35	±1.47, 0 to −2.94	mA
Output Impedance: Bipolar	2.5	3.1	3.7	2.5	3.1	3.7	kΩ
Unipolar	5.8	7.2	8.6	5.8	7.2	8.6	kΩ
Compliance	−2.5		+2.5	−2.5		+2.5	V
POWER SUPPLIES AND REFERENCE							
Reference Voltage Output	+6.23	+6.3	+6.37	+6.23	+6.3	+6.37	V
Current (for external loads), Source	1.5	2.5		1.5	2.5		mA
Temperature Coefficient of Drift		±10	±20		±10	±25	ppm/°C
Power Supply Requirements: $\pm V_{CC}$	±11.4	±15	±16.5	±11.4	±15	±16.5	VDC
V_{DD}[7]	+4.5	+5	+16.5	+4.5	+5	+16.5	VDC
Power Supply Drain: $\pm V_{CC}$ (no load)		+8, −20	+12, −25		+8, −20	+12, −25	mA
V_{DD} (logic supply)		+7	+10		+7	+10	mA
PHYSICAL CHARACTERISTICS							
TEMPERATURE RANGE							
Specification	−25		+85	−55		+125	°C
Storage	−65		+150	−65		+150	°C
PACKAGE	24-pin hermetic DIP side-brazed ceramic						

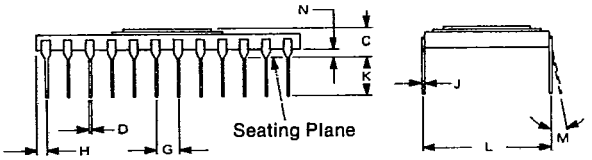
NOTES: (1) Adding external CMOS hex buffers CD 4094A/4050A will provide CMOS input compatibility. Refer to Logic Input Compatibility section. (2) Adjustable to zero with external trim potentiometer. (3) FSR means "Full Scale Range" and is 20V for ±10V range, 10V for ±5V range, etc. (4) To maintain drift spec, internal feedback resistors must be used for current output models. (5) Includes the effects of gain, offset and linearity drift. Gain and offset errors are adjusted to zero at +25°C. (6) For operation of −V models with supply voltages of less than ±13VDC, load current must be limited to ±1mA max, at V_{OUT} = ±10V. (7) Power dissipation is an additional 100mW, max, when V_{DD} is operated at +15V.

MECHANICAL



NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.185	1.215	30.10	30.86
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M		10°		10°
N	.025	.060	0.64	1.52

NOTE:
Metal Cap connected to -Vcc internally.

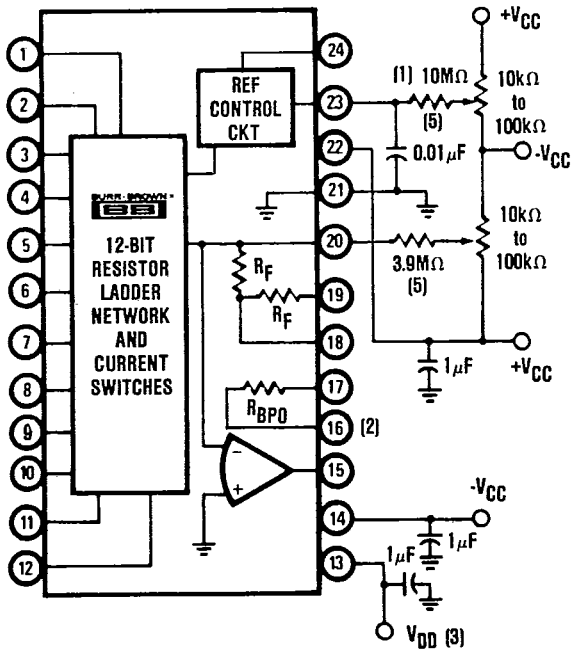
CASE: Ceramic
MATING CONNECTOR: 0245MC
WEIGHT: 8.4 grams (0.3oz.)

PIN ASSIGNMENTS

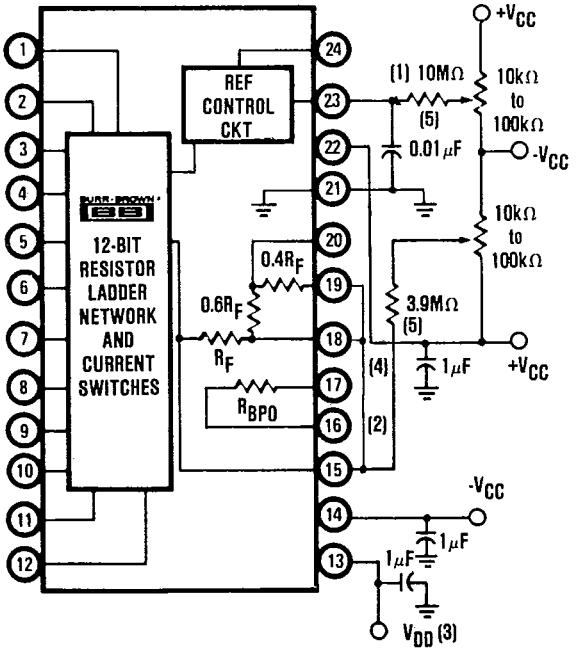
I Models	Pin	V Models
(MSB) Bit 1	1	Bit 1 (MSB)
Bit 2	2	Bit 2
Bit 3	3	Bit 3
Bit 4	4	Bit 4
Bit 5	5	Bit 5
Bit 6	6	Bit 6
Bit 7	7	Bit 7
Bit 8	8	Bit 8
Bit 9	9	Bit 9
Bit 10	10	Bit 10
Bit 11	11	Bit 11
(LSB) Bit 12	12	Bit 12 (LSB)
Logic Supply, V_{DD}	13	Logic Supply, V_{DD}
$-V_{CC}$	14	$-V_{CC}$
I_{OUT}	15	V_{OUT}
Reference Input	16	Reference Input
Bipolar Offset	17	Bipolar Offset
Scaling Network	18	10V Range
Scaling Network	19	20V Range
Scaling Network	20	Summing Junction
Common	21	Common
$+V_{CC}$	22	$+V_{CC}$
Gain Adjust	23	Gain Adjust
6.3V Reference Out	24	6.3V Reference Out

CONNECTION DIAGRAMS

Voltage Model



Current Model



NOTES:
1. DAC850/851 use a 10MΩ resistor. These models can replace the DAC85 which uses an 18MΩ resistor and the DAC87 which uses a 33MΩ resistor.
2. Pin 16 of DAC850/851 is used only to connect the bipolar offset resistor. An external reference voltage may not be used with DAC850/851.
3. If connected to $+V_{CC}$, which is permissible, power dissipation increases 75mW typ., 100mW max.
4. For fastest settling time connect pins 19, 18, and 15 together.
5. Values shown are for ±15V supplies. For supplies below ±13.5V use 2.7MΩ in place of 3.9MΩ and 7.5MΩ in place of 10MΩ.

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC850 and DAC851 accept complementary binary digital input codes. They may be connected by the user for any one of three complementary codes; CSB, CTC, or COB (see Table I).

ACCURACY

Linearity of a D/A converter is the true measure of its performance. The linearity error is specified over its entire temperature range. This means that the analog output will not vary by more than ±1/2LSB, maximum, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range.

TABLE I. Digital Input Codes.

DIGITAL INPUT MSB ↓ LSB ↓	ANALOG OUTPUT CSB Compl. Straight Binary	COB Compl. Offset Binary	CTC* Compl. Two's Compl.
000000000000	+Full Scale	+Full Scale	-LSB
011111111111	+1/2 Full Scale	Zero	-Full Scale
100000000000	Midscale -1LSB	-1LSB	+Full Scale
111111111111	Zero	-Full Scale	Zero

*Invert the MSB of the COB code with an external inverter to obtain CTC code.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next.

Monotonicity over the specification temperature range is guaranteed to insure that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain drift is established by: 1) testing the end point differences at -25°C, +25°C, and +85°C for the DAC850 and at -55°C, +25°C, and +125°C for the DAC851; 2) calculating the gain error with respect to the +25°C value and; 3) dividing by the temperature change. This is expressed in ppm/°C.

Offset drift is a measure of the actual change in output with all "1"s on the input over the specification temperature range. The offset is measured at -25°C, +25°C, and +85°C for the DAC850 and at -55°C, +25°C, and +125°C for the DAC851. The maximum change in offset is referenced to the offset at +25°C and is divided by the temperature change. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 1).

Voltage Output Models: Three settling times are specified to ±0.01% of full scale range (FSR): two for maximum full scale range changes of 20V and 10V, and one for a 1LSB change. The 1LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst-case settling time occurs.

Current Output Models: Two settling times are specified to ±0.01% of FSR. Each is given for current models connected with two different resistive loads: 10Ω to 100Ω and 1000Ω. Internal resistors are provided for connecting a nominal load resistance of approximately 1000Ω for output voltage ranges of ±1V and 0 to -2V.

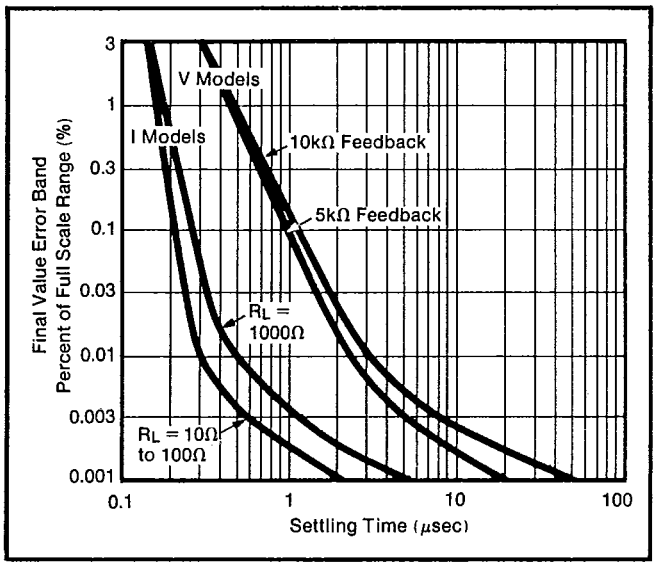


FIGURE 1. Full Scale Range Settling Time vs Final Value Error Band.

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy. The maximum compliance voltage of all current output models is +2.5V to -2.5V.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive, negative, or logic supplies about the nominal power supply voltages (see Figure 2).

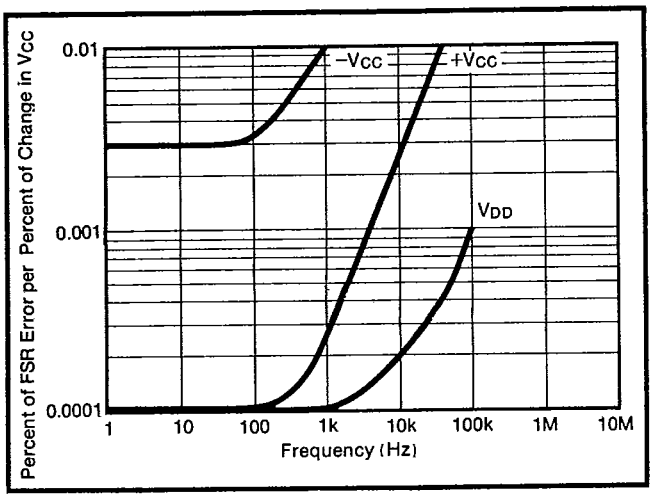


FIGURE 2. Power Supply Rejection vs Power Supply Ripple.

REFERENCE SUPPLY

All models are supplied with an internal 6.3V reference voltage supply. This voltage (pin 24) has a tolerance of ±1% and must be connected to the Reference Input (pin 16) for specified operation. This reference may be used externally also. The external current drain is limited to sourcing 2.5mA up to +85°C and 1mA up to +125°C not including current required by the bipolar offset circuit. An external buffer amplifier is recommended if this reference will be used to drive other system components because variations in a load driven from the reference will result in bipolar offset variations of the D/A converter. Gain and bipolar offset adjustments should be made under constant load conditions.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagrams. These capacitors (1μF tantalum or electrolytic recommended) should be located close to the case. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for best high frequency performance. The metal cap on the top of the package is connected internally to -Vcc.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external offset and gain potentiometers. Connect these potentiometers as shown in the Connection Diagrams and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 10MΩ resistors (20% carbon or better) should be located close to the case to prevent noise pickup. For operation with supplies of less than ±13.5V, use 2.7MΩ and 7.5MΩ resistors in place of the 3.9MΩ and 10MΩ resistors, respectively. If it is not convenient to use these high value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in each case. Figures 4 and 5 illustrate the relationship of offset and main adjustments to unipolar and bipolar D/A converter output.

Offset Adjustment: For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the offset potentiometer for zero output.

For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output voltage and adjust the Offset potentiometer for minus full scale voltage. Example: If the Full Scale Range is connected for 20V, the maximum negative output voltage is -10V. See Table II for corresponding codes and the Connection Diagrams for offset adjustment connections.

Gain Adjustment: For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the gain

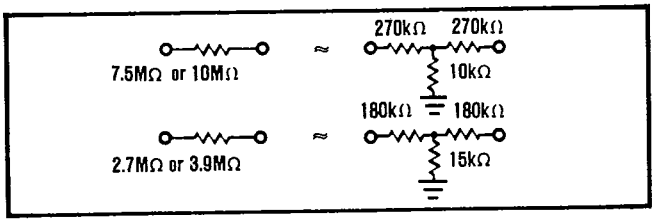


FIGURE 3. Equivalent Resistances.

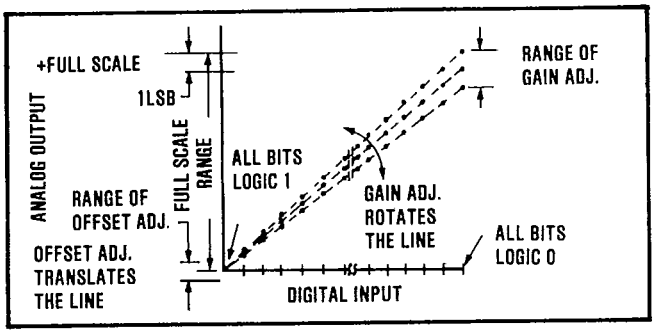


FIGURE 4. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

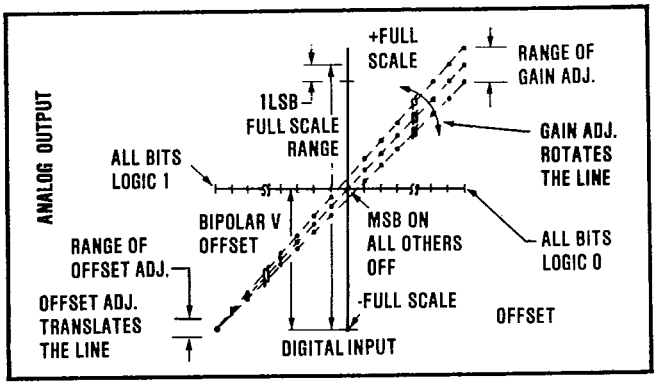


FIGURE 5. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

potentiometer for this positive full scale voltage. See Table II for positive full scale voltages and the Connection Diagrams for gain adjustment connections.

TABLE II. Digital Input/Analog Output.

DIGITAL INPUT MSB ↓ LSB ↓	ANALOG OUTPUT VOLTAGE* 0 to +10V	VOLTAGE* ±10V	CURRENT 0 to -2mA	CURRENT ±1mA
000000000000	+9.9976V	+9.9951V	-1.9995mA	-0.9995mA
011111111111	+5.0000V	0.0000V	-1.0000mA	0.0000mA
100000000000	+4.9976V	-0.0049V	-0.9995mA	+0.0005mA
111111111111	0.0000V	-10.0000V	0.0000mA	+1.000mA
One LSB	2.44mV	4.88mV	0.488μA	0.488μA

*To obtain values for other binary ranges:
0 to +5V range divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.

VOLTAGE OUTPUT MODELS

Output Range Connections

Internal scaling resistors provided in the DAC850 may be connected to produce bipolar output voltage ranges of ±10V, ±5V or ±2.5V or unipolar output voltage ranges of 0 to +5V or 0 to +10V. See Figure 6.

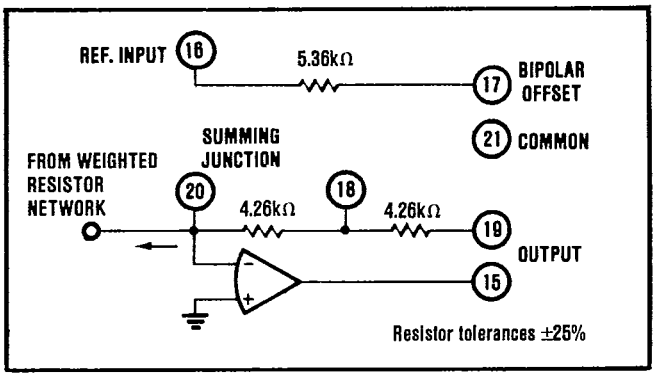


FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

Gain and offset drift are minimized because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table III. Settling time for a full scale range change is specified as 3μsec for the 20 volt range and 2.5μsec for the 10 volt range.

TABLE III. Output Voltage Range Connections - Voltage Model.

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10	COB or CTC	19	20	15	24
±5	COB or CTC	18	20	NC	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	NC	24
0 to +5V	CSB	18	21	20	24

CURRENT OUTPUT MODELS

The resistive scaling network and equivalent output circuit of the current model differ from the voltage model and are shown in Figures 7 and 8. It is important to note that there is a relationship between the tolerances of the current source and the scaling resistors. The magnitude of the tolerance tracks very closely but with opposite sign. The tolerance of the internal resistance of the converter (7.2kΩ unipolar, 3.07kΩ bipolar) tracks the tolerance of the scaling resistors in sign and approximately proportionately in magnitude. That is, if the scaling resistors are high by 10%, the internal impedance is high by about 8%.

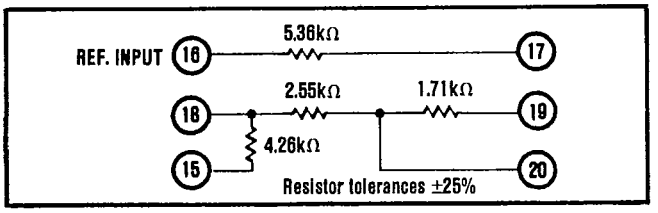


FIGURE 7. Internal Scaling Resistors.

Internal scaling resistors (Figure 7) are provided to scale an external op amp or to configure load resistors for a low drift direct voltage output. These connections are described in the following sections.

If the internal resistors are not used for voltage scaling, external R_L (or R_F) resistors should have a TCR of ±25ppm/°C or less to minimize drift. This will typically add ±50ppm/°C plus the TCR of R_L (or R_F) to the total drift.

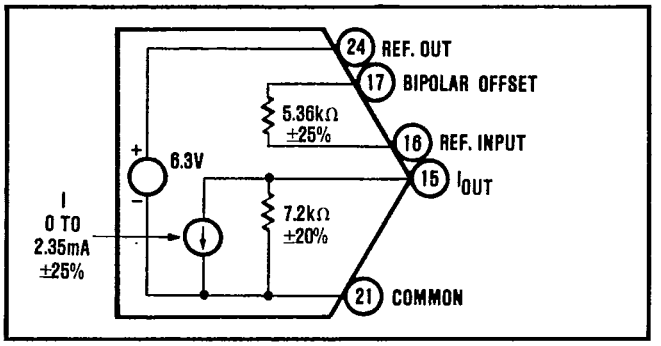


FIGURE 8. Current Output Model Equivalent Output Current.

Driving a Resistive Load Unipolar

A load resistance, $R_L = R_{LI} + R_{LS}$, connected as shown in Figure 9 will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2.35mA \left(\frac{R_L \times 7.2k\Omega}{R_L + 7.2k\Omega} \right)$$

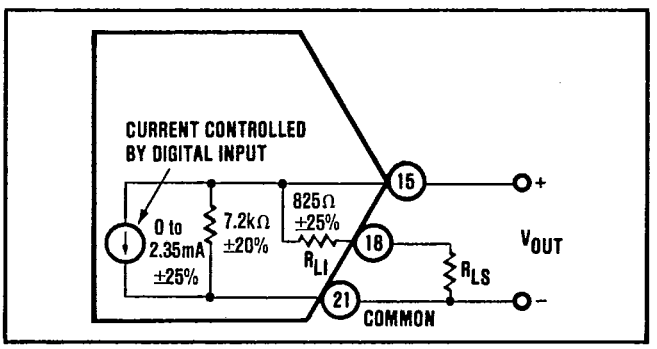


FIGURE 9. Current Output Model Equivalent Circuit Connected for Unipolar Voltage Output with Resistive Load.

To achieve specified drift, connect the internal scaling resistor (R_{LI}) as shown to an external metal film trim resistor (R_{LS}) to provide full scale output voltage range of 0 to -2V. Tolerances on internal equivalent resistors are wide. R_{LS} will have to be selected for each unit.

Driving a Resistive Load Bipolar

The equivalent output circuit for a bipolar output voltage range is shown in Figure 10, $R_L = R_{LI} + R_{LS}$. V_{OUT} is determined by:

$$V_{OUT} = \pm 1.175mA\left(\frac{R_L \times 3.17k\Omega}{R_L + 3.17k\Omega}\right)$$

To achieve specified drift, connect the 1.71kΩ and 2.55kΩ internal scaling resistors in parallel (R_{LI}) and add an external metal film resistor (R_{LS}) in series to obtain a full scale output range of ±1V. The tolerances on the equivalent internal resistors are wide. R_{LS} will have to be selected for each unit.

Driving An External Op Amp

The current output model will drive the summing junction of an op amp used as a current-to-voltage converter to produce an output voltage (see Figure 11).

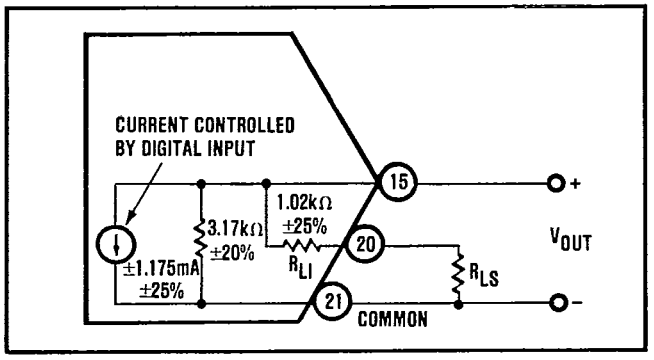


FIGURE 10. Current Output Model Connected for Bipolar Output Voltage with Resistive Load.

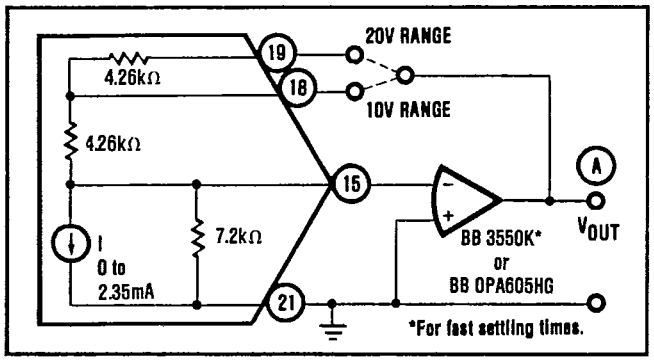


FIGURE 11. External Op Amp - Using Internal Feedback Resistors.

$$V_{OUT} = I_{OUT} \times R_F$$

where I_{OUT} is the output current and R_F is the feedback resistor. Using the internal feedback resistors of the current output model provides output voltage ranges the same as the voltage model. To obtain the desired output voltage range when connecting an external op amp, refer to Table IV.

TABLE IV. Voltage Range of Current Output D/A Converter.

Output Range	Digital Input Codes	Connect Ⓐ to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	15	Ⓐ	24
±5V	COB or CTC	18	15	NC	24
±2.5V	COB or CTC	18	15	15	24
0 to +10V	CSB	18	21	NC	24
0 to +5V	CSB	18	21	15	24

Output Larger Than 20V Range

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1.175mA for bipolar voltage ranges and -2.35mA for unipolar voltage ranges (see Figure 12). Use protection diodes when a high voltage op amp is used.

The feedback resistor, R_F, should have a temperature coefficient as low as possible. Using an external feedback resistor, overall drift of the circuit increases due to the lack of temperature tracking between R_F and the internal scaling resistor network. This will typically add 50ppm/°C + R_F drift to total drift.

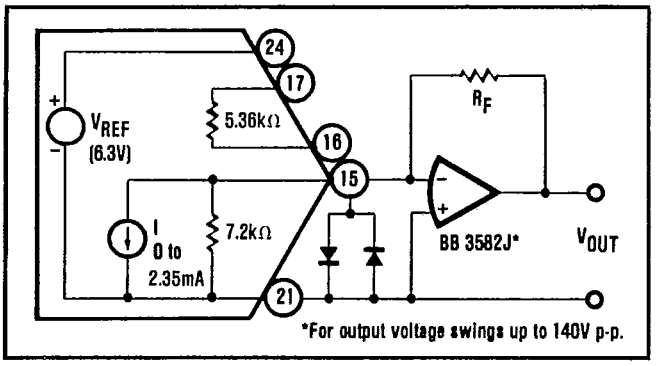


FIGURE 12. External Op Amp - Using External Feedback Resistors.

LOGIC INPUT COMPATIBILITY

DAC850 and DAC851 digital inputs are TTL, LSTTL, 54/74HC CMOS compatible as shown in the specification table when V_{DD} is operated over 4.5 to 16.5 volts.

Figure 13 illustrates using CMOS hex buffers with DAC850 to provide CMOS input compatibility. This combination will operate together over a wide range of logic power supply voltages.

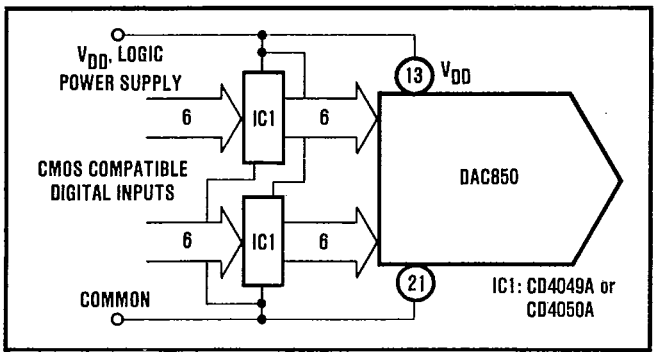


FIGURE 13. Using DAC850, 851 with CMOS Hex Buffers Over a Wide Range of Logic Power Supply Voltages.