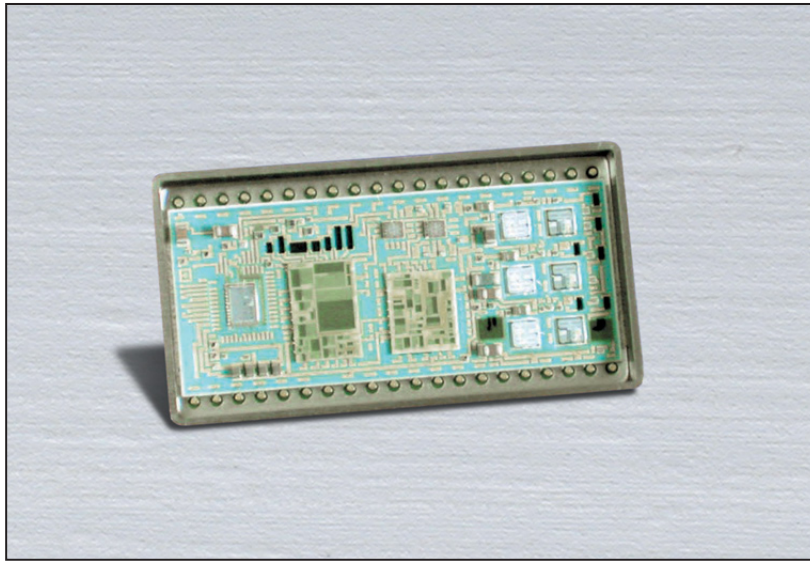


# DSC-10510

## 7 VA DIGITAL-TO-SYNCHRO (D/S) CONVERTER

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### FEATURES

- 7 VA Drive Capability for CT, CDX, or TR Loads
- Double Buffered Transparent Input Latch
- 16-Bit Resolution
- Up to 2 Minute Accuracy
- Power Amplifier Uses Pulsating or DC Supplies
- Built-In-Test (BIT) Output

### DESCRIPTION

The DSC-10510 is a high power Digital-to-Synchro converter, with 16-bit resolution and up to  $\pm 2$  minute accuracy. The DSC-10510 is capable of driving multiple Control Transformer (CT), Control Differential Transmitter (CDX) and Torque Receiver (TR) loads up to 7 VA.

The DSC-10510 contains a high accuracy D/R converter, a triple power amplifier stage, a walk-around circuit (to prevent torque receiver hangups), and thermal and over-current protection circuits. The hybrid is protected against overloads, load transients, over-temperature, loss of reference, and power amplifier or DC power supply shutdown.

Microprocessor compatibility is provided through a 16-bit/2-byte double-buffered input latch. Data input is natural binary angle in TTL compatible parallel positive logic format.

Packaged in a 40-pin TDIP, the DSC-10510 features a power stage that may be driven by either a standard  $\pm 15$  VDC supply or by a pulsating reference supply when used with an optional power transformer. When powered by the reference source, heat dissipation is reduced by 50%.

### APPLICATIONS

The DSC-10510 can be used where digitized shaft angle data must be converted to an analog format for driving CT's, CDX's, and TR loads. With its double buffered input latches, the DSC-10510 easily interfaces with microprocessor based systems such as flight simulators, flight instrumentation, fire control systems, and flight data computers.



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### FOR MORE INFORMATION CONTACT:

Technical Support:  
1-800-DDC-5757 ext. 7771

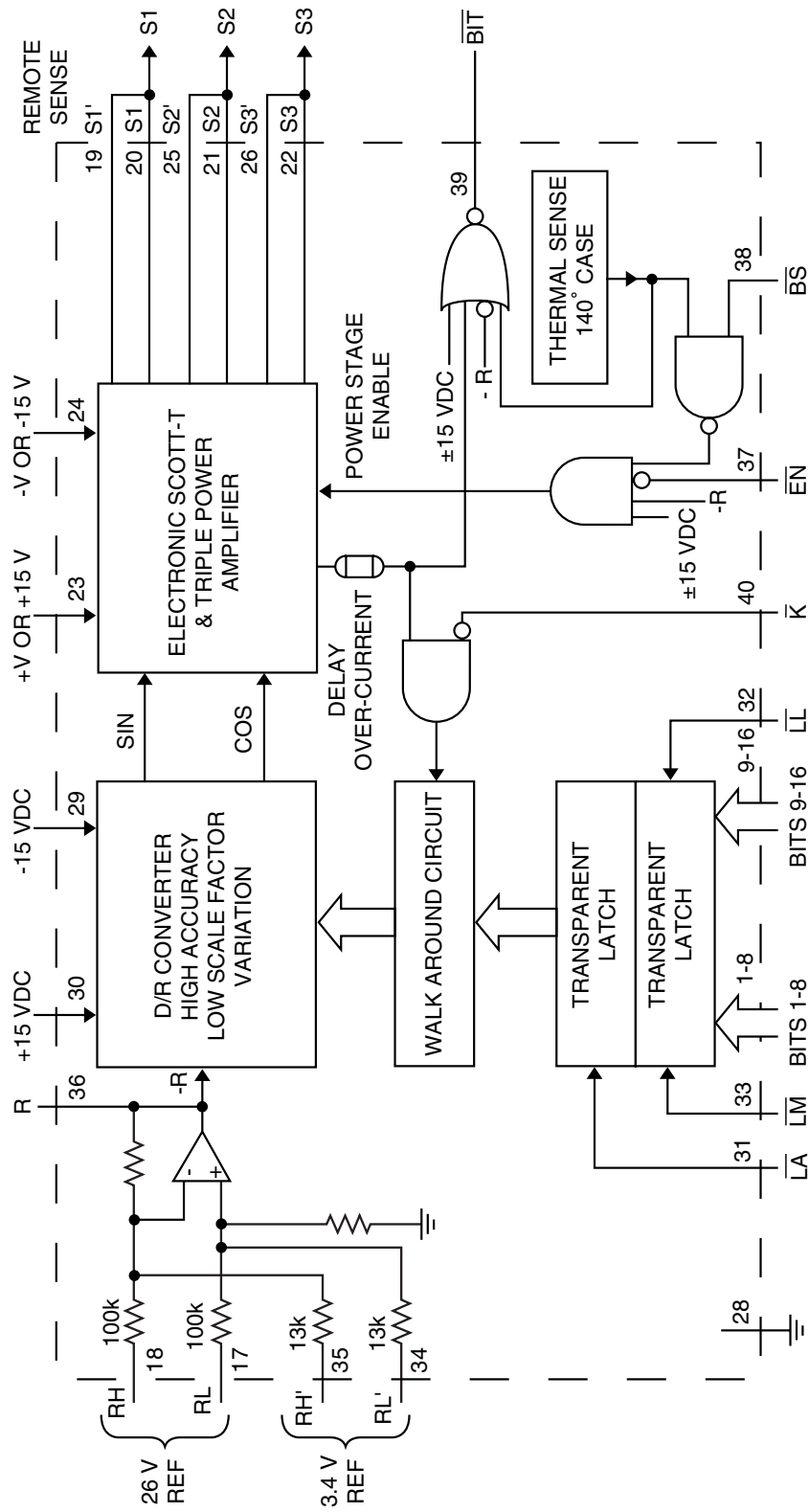


FIGURE 1. DSC-10510 BLOCK DIAGRAM

**TABLE 1. DSC-10510 SPECIFICATIONS**

PARAMETER	VALUE	DESCRIPTION
<b>RESOLUTION</b>	16 bits	Bit 1 = MSB, Bit 16 = LSB
<b>ACCURACY</b>	±2 or 4 minutes	(Note 1)
<b>DIFFERENTIAL LINEARITY</b>	1 LSB max in the 16th bit	
<b>OUTPUT SETTLING TIME</b>	40 µs max	For any digital input step change (passive loads)
<b>DIGITAL INPUT/OUTPUT</b> Logic Type Digital Inputs  Loading $\overline{K}$ $\overline{EN}$  Digital Outputs $\overline{BIT}$  Drive Capability	Logic 0 = 0.8 V max Logic 1 = 2.0 V min 20 µA max//5pf max 65 µA typ//100 µA max//5pf max Logic 0 or 1  Logic 0 or 1  Logic 0 = 1 TTL Load Logic 1 = 10 TTL Loads	TTL/CMOS compatible All inputs except K (Kick pin 40) Bits 1 - 16, $\overline{BS}$ , and $\overline{EN}$ LL, LM, and LA (CMOS transient protected) Logic 0 enables Kick circuit, open (Logic 1) to disable; pulls self up to +15V. Logic 0 enables power amplifier. Logic 1 will disable "shutoff" of the power amplifier.  Logic 0 for $\overline{BIT}$ condition (see $\overline{BIT}$ pin function)  1.6mA at 0.4V max 0.4mA at 2.8V min
<b>REFERENCE INPUT</b> Type  Max Voltage w/o Damage  Frequency Input Impedance Single Ended  Differential	26 Vrms differential 3.4 Vrms differential  72.8 Vrms for RH - RL 9.52 Vrms for RH' - RL' DC to 1 kHz  100k Ohms ±0.5% 13k Ohms ±0.5% 200k Ohms ±0.5% 26k Ohms ±0.5%	RH - RL RH' - RL'    RH - RL RH' - RL' RH - RL RH' - RL'
<b>SYNCHRO OUTPUT</b> Voltage L-L Scale Factor Variation  Current CT, CDX or TR Load DC Offset  Protection	11.8 Vrms ±0.5% for nom Ref V ±0.1% max  700 mA rms max 7 VA max ±15 mV max	Simultaneous amplitude variation on all output lines as a function of digital angle.  Each line to ground. Varies with angle.  Output protected from overcurrent, voltage feedback transient, and over temperature, loss of reference, loss of power amplifier, and loss of ±DC supply voltage.
<b>POWER SUPPLY CHARACTERISTICS</b> Nominal Voltage Voltage Range  Max Voltage w/o Damage Current	±15 V ±5%  18V 25 mA max	±V 20 V peak max, 3 V above output min 25 V load dependent
<b>TEMPERATURE RANGES</b> Operating (Case) -3XX -1XX Storage	0°C to +70°C -55°C to +125°C -65°C to +150°C	
<b>PHYSICAL CHARACTERISTICS</b> Size  Weight	2.0 x 1.1 x 0.2 inches (50.8 x 27.9 x 5.1 mm) 0.9 oz (25.5 g)	40 Pin Triple DIP

Note 1: DSC-10510-303 accuracy = ±4 minutes (No Load) + 1.6 minutes at full load (7 VA Inductive)  
DSC-10510-304 accuracy = ±2 minutes (No Load) + 1.6 minutes at full load (7 VA Inductive)

# INTRODUCTION

## SYSTEM CONSIDERATIONS:

### POWER SURGE AT TURN ON

The output power stages can fully turn on before all the supplies stabilize, when power is initially applied. Multiple D/S converters with substantial loads can cause the system power supply to have difficulty coming up and may even cause the supply to shut down. It is important that the power supply can handle the turn-on surge or that the D/S turn-ons be staggered. Typically, the surge will be twice the max rated draw of the converter.

### POWER SUPPLY CYCLING

Power supply cycling of the DSC-10510 should follow the guidelines below to avoid any potential problems.

Strictly maintain proper sequencing of supplies and signals per typical CMOS circuit guidelines:

- Apply power supplies first (+15, -15V and ground).
- Apply digital control signals next.
- Apply analog signals last.

The reverse sequence should be followed during power down of the circuit.

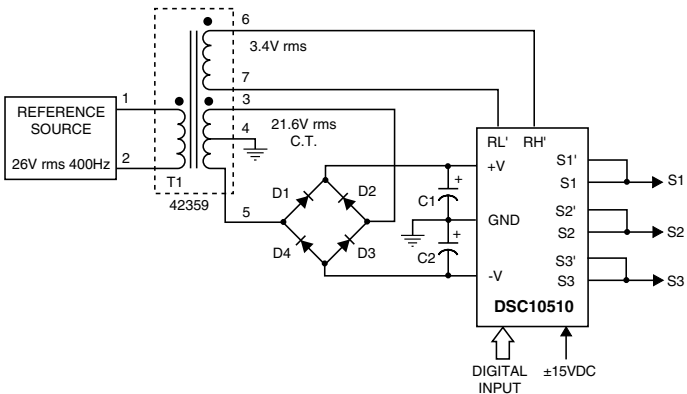
It is also recommended that the KICK pin, if unused, be left in the "No Connection" (N/C) state. The internal pull up will disable the pin (this removes any unnecessary voltages from the converter).

### TORQUE LOAD MANAGEMENT

The above problems are compounded by the high power levels involved when multiple torque loads (TR) are being driven. In this configuration, power supply fold back problems are common unless the stagger technique is used. The load will also need time to stabilize. On turn-on it is likely that some of output loads will be at a different angle than the D/S output. As the angular difference increases so does the power draw until the difference is 180 degrees. At this point the load impedance drops to  $Z_{ss}$  and current draw is at a maximum.

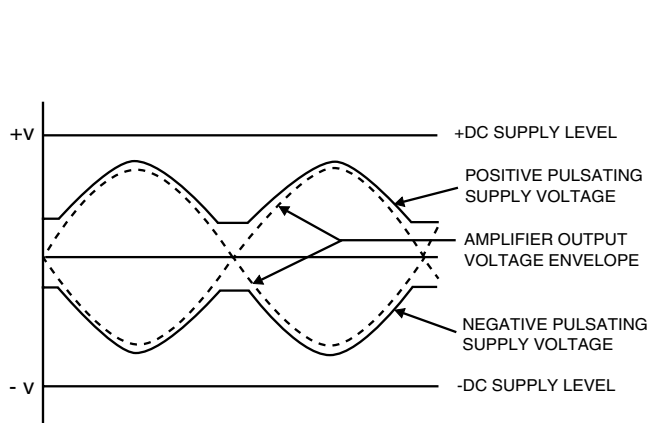
### PULSATING POWER SUPPLIES

D/S and D/R converters have been designed to operate their output power stages with pulsating power to reduce power dissipation and power demand from regulated supplies. Figures 2 and 3 illustrate this technique. The power output stage is only supplied with enough instantaneous voltage to be able to drive the required instantaneous signal level. The AC reference can be full wave rectified and applied to the push-pull output drivers since the output signal is required to be in phase with the AC reference. The supply voltage will be just a few volts more than the output signal and internal power dissipation is minimized.

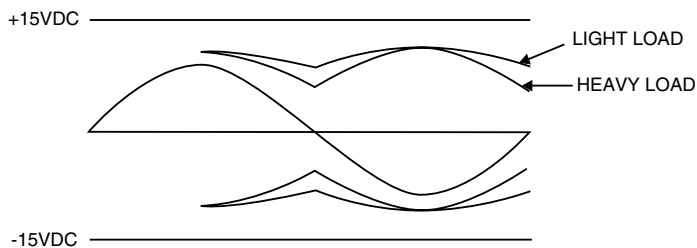


NOTES:  
PARTS LIST FOR 400Hz  
D1, D2, D3, D4 = 1N4245  
C1 AND C2 = 47µF, 35V DC CAPACITOR

**FIGURE 2. TYPICAL CONNECTION DIAGRAM UTILIZING PULSATING POWER SOURCE**



**FIGURE 3. PULSATING POWER SUPPLY VOLTAGE WAVEFORMS**



**FIGURE 4. LOADED WAVEFORMS**

**THERMAL CONSIDERATIONS**

Power dissipation in D/S and D/R circuits is dependent on the load, whether active (TR) or passive (CT or CDX), and the power supply, whether DC or pulsating. With inductive loads virtually all the power consumed will have to be dissipated in the output amplifiers. This can require considerable care in heat sinking.

*Example:*

For illustrative purposes the following thermal calculations are made using the DSC-10510's specifications. The DSC-10510 has a 7 VA drive capability for CT, CDX, or TR loads.

Simplest case first: **Passive Inductive Load and ±15 Volt DC power stage supplies (as shown in Figure 2).** The power dissipated in the power stage can be calculated by taking the integral of the instantaneous current multiplied by the voltage difference from the DC supply that supplies the current and instantaneous output voltage over one cycle of the reference. For an inductive load this is a rather tedious calculation. Instead take the difference between the power input from the DC supplies minus the power delivered to the load. An actual synchro load is highly inductive with a Q of 4-6; therefore assume that it is purely reactive. The power out, then, is 0 Watts. As a worst case scenario, also assume the load is the full 7 VA, the converter's rated load.

The VA delivered to the load is independent of the angle but the voltage across the synchro varies with the angle from a high of 11.8 Volts line-to-line (L-L) to a low of 10.2 V L-L (Note 1). The maximum current therefore is  $7VA/10.2 V = 0.68 A$  rms. The

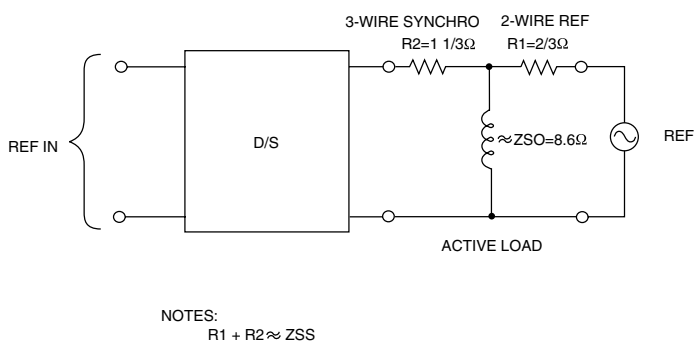
output is L-L push-pull, that is, all the current flows from the positive supply out to the load and back to the negative supply. The power input is the DC voltage times the average current or  $30 V \times (0.68 A \times 0.635/0.707) [avg/rms] = 18.32$  Watts.

**Note 1:** The DSC-10510 has an 11.8 VL-L synchro output. In this case, we use  $11.8V \times \sin 120^\circ = 11.8V \times .866 = 10.2$  VL-L. To calculate the load use  $Z_{so}$ .  $Z_{so}$  is the impedance between one of the three stator wires and the other two shorted together with the rotor open circuit. VL-L x .866 is the voltage that would result from this configuration.

The power dissipated by the output driver stage is over 18 Watts shared by the six power transistors. Since one synchro line supplies all the current while the other two share it equally, one will dissipate 2/3 of the power and the other two will each dissipate 1/3. There are 2 transistors per power stage so each of the two transistors dissipates 1/3 of the power and the other transistors dissipate 1/6 of the power. This results in a maximum power in any one transistor of  $1/3 \times 18.32 W = 6.04$  Watts. The heat rise from the junction to the outside of the package, assuming a thermal impedance of  $4^\circ C$  per watt =  $24.16^\circ C$ . At an operating case temperature of  $125^\circ C$  the maximum junction temperature will be  $149.16^\circ C$ .

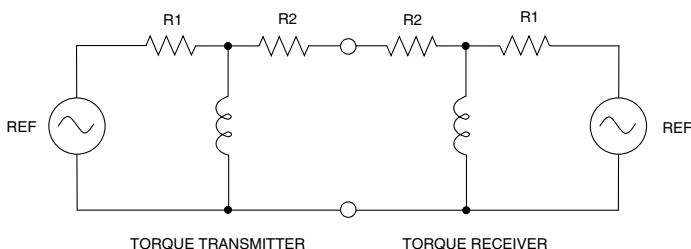
The other extreme condition to consider is when the output voltage is 11.8 V. The current then will be 0.42 Amps and the power will be  $30 \times (0.42A \times 0.635/0.707) = 11.32$  Watts. A similar calculation will show the maximum power per transistor to be 2.3 Watts. This is much less than when the output voltage is 10.2 V.

For **Pulsating Supplies** the analysis is much more difficult. Calculations for a purely reactive load with DC supplies equal to the output voltage peak vs. pulsating supplies with a supply voltage equal to the output voltage yield **an exact halving of the power dissipated**. At light loads the pulsating supplies approximate DC supplies and at heavy loads, which is the worst case, they approximate a pulsating supply as shown in Figure 4. Advantages of the pulsating supply technique are:

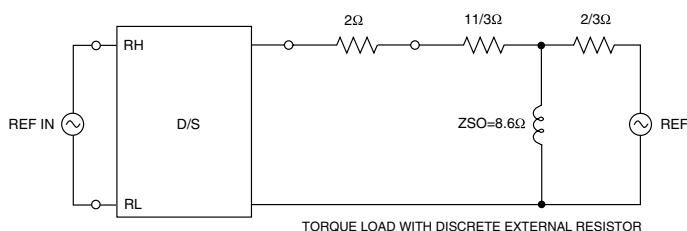


NOTES:  
R1 + R2 ≈ ZSS

**FIGURE 5. EQUIVALENT 2-WIRE CIRCUIT**



**FIGURE 6. TORQUE SYSTEM**



**FIGURE 7. D/S EQUIVALENT**

- Reduced load on the regulated  $\pm 15$  VDC supplies
- Halving of the total power
- Simplified power dissipation management

**ACTIVE LOAD**

Active loads (torque receivers) make it more difficult to calculate power dissipation. The load is composed of an active part and a passive part. Figure 5 illustrates the equivalent two wire circuit. At null, when the torque receiver’s shaft rotates to the angle that minimizes the current in R2, the power dissipated is at its lowest. The typical ratio of  $Z_{so}/Z_{ss} = 4.3$ . For the maximum specified load of  $Z_{ss} = 2$  ohm, the  $Z_{so} = 2 \times 4.3 = 8.6$  ohms. Also, the typical ratio of  $R2/R1 = 2$ .

In synchro systems with a torque transmitter driving a torque receiver, the actual line impedances are as shown in Figure 6. The torque transmitter and torque receiver are electrically identical, so that the total line impedance is double that of Figure 5. The torque system is designed to operate this way. The higher the total line impedances, the lower the current flow at null and the lower the power dissipation. It is recommended that with

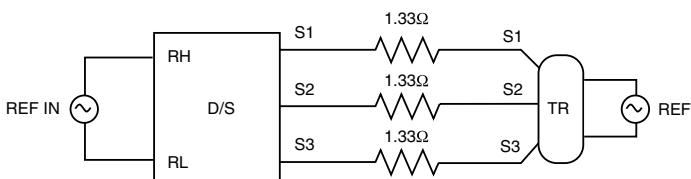
torque loads, discrete resistors be used as shown in Figures 7 and 8.

A torque load is normally at null. Once the torque receiver nulls at power turn on, the digital commands to the D/S are typically in smaller angular steps, so the torque system is always at or near null. Large digital steps, load disturbances, a stuck torque receiver or one synchro line open, however, cause an off null condition.

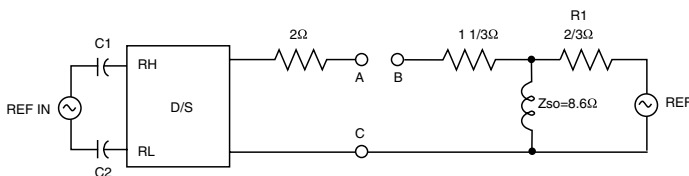
At null the load current could be zero (See Figure 9 ). If  $V_{ac} = V_{ab}$ , both in magnitude and phase, then, when “a” is connected to “b,” no current will flow. Pick C1 and C2 to match the phase lead of R1 – Zso. In practice this ideal situation is not realized. The input to output transformation ratio of torque receivers is specified at 2% and the turns ratio at 0.4%. The in-phase current flow due to this nominal output voltage (10.2 V) multiplied by the % error (2.4/100) divided by total resistance (4 Ohms) = 61mA. A phase lead mismatch between the torque receiver and the converter of 1 degree results in a quadrature current of  $10.2 \text{ V} \times \sin 1^\circ / 4 \text{ Ohms} = 44.5 \text{ mA}$ . Total current is the phaser sum  $61 + 44.5 = 75.5 \text{ mA}$ . Power dissipation is  $30 \text{ VDC} \times 75.5 \text{ mA rms} \times 0.9$  (avg/rms) = 2.04 Watts. Since this is a light load condition, even pulsating supplies would be approximating DC supplies.

The **off null** condition power dissipation is quite different. Actual synchros have no current limiting, so the circuit current is the current that the circuit conditions demand. The worst case would be for a 180 degree error between the two synchros as shown in Figure 10. For this condition the two equivalent voltage sources are 10.2 V opposing. The current is  $(10.2 \times 2) / 4 = 5.1 \text{ A}$  in phase.

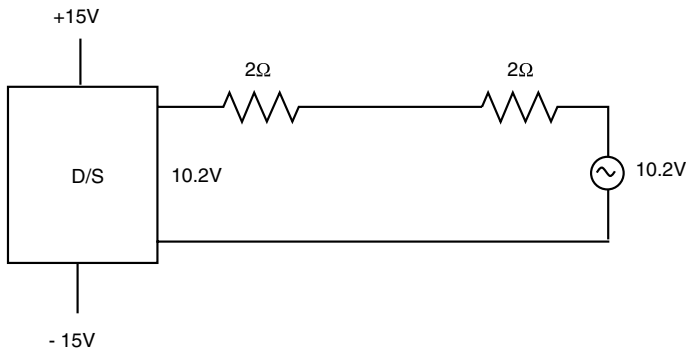
The power dissipated in the converter is the power supplied by the  $\pm 15$  VDC supplies minus the power delivered to the load  $(30 \text{ V} \times 5.1 \text{ A} \times 0.9) - (10.2 \text{ V} \times 5.1 \text{ A}) = 87.7 \text{ Watts}$  for DC supplies. This requires a large power supply and high wattage resistors.



**FIGURE 8. D/S - ACTUAL HOOK-UP**



**FIGURE 9. IDEAL NULL CONDITION**



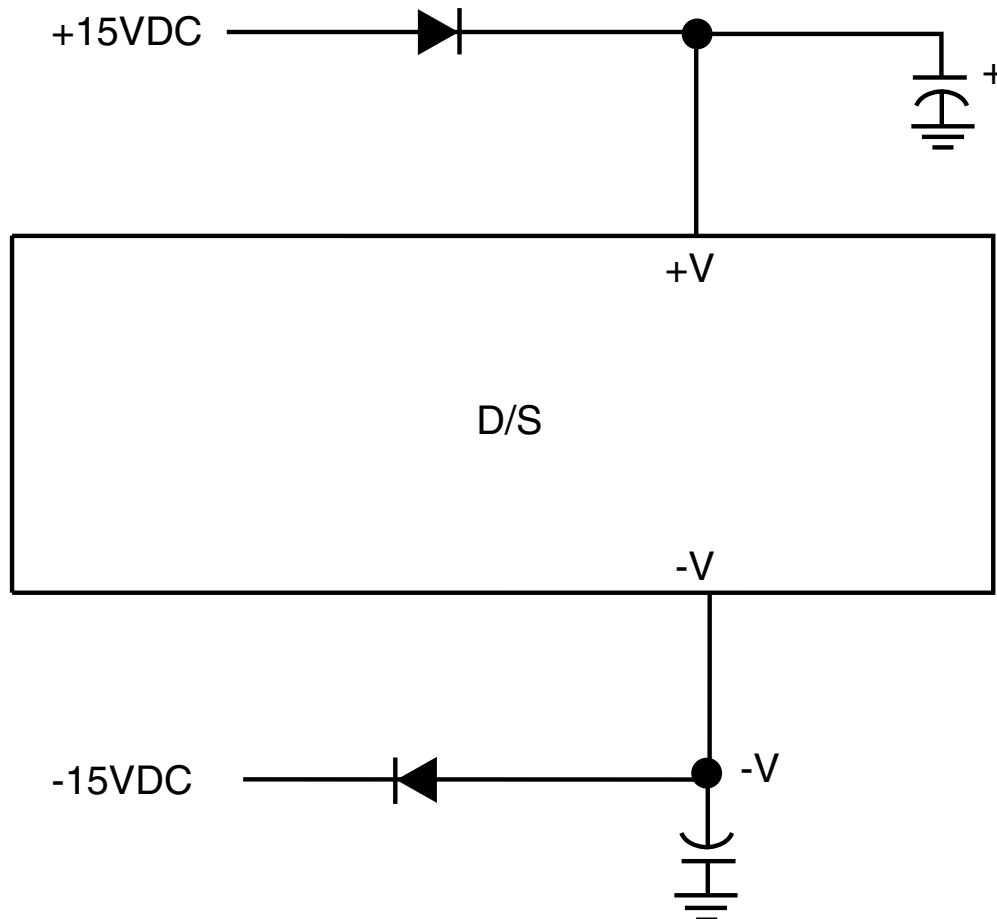
**FIGURE 10. WORST CASE 180° ERROR**

The converter output current is typically limited (in the DSC-10510 case to 0.8 A peak). This limits the power supply to more reasonable values but introduces another problem – the torque receiver can hang up in a continuous current limited condition at a false stable null. The DSC-10510 has special circuits that sense this continuous current overload condition and sends a momentary 45° “kick” to the torque receiver thus knocking it off the false null. The torque receiver will then swing to the correct angle and properly null. If the torque receiver is stuck it will not be able to swing off the over-current condition. In this case the converter will send a  $\overline{\text{BIT}}$  signal when the case temperature

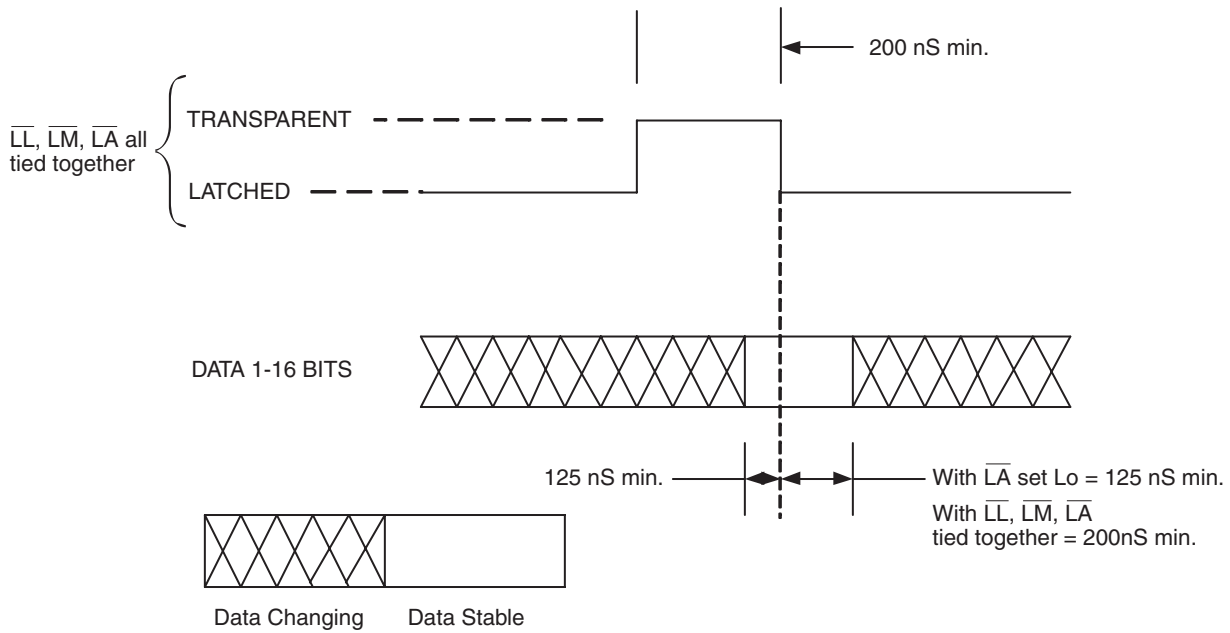
exceeds 140°C. This  $\overline{\text{BIT}}$  signal can be used to shut down the output power stage.

An additional advantage of using pulsating power supplies is that the loss of reference when driving torque loads is fail safe. The load will pump up the  $\pm V$  voltage through the power stage clamp diodes and the loss of the reference detector will disable the power stage. The power stage will be turned off with the required power supply voltages. The pulsating power supply diodes will isolate the pumped up pulsating supplies from the reference. If the DC power supplies are to be used for the power stage, and there is a possibility of the DC supplies being off while the reference to the torque receiver is on, then the protection circuitry shown in Figure 11 is highly recommended.

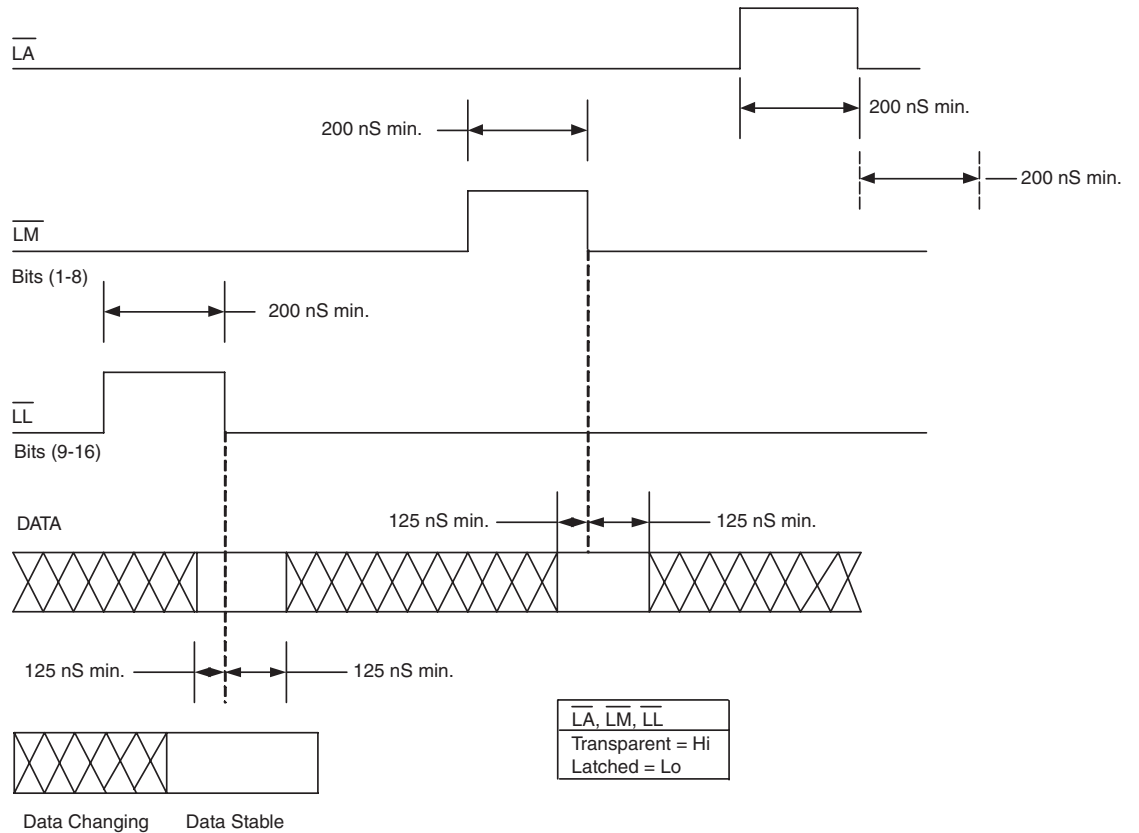
A remote sense feature is incorporated in DDC’s DSC-10510 hybrid digital-to-synchro converter. Rated at 7 VA, it offers accuracies to  $\pm 2$  minutes of arc at the load. This remote sense feature operates just as other precision sources do. A separate line is run to each leg of the synchro (in addition to the drive line) to sense the voltage actually appearing on the load. This is then used to regulate the output based on load voltage rather than converter output voltage. This feature is very useful in driving heavy passive loads in precision systems.



**FIGURE 11. PROTECTION CIRCUITRY**



**FIGURE 12A.  $\overline{LL}, \overline{LM}, \overline{LA}$  TIMING DIAGRAM (16 BIT)**

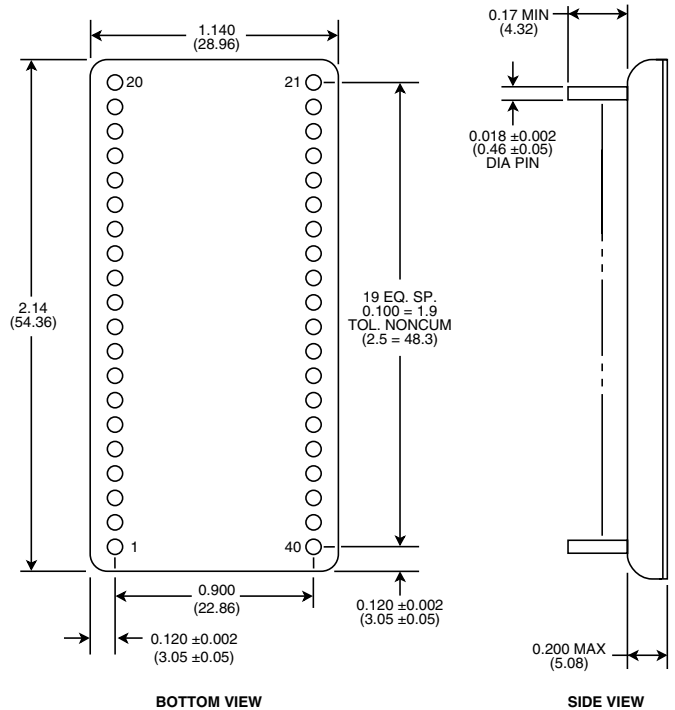


**FIGURE 12B .  $\overline{LL}, \overline{LM}, \overline{LA}$  TIMING DIAGRAM (8 BIT)**



**TABLE 2. DSC-10510 PIN FUNCTIONS**

PIN	NAME	FUNCTION
1	DO1	Digital Input 01 (MSB) Logic "1" enables.
2	DO2	Digital Input 02
3	DO3	Digital Input 03
4	DO4	Digital Input 04
5	DO5	Digital Input 05
6	DO6	Digital Input 06
7	DO7	Digital Input 07
8	DO8	Digital Input 08
9	DO9	Digital Input 09
10	DO10	Digital Input 10
11	DO11	Digital Input 11
12	DO12	Digital Input 12
13	DO13	Digital Input 13
14	DO14	Digital Input 14
15	DO15	Digital Input 15
16	DO16	Digital Input 16 (LSB)
17	RL	26 Vrms Reference Low Input
18	RH	26 Vrms Reference High Input
19	S1'	Synchro S1 Remote Sense Output
20	S1	Synchro S1 Output
21	S2	Synchro S2 Output
22	S3	Synchro S3 Output
23	+V	Power Stage +V
24	-V	Power Stage -V
25	S2'	Synchro S2 Remote Sense Output
26	S3'	Synchro S3 Remote Sense Output
27	NC	No Connection
28	GND	Ground
29	-15 V	Power Supply
30	+ 15V	Power Supply
31	$\overline{L}A$	2nd Latch All Enable. Input enables dual latch.
32	$\overline{L}L$	1st Latch LSBs Enable. Enables bits 9 - 16
33	$\overline{L}M$	1st Latch MSBs Enable. Enables bits 1 - 8
34	RL'	3.4 Vrms Reference Low Input
35	RH'	3.4 Vrms Reference High Input
36	-R (TP)	No connection. Factory test point.
37	$\overline{E}N$	Power stage enable input allows for digital shutdown of power stage when this pin is set to Logic 1.
38	$\overline{B}S$	Battle Short Input. Logic 0 overrides over temperature protection.
39	$\overline{B}IT$	Built-In-Test Output. Logic 0 when loss of reference, loss of $\pm 15$ VDC supply, case temperature of $+140^{\circ}C$ , or an output over-current has been detected. Loss of reference, loss of $\pm 15$ VDC supply or case temperature of $+140^{\circ}C$ will disable the power output
40	$\overline{K}$	Kick. Input used for reducing excessive current flow in torque receiver loads at false null.

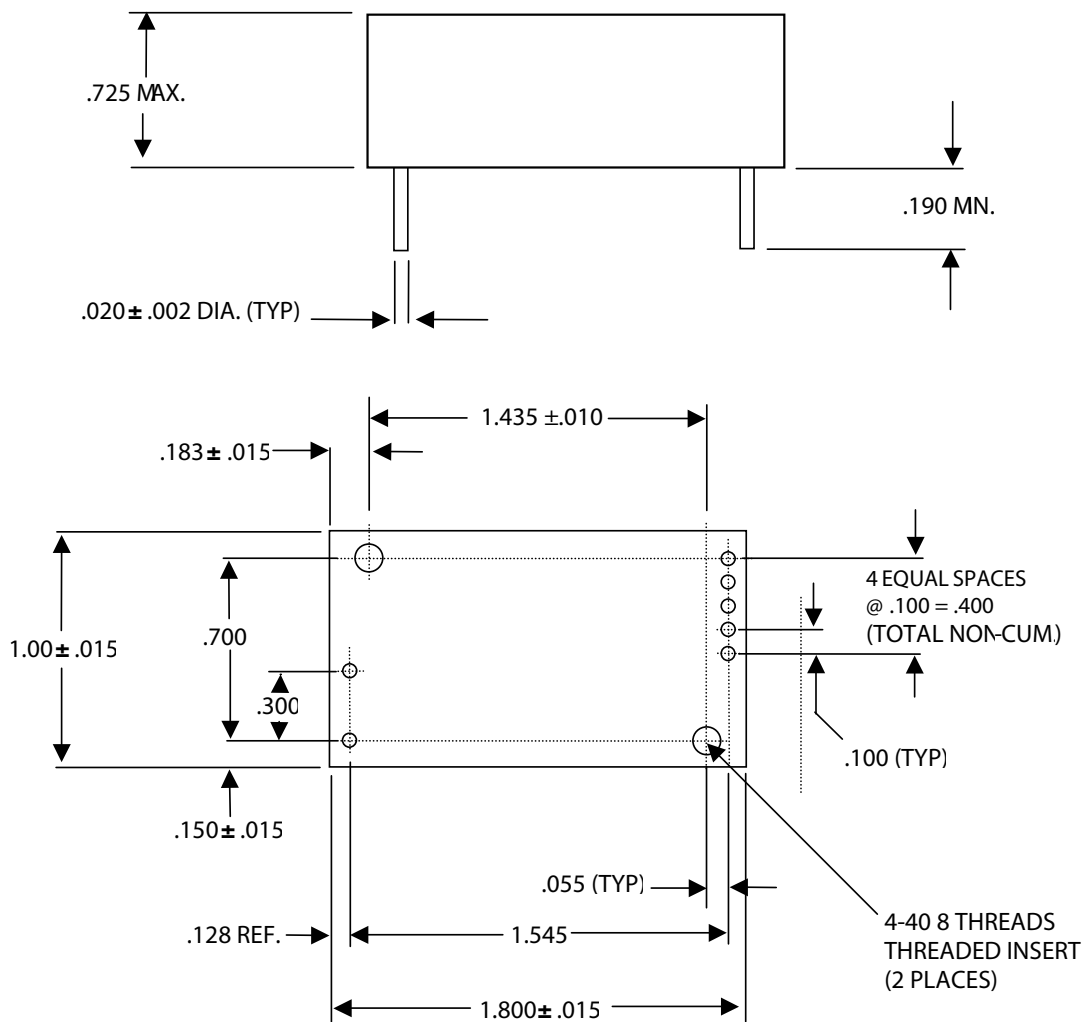


- Notes:**
1. Dimensions are in inches (millimeters).
  2. Lead identification numbers for reference only.
  3. Lead cluster shall be centered within  $\pm 0.10$  of outline dimensions. Lead spacing dimensions apply only at seating plane.
  4. Pin material meets solderability requirements of MIL-PRF-38534

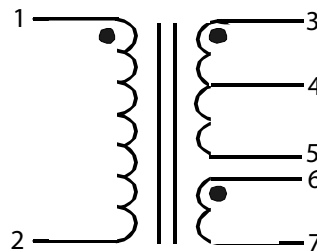
**FIGURE 13. DSC-10510 MECHANICAL OUTLINE 40-PIN TDIP**

**TABLE 3. ANGLES IN DEGREES CROSS REFERENCED TO A 16-BIT DIGITAL WORD**

DEGREES (HEX)	16 BIT DIGITAL WORD ( $\Phi$ ) (1 = MSB, 16 = LSB)															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0° (0000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15° (0AAB)	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	1
30° (1555)	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1
45° (2000)	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
60° (2AAB)	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1
75° (3666)	0	0	1	1	0	1	0	1	0	1	0	1	0	1	0	1
90° (4000)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
120° (5555)	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
135° (6000)	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
180° (8000)	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
240° (AAAB)	1	0	1	0	1	0	1	0	0	0	1	0	1	0	1	1
270° (C000)	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
285° (CAAB)	1	1	0	0	1	0	1	0	1	0	0	0	1	0	1	1
300° (D555)	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
315° (E000)	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
330° (EAAB)	1	1	1	0	1	0	1	0	1	0	1	0	1	0	1	1
345° (F555)	1	1	1	1	0	1	0	1	0	1	0	1	0	1	0	1
359° (FFFF)	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

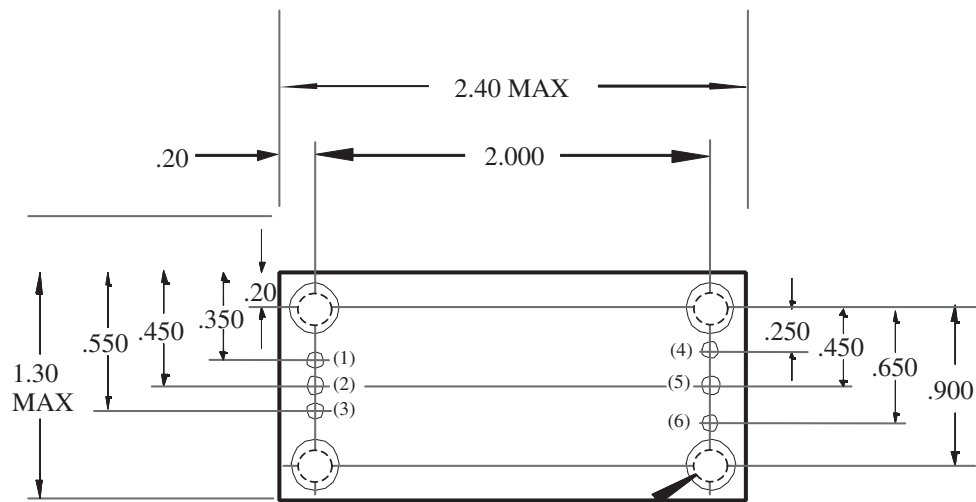


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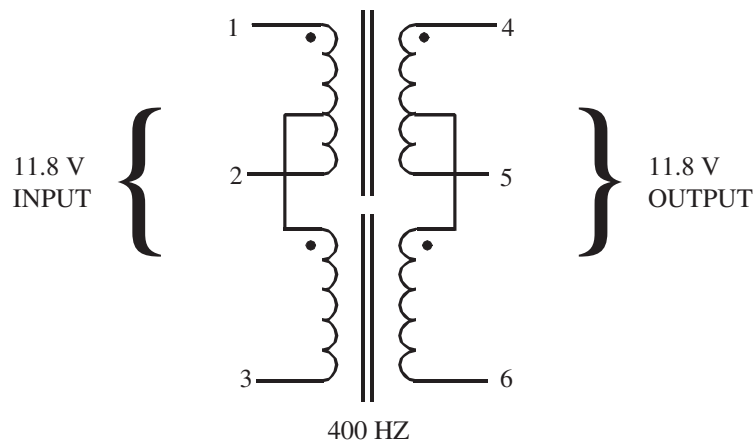
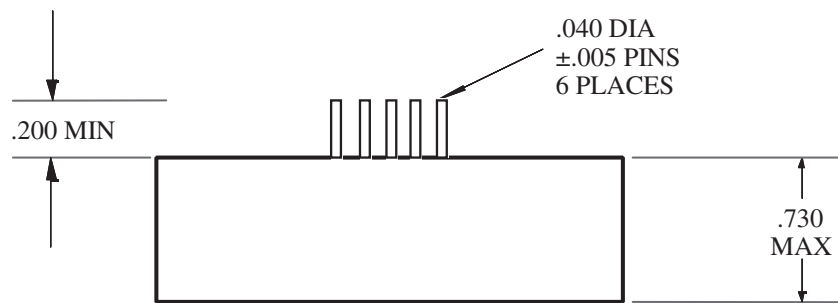


NOTE:  
FOR REFERENCE ONLY, CONTACT BETA TRANSFORMER CORPORATION FOR SPEC DETAILS.

**FIGURE 14. DDC 42359 OUTLINE DRAWING (26 VOLT POWER TRANSFORMER)**



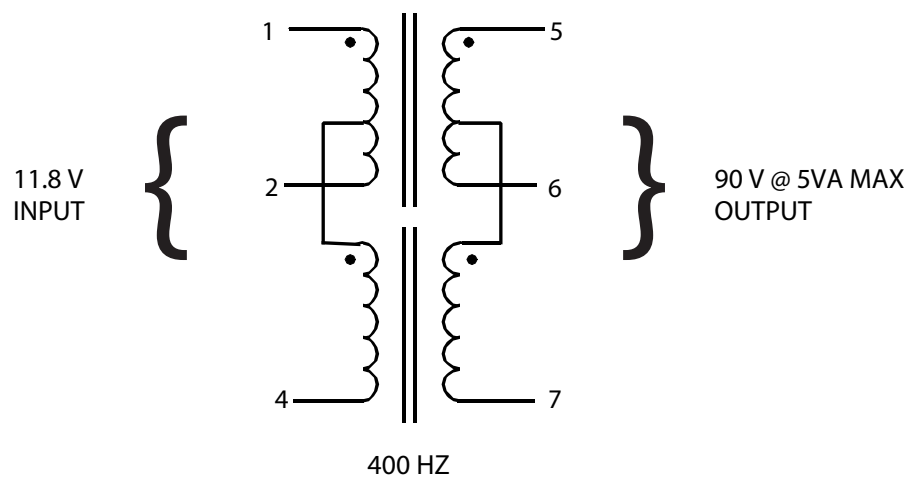
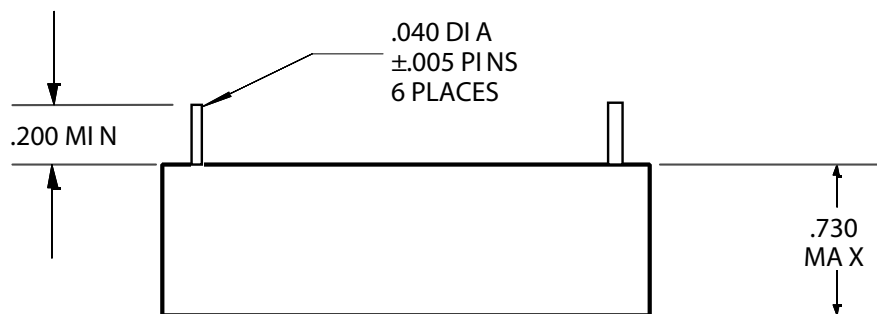
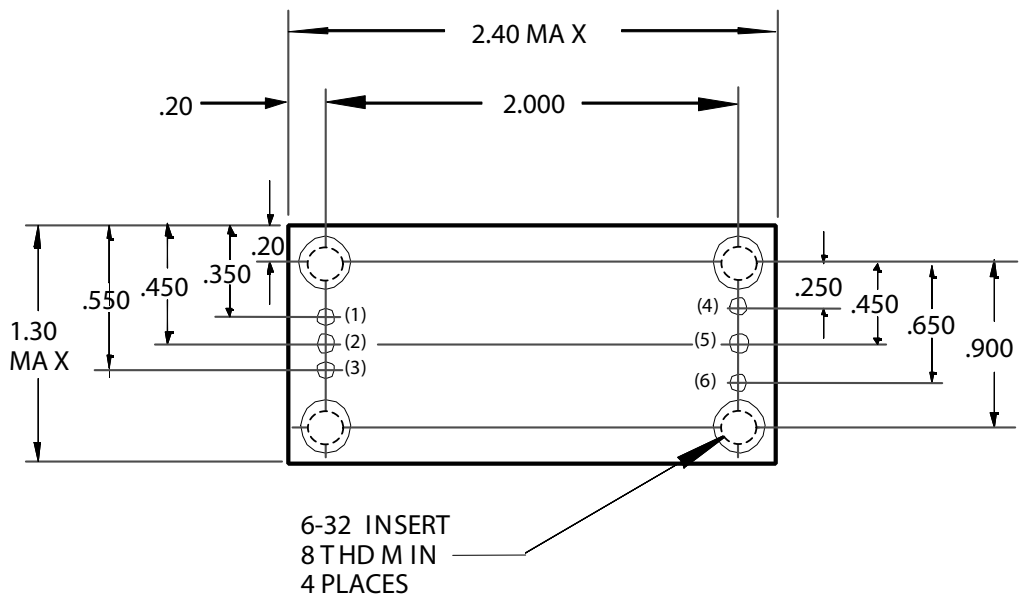
6-32 STAINLESS STEEL INSERTS  
8 THD MIN (4 REQ'D)



11.8 V SYNCHRO TO 11.8 V SYNCHRO AT 400 HZ, 5VA MAX  
(USE FOR S2 GROUNDED APPLICATIONS)

NOTE: FOR REF ONLY, CONTACT BETA TRANSFORMER CORPORATION  
FOR SPEC DETAILS.

**FIGURE 15. DDC 42929 OUTLINE DRAWING**



NOTE: FOR REF ONLY, CONTACT BETA TRANSFORMER CORPORATION FOR SPEC DETAILS.

**FIGURE 16. DDC 41402 OUTLINE DRAWING**

## ORDERING INFORMATION

### DSC-10510-XXXX

#### Supplemental Process Requirements:

- S = Pre-Cap Source Inspection
- L = Pull Test
- Q = Pull Test and Pre-Cap Inspection
- Blank = None of the Above

#### Accuracy:

- 3 = ±4 minutes (No Load) + 1.6 minutes at full Load (7VA Inductive)
- 4 = ±2 minutes (No Load) + 1.6 minutes at full Load (7VA Inductive)

#### Process Requirements:

- 0 = Standard DDC Processing, no Burn-In (See table below.)
- 1 = MIL-PRF-38534 Compliant (Note 3)
- 2 = B (Note 1)
- 3 = MIL-PRF-38534 Compliant with PIND Testing (Note 3)
- 4 = MIL-PRF-38534 Compliant with Solder Dip (Note 3)
- 5 = MIL-PRF-38534 Compliant with PIND Testing and Solder Dip (Note 3)
- 6 = B (Note 1) with PIND Testing
- 7 = B (Note 1) with Solder Dip
- 8 = B (Note 1) with PIND Testing and Solder Dip
- 9 = Standard DDC Processing with Solder Dip, no Burn-In (See table below.)

#### Temperature Grade/Data Requirements:

- 1 = -55°C to +125°C
- 2 = -40°C to +85°C
- 3 = 0°C to +70°C
- 4 = -55°C to +125°C with Variables Test Data
- 5 = -40°C to +85°C with Variables Test Data
- 8 = 0°C to +70°C with Variables Test Data

## TRANSFORMERS

- 1) Optional Power Transformer, DDC P/N 42359 (See Figure 2 & 14)
- 2) For S2 Grounded Applications, use Transformer DDC P/N 42929 (Figure 15)  
Synchro to Synchro 11.8v TO 11.8v 400Hz
- 3) Synchro 11.8v to Synchro 90v, 400Hz 5 VA max, see Beta Scott-T #41402 (Figure 16).

#### Notes:

1. Standard DDC Processing with burn-in and full temperature test—see table below.
2. These products contain tin-lead solder finish as applicable to solder dip requirements.
3. MIL-PRF-38534 product grading is designated with the following dash numbers:  
Class H is a -11X, 13X, 14X, 15X, 41X, 43X, 44X, 45X  
Class G is a -21X, 23X, 24X, 25X, 51X, 53X, 54X, 55X  
Class D is a -31X, 33X, 34X, 35X, 81X, 83X, 84X, 85X

STANDARD DDC PROCESSING FOR HYBRID AND MONOLITHIC HERMETIC PRODUCTS		
TEST	MIL-STD-883	
	METHOD(S)	CONDITION(S)
INSPECTION	2009, 2010, 2017, and 2032	—
SEAL	1014	A and C
TEMPERATURE CYCLE	1010	C
CONSTANT ACCELERATION	2001	3000g
BURN-IN	1015 (note 1), 1030 (note 2)	TABLE 1

#### Notes:

1. For Process Requirement "B" (refer to ordering information), devices may be non-compliant with MIL-STD-883, Test Method 1015, Paragraph 3.2. Contact factory for details.
2. When applicable.

The information in this data sheet is believed to be accurate; however, no responsibility is assumed by Data Device Corporation for its use, and no license or rights are granted by implication or otherwise in connection therewith.  
Specifications are subject to change without notice.

Please visit our web site at [www.ddc-web.com](http://www.ddc-web.com) for the latest information.



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