28F016SV
16-MBIT (1 MBIT x 16, 2 MBIT x 8) FlashFile™ MEMORY

Includes Commercial and Extended Temperature Specifications

- **SmartVoltage Technology**
  - **— User-Selectable 3.3V or 5V V_{CC}**
  - **— User-Selectable 5V or 12V V_{PP}**
- **65 ns Access Time**
- **1 Million Erase Cycles per Block**
- **30.8 MB/sec Burst Write Transfer Rate**
- **0.48 MB/sec Sustainable Write Transfer Rate**
- **Configurable x8 or x16 Operation**
- **56-Lead TSOP and SSOP Type I Packages**
- **Backwards-Compatible with 28F016SA, 28F008SA Command Set**
- **Revolutionary Architecture**
  - **— Multiple Command Execution**
  - **— Program during Erase**
  - **— Command Super-Set of the Intel 28F008SA**
  - **— Page Buffer Program**
- **2 µA Typical Deep Power-Down**
- **32 Independently Lockable Blocks**
- **State-of-the-Art 0.6 µm ETOX™ IV Flash Technology**

Intel's 28F016SV 16-Mbit FlashFile™ memory is a revolutionary architecture which is the ideal choice for designing embedded direct-execute code and mass storage data/file flash memory systems. With innovative capabilities, low-power operation, user-selectable V_{PP} voltage and high read/program performance, the 28F016SV enables the design of truly mobile, high-performance personal computing and communications products.

The 28F016SV is the highest density, highest performance nonvolatile read/program solution for solid-state storage applications. Its symmetrically-blocked architecture (100% compatible with the 28F008SA 8-Mbit and 28F016SA 16-Mbit FlashFile memories), extended cycling, flexible V_{CC} and V_{PP} voltage (SmartVoltage technology), fast program and read performance and selective block locking, provide a highly-flexible memory component suitable for Resident Flash Arrays, high-density memory cards and PCMCIA-ATA flash drives. The 28F016SV's dual read voltage enables the design of memory cards which can be read/written in 3.3V and 5V systems interchangeably. Its x8/x16 architecture allows optimization of the memory-to-processor interface. The flexible block locking option enables bundling of executable application software in a Resident Flash Array or memory card. The 28F016SV is manufactured on Intel's 0.6 µm ETOX IV process technology.

July 1997

Order Number: 290528-007

The 28F016SV may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

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REVISION HISTORY

Number	Description
-001	Original Version
-002	Added 28F016SV-065/-070 at 5V V_{CC} and 28F016SV-075 at 3.3V V_{CC}. Improved burst write transfer rate to 30.8 MB/sec. Added 56-lead SSOP Type I packaging information. Changed V_{PPLK} from 2V to 1.5V. Increased I_{CCR} at 5V V_{CC} and 3.3V V_{CC}: I_{CCR1} from 30 mA (typ)/35 mA (max) to 40 mA (typ)/50 mA (max) @ V_{CC} = 3.3V I_{CCR2} from 15 mA (typ)/20 mA (max) to 20 mA (typ)/30 mA (max) @ V_{CC} = 3.3V I_{CCR1} from 50 mA (typ)/60 mA (max) to 75 mA (typ)/95 mA (max) @ V_{CC} = 5V I_{CCR2} from 30 mA (typ)/35 mA (max) to 45 mA (typ)/55 mA (max) @ V_{CC} = 5V Moved AC Characteristics for Extended Register Reads into separate table. Increased V_{PP} MAX from 13V to 14V. Added Erase Suspend Command Latency times to Section 5.12 Modified Device Nomenclature Section to include SSOP package option and Ordering Information
-003	Changed definition of “NC.” Removed “No internal connection to die” from description. Added “xx” to Upper Byte of Command (Data) Definition in Sections 4.3 and 4.4. Added Note to Sleep Command (Section 4.4) denoting that the chip must be de-selected in order for the power consumption in sleep mode to reach deep power-down levels. Modified parameters “V” and “I” of Section 5.1 to apply to “NC” pins. Increased I_{PPR} (V_{PP} Read Current) for V_{PP}> V_{CC} to 200 µA at V_{CC} = 3.3V and V_{CC} = 5V Changed V_{CC} = 5V DC Characteristics (Section 5.5) marked with Note 1 to indicate that these currents are specified for a CMOS rise/fall time (10% to 90%) of <5 ns and a TTL rise/fall time of <10 ns. Corrected the graphical representation of t_{WHGL} and t_{EHGL} in Figures 15 and 16. Increased Typical “Page Buffer Byte/Word Program Times” from 6.0 µs to 8.0 µs (Byte) and 12.1 µs to 16.0 µs (Word) @ V_{CC} = 3.3V/5V and V_{PP} = 5V: Increased Typ. “Byte/Word Program Times” (t_{WHRH1A}/t_{WHRH1B}) for V_{PP} = 5V (Section 5.12) t_{WHRH1A} from 16.5 µs to 29.0 µs and t_{WHRH1B} from 24.0 µs to 35.0 µs at V_{CC} =3.3V t_{WHRH1A} from 11.0 µs to 20.0 µs and t_{WHRH1B} from 16.0 µs to 25.0 µs at V_{CC} = 5V Increased Typical “Block Program Times” (t_{WHRH2}/t_{WHRH3})for V_{PP} =5V (Section 5.12): t_{WHRH2} from 1.1 sec to 1.9 sec and t_{WHRH3} from 0.8 sec to 1.2 sec at V_{CC} = 3.3V t_{WHRH2} from 0.8 sec to 1.4 sec and t_{WHRH3} from 0.6 sec to 0.85 sec at V_{CC} = 5V Changed “Time from Erase Suspend Command to WSM Ready” spec name to “Erase Suspend Latency Time to Read;” modified typical values and added Min/Max values at V_{CC} =3.3/5V and V_{PP} =5V/12V (Section 5.12) Added “Erase Suspend Latency Time to Program” Specifications to Section 5.12 Minor cosmetic changes throughout document

REVISION HISTORY (Continued)

Number	Description
-004	Added 3/5# pin to Block Diagram (Figure 1), Pinout Configurations (Figures 2 and 3), Product Overview (Section 1.1) and Lead Descriptions (Section 2.1) Added 3/5# pin to Test Conditions of I_{CCS} Specifications Added 3/5# pin (Y) to Timing Nomenclature (Section 5.5) Increased t_{PHQV} Specifications at 5V V_{CC} to 400 ns for E28F016SV 065 devices and 480 ns for E28F106SV 070 devices. Modified Power-Up and Reset Timings (Section 5.9) to include 3/5# pin: Removed t_{5VPH} and t_{3VPH} specifications; Added t_{PLYL}, t_{PLYH}, t_{YLPH}, and t_{YHPH} specifications Added t_{PHEL3} and t_{PHEL5} specifications to Power-Up and Reset Timings (Section 5.9) Corrected TSOP Mechanical Specification A_1 from 0.50 mm to 0.050 mm (Section 6.0) Corrected SSOP Mechanical Spec. B (max) from 0.20 mm to 0.40 mm (Section 6.0) Minor cosmetic changes throughout document.
-005	Updated DC Specifications: I_{CCD}, I_{PPES} Updated AC Specifications: Page Buffer Reads: (t_{AVAV}, t_{AVQV}, t_{ELQV}, and t_{FLQV}/t_{FHQV}) Page Buffer WE#-Controlled Command Writes (t_{ELWL}) CE#-Controlled Command Write Parameters (t_{AVAV}, t_{ELEH}, t_{EHEL}) Combined Commercial and Extended Temperature information into single datasheet.
-006	Updated AC Specifications: Page Buffer Reads: (t_{AVAV}, t_{AVQV}, t_{ELQV}, and t_{FLQV}/t_{FHQV})
-007	Updated Disclaimer

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1.0 INTRODUCTION

The documentation of the Intel 28F016SV memory device includes this datasheet, a detailed user's manual, and a number of application notes and design tools, all of which are referenced in Appendix B.

The datasheet is intended to give an overview of the chip feature-set and of the operating AC/DC specifications. The *16-Mbit Flash Product Family User's Manual* provides complete descriptions of the user modes, system interface examples and detailed descriptions of all principles of operation. It also contains the full list of software algorithm flowcharts, and a brief section on compatibility with the Intel 28F008SA.

A significant 28F016SV change occurred between datasheet revisions 290528-003 and 290528-004. This change centers around the addition of a 3/5# pin to the device's pinout configuration. Figures 2 and 3 show the 3/5# pin assignment for TSOP and SSOP Type 1 packages. Intel recommends that all customers obtain the latest revisions of 28F016SV documentation.

1.1 Enhanced Features

The 28F016SV is backwards compatible with the 28F016SA and offers the following enhancements:

- SmartVoltage Technology
  - Selectable 5V or 12V V_{PP}
- V_{PP} Level Bit in Block Status Register
- Additional RY/BY# Configuration
  - Pulse-On-Program/Erase
- Additional Upload Device Information Command Feedback
  - Device Proliferation Code
  - Device Configuration Code

1.2 Product Overview

The 28F016SV is a high-performance, 16-Mbit (16,777,216-bit) block erasable, nonvolatile random access memory, organized as either 1 Mword x 16 or 2 Mbyte x 8. The 28F016SV includes thirty-two 64-KB (65,536 byte) blocks or thirty-two 32-KW (32,768 word) blocks. A chip memory map is shown in Figure 4.

The implementation of a new architecture, with many enhanced features, will improve the device operating characteristics and result in greater product reliability and ease-of-use.

The 28F016SV incorporates SmartVoltage technology, providing V_{CC} operation at both 3.3V and 5V and program and erase capability at V_{PP} = 12V or 5V. Operating at V_{CC} = 3.3V, the 28F016SV consumes approximately one half the power consumption at 5V V_{CC}, while 5V V_{CC} provides the highest read performance capability. V_{PP} = 5V operation eliminates the need for a separate 12V converter, while V_{PP} = 12V maximizes program/erase performance. In addition to the flexible program and erase voltages, the dedicated V_{PP} gives complete code protection with $V_{PP} \leq V_{PPLK}$.

A 3/5# input pin configures the device's internal circuitry for optimal 3.3V or 5V read/program operation.

A Command User Interface (CUI) serves as the system interface between the microprocessor or microcontroller and the internal memory operation.

Internal Algorithm Automation allows byte/word programs and block erase operations to be executed using a Two-Program command sequence to the CUI in the same way as the 28F008SA 8-Mbit FlashFile™ memory.

A super-set of commands has been added to the basic 28F008SA command-set to achieve higher program performance and provide additional capabilities. These new commands and features include:

- Page Buffer Programs to Flash
- Command Queuing Capability
- Automatic Data Programs during Erase
- Software Locking of Memory Blocks
- Two-Byte Successive Programs in 8-bit Systems
- Erase All Unlocked Blocks

Writing of memory data is performed in either byte or word increments typically within 6 µs (12V V_{PP})—a 33% improvement over the 28F008SA. A block erase operation erases one of the 32 blocks in typically 0.6 sec (12V V_{PP}), independent of the other blocks, which is about a 65% improvement over the 28F008SA.

Each block can be written and erased a minimum of 100,000 cycles. Systems can achieve one million Block Erase Cycles by providing wear-leveling algorithms and graceful block retirement. These techniques have already been employed in many flash file systems and hard disk drive designs.

The 28F016SV incorporates two Page Buffers of 256 bytes (128 words) each to allow page data programs. This feature can improve a system program performance by up to 4.8 times over previous flash memory devices, which have no Page Buffers.

All operations are started by a sequence of Program commands to the device. Three Status Registers (described in detail later in this datasheet) and a RY/BY# output pin provide information on the progress of the requested operation.

While the 28F008SA requires an operation to complete before the next operation can be requested, the 28F016SV allows queuing of the next operation while the memory executes the current operation. This eliminates system overhead when writing several bytes in a row to the array or erasing several blocks at the same time. The 28F016SV can also perform program operations to one block of memory while performing erase of another block.

The 28F016SV provides selectable block locking to protect code or data such as Device Drivers, PCMCIA card information, ROM-Executable O/S or Application Code. Each block has an associated nonvolatile lock-bit which determines the lock status of the block. In addition, the 28F016SV has a master Write Protect pin (WP#) which prevents any modifications to memory blocks whose lock-bits are set.

The 28F016SV contains three types of Status Registers to accomplish various functions:

- A Compatible Status Register (CSR) which is 100% compatible with the 28F008SA FlashFile memory Status Register. The CSR, when used alone, provides a straightforward upgrade capability to the 28F016SV from a 28F008SA-based design.
- A Global Status Register (GSR) which informs the system of command Queue status, Page Buffer status, and overall Write State Machine (WSM) status.
- 32 Block Status Registers (BSRs) which provide block-specific status information such as the block lock-bit status.

The GSR and BSR memory maps for byte-wide and word-wide modes are shown in Figures 5 and 6.

The 28F016SV incorporates an open drain RY/BY# output pin. This feature allows the user to OR-tie many RY/BY# pins together in a multiple memory configuration such as a Resident Flash Array.

Other configurations of the RY/BY# pin are enabled via special CUI commands and are described in detail in the *16-Mbit Flash Product Family User's Manual.*

The 28F016SV's enhanced Upload Device Information command provides access to additional information that the 28F016SA previously did not offer. This command uploads the Device Revision Number, Device Proliferation Code and Device Configuration Code to the page buffer. The Device Proliferation Code for the 28F016SV is 01H, and the Device Configuration Code identifies the current RY/BY# configuration. Section 4.4 documents the exact page buffer address locations for all uploaded information. A subsequent Page Buffer Swap and Page Buffer Read command sequence is necessary to read the correct device information.

The 28F016SV also incorporates a dual chip-enable function with two input pins, CE_0# and CE_1#. These pins have exactly the same functionality as the regular chip-enable pin, CE#, on the 28F008SA. For minimum chip designs, CE_1# may be tied to ground and system logic may use CE_0# as the chip enable input. The 28F016SV uses the logical combination of these two signals to enable or disable the entire chip. Both CE_0# and CE_1# must be active low to enable the device. If either one becomes inactive, the chip will be disabled. This feature, along with the open drain RY/BY# pin, allows the system designer to reduce the number of control pins used in a large array of 16-Mbit devices.

The BYTE# pin allows either x8 or x16 read/programs to the 28F016SV. BYTE# at logic low selects 8-bit mode with address A_0 selecting between the low byte and high byte. On the other hand, BYTE# at logic high enables 16-bit operation with address A_1 becoming the lowest order address and address A_0 is not used (don't care). A device block diagram is shown in Figure 1.

The 28F016SV is specified for a maximum access time of 65 ns (t_{ACC}) at 5V operation (4.75V to 5.25V) over the commercial temperature range (0°C to +70°C). A corresponding maximum access time of 75 ns at 3.3V (3.0V to 3.6V and 0°C to +70°C) is achieved for reduced power consumption applications.

The 28F016SV incorporates an Automatic Power Saving (APS) feature, which substantially reduces the active current when the device is in static mode of operation (addresses not switching). In APS mode, the typical I_{CC} current is 1 mA at 5V (3.0 mA at 3.3V).

A deep power-down mode of operation is invoked when the RP# (called PWD# on the 28F008SA) pin transitions low. This mode brings the device power consumption to less than 2.0 µA, typically, and provides additional program protection by acting as a device reset pin during power transitions. A reset time of 400 ns (5V V_{CC} operation) is required from RP# switching high until outputs are again valid. In the Deep Power-Down state, the WSM is reset (any current operation will abort) and the CSR, GSR and BSR registers are cleared.

A CMOS standby mode of operation is enabled when either CE_0# or CE_1# transitions high and RP# stays high with all input control pins at CMOS levels. In this mode, the device typically draws an I_{CC} standby current of 70 µA at 5V V_{CC}.

The 28F016SV will be available in 56-lead, 1.2 mm thick, 14 mm x 20 mm TSOP and 56-lead, 1.8 mm thick, 16 mm x 23.7 SSOP Type I packages. The form factor and pinout of these two packages allow for very high board layout densities.

2.0 DEVICE PINOUT

The 28F016SV 56-lead TSOP and 56-lead SSOP Type I pinout configurations are shown in Figures 2 and 3.

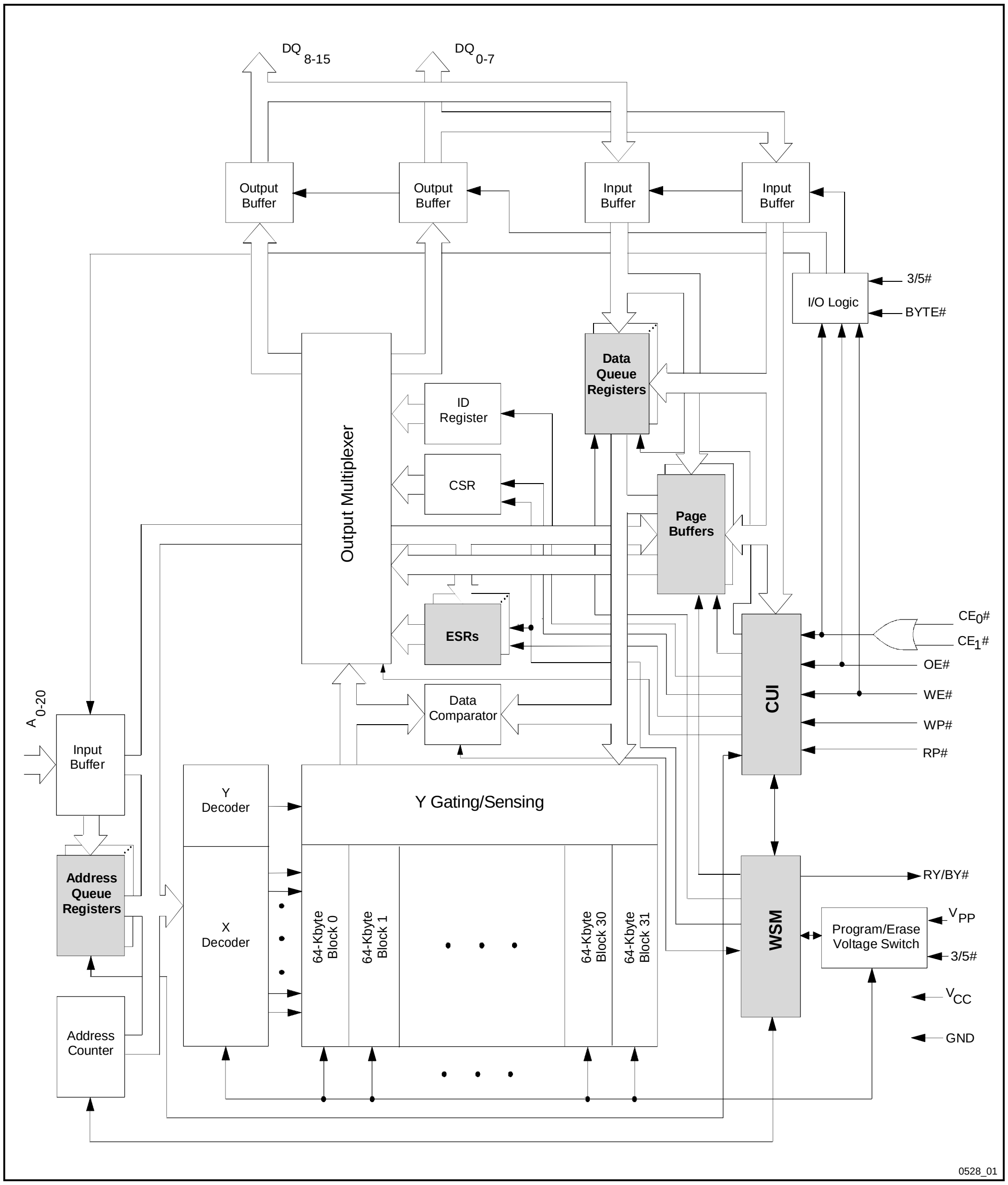


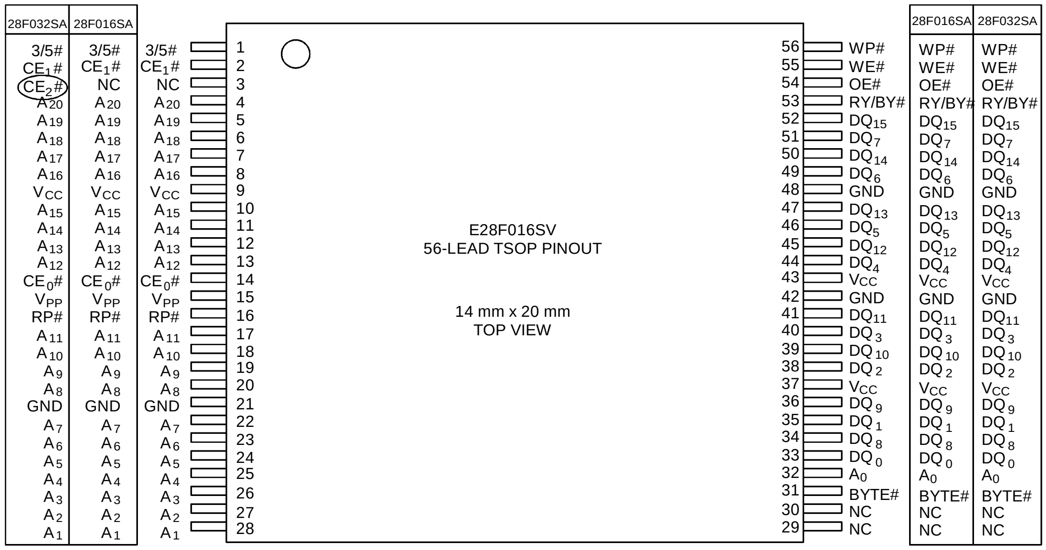
Figure 1. 28F016SV Block Diagram
Architectural Evolution Includes SmartVoltage Technology, Page Buffers, Queue Registers and Extended Registers

2.1 Lead Descriptions

Symbol	Type	Name and Function
A_0	INPUT	**BYTE-SELECT ADDRESS:** Selects between high and low byte when device is in x8 mode. This address is latched in x8 data programs. Not used in x16 mode (i.e., the A_0 input buffer is turned off when BYTE# is high).
A_1–A_{15}	INPUT	**WORD-SELECT ADDRESSES:** Select a word within one 64-Kbyte block. A_{6-15} selects 1 of 1024 rows, and A_{1-5} selects 16 of 512 columns. These addresses are latched during data programs.
A_{16}–A_{20}	INPUT	**BLOCK-SELECT ADDRESSES:** Select 1 of 32 Erase blocks. These addresses are latched during data programs, erase and lock block operations.
DQ_0–DQ_7	INPUT/OUTPUT	**LOW-BYTE DATA BUS:** Inputs data and commands during CUI program cycles. Outputs array, buffer, identifier or status data in the appropriate read mode. Floated when the chip is de-selected or the outputs are disabled.
DQ_8–DQ_{15}	INPUT/OUTPUT	**HIGH-BYTE DATA BUS:** Inputs data during x16 data program operations. Outputs array, buffer or identifier data in the appropriate read mode; not used for Status Register reads. Floated when the chip is de-selected or the outputs are disabled.
CE_0#, CE_1#	INPUT	**CHIP ENABLE INPUTS**: Activate the device's control logic, input buffers, decoders and sense amplifiers. With either CE_0# or CE_1# high, the device is de-selected and power consumption reduces to standby levels upon completion of any current data program or erase operations. Both CE_0# and CE_1# must be low to select the device. All timing specifications are the same for both signals. Device Selection occurs with the latter falling edge of CE_0# or CE_1#. The first rising edge of CE_0# or CE_1# disables the device.
RP#	INPUT	**RESET/POWER-DOWN:** RP# low places the device in a deep power-down state. All circuits that consume static power, even those circuits enabled in standby mode, are turned off. When returning from deep power-down, a recovery time of t_{PHQV} is required to allow these circuits to power-up. When RP# goes low, any current or pending WSM operation(s) are terminated, and the device is reset. All Status Registers return to ready (with all status flags cleared). Exit from deep power-down places the device in read array mode.
OE#	INPUT	**OUTPUT ENABLE:** Gates device data through the output buffers when low. The outputs float to tri-state off when OE# is high. **NOTE:** CE_X# overrides OE#, and OE# overrides WE#.
WE#	INPUT	**WRITE ENABLE:** Controls access to the CUI, Page Buffers, Data Queue Registers and Address Queue Latches. WE# is active low, and latches both address and data (command or array) on its rising edge. Page Buffer addresses are latched on the falling edge of WE#.

2.1 Lead Descriptions (Continued)

Symbol	Type	Name and Function
RY/BY#	OPEN DRAIN OUTPUT	**READY/BUSY:** Indicates status of the internal WSM. When low, it indicates that the WSM is busy performing an operation. RY/BY# floating indicates that the WSM is ready for new operations (or WSM has completed all pending operations), or erase is suspended, or the device is in deep power-down mode. This output is always active (i.e., not floated to tri-state off when OE# or CE_0#, CE_1# are high), except if a RY/BY# Pin Disable command is issued.
WP#	INPUT	**WRITE PROTECT:** Erase blocks can be locked by writing a nonvolatile lock-bit for each block. When WP# is low, those locked blocks as reflected by the Block-Lock Status bits (BSR.6), are protected from inadvertent data programs or erases. When WP# is high, all blocks can be written or erased regardless of the state of the lock-bits. The WP# input buffer is disabled when RP# transitions low (deep power-down mode).
BYTE#	INPUT	**BYTE ENABLE:** BYTE# low places device in x8 mode. All data is then input or output on DQ_{0-7}, and DQ_{8-15} float. Address A_0 selects between the high and low byte. BYTE# high places the device in x16 mode, and turns off the A_0 input buffer. Address A_1, then becomes the lowest order address.
3/5#	INPUT	**3.3/5.0 VOLT SELECT:** 3/5# high configures internal circuits for 3.3V operation. 3/5# low configures internal circuits for 5V operation. **NOTE:** Reading the array with 3/5# high in a 5V system could damage the device. Reference the power-up and reset timings (Section 5.7) for 3/5# switching delay to valid data.
V_{PP}	SUPPLY	**PROGRAM/ERASE POWER SUPPLY (12V ± 0.6V, 5V ± 0.5V) :** For erasing memory array blocks or writing words/bytes/pages into the flash array. V_{PP} = 5V ± 0.5V eliminates the need for a 12V converter, while connection to 12V ± 0.6V maximizes Program/Erase Performance. **NOTE:** Successful completion of program and erase attempts is inhibited with V_{PP} at or below 1.5V. Program and erase attempts with V_{PP} between 1.5V and 4.5V, between 5.5V and 11.4V, and above 12.6V produce spurious results and should not be attempted.
V_{CC}	SUPPLY	**DEVICE POWER SUPPLY (3.3V ± 0.3V, 5V ± 0.5V, 5.0 ± 0.25V):** To switch 3.3V to 5V (or vice versa), first ramp V_{CC} down to GND, and then power to the new V_{CC} voltage. Do not leave any power pins floating.
GND	SUPPLY	**GROUND FOR ALL INTERNAL CIRCUITRY:** Do not leave any ground pins floating.
NC		**NO CONNECT:** Lead may be driven or left floating.



NOTE:

56-lead TSOP Mechanical Diagrams and dimensions are shown at the end of this datasheet.

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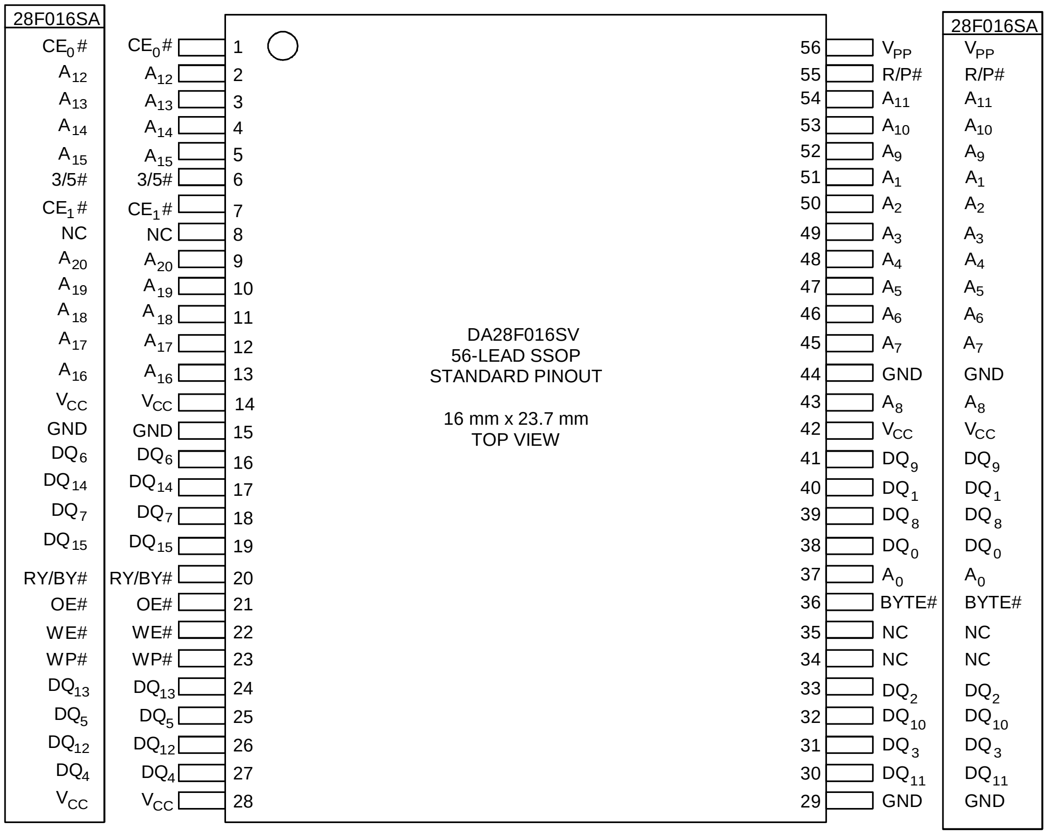
Figure 2. 28F016SV 56-Lead TSOP Pinout Configuration Shows Compatibility with 28F016SA/28F032SA



NOTE:

56-lead SSOP Mechanical Diagrams and dimensions are shown at the end of this datasheet.

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Figure 3. 56-Lead SSOP Pinout Configuration

3.0 MEMORY MAPS

Block	Byte-Wide (x8) Mode $A_{[20-0]}$	64-Kbyte Block	Word-Wide (x16) Mode $A_{[20-1]}$	32-Kword Block
31	1FFFFF – 1F0000	64-Kbyte Block	FFFFF – F8000	32-Kword Block
30	1EFFFF – 1E0000	64-Kbyte Block	F7FFF – F0000	32-Kword Block
29	1DFFFF – 1D0000	64-Kbyte Block	EFFFF – E8000	32-Kword Block
28	1CFFFF – 1C0000	64-Kbyte Block	E7FFF – E0000	32-Kword Block
27	1BFFFF – 1B0000	64-Kbyte Block	DFFFF – D8000	32-Kword Block
26	1AFFFF – 1A0000	64-Kbyte Block	D7FFF – D0000	32-Kword Block
25	19FFFF – 190000	64-Kbyte Block	CFFFF – C8000	32-Kword Block
24	18FFFF – 180000	64-Kbyte Block	C7FFF – C0000	32-Kword Block
23	17FFFF – 170000	64-Kbyte Block	BFFFF – B8000	32-Kword Block
22	16FFFF – 160000	64-Kbyte Block	B7FFF – B0000	32-Kword Block
21	15FFFF – 150000	64-Kbyte Block	A8FFF – A8000	32-Kword Block
20	14FFFF – 140000	64-Kbyte Block	A7FFF – A0000	32-Kword Block
19	13FFFF – 130000	64-Kbyte Block	9FFFF – 98000	32-Kword Block
18	12FFFF – 120000	64-Kbyte Block	97FFF – 90000	32-Kword Block
17	11FFFF – 110000	64-Kbyte Block	8FFFF – 88000	32-Kword Block
16	10FFFF – 100000	64-Kbyte Block	87FFF – 80000	32-Kword Block
15	0FFFFF – 0F0000	64-Kbyte Block	7FFFF – 78000	32-Kword Block
14	0EFFFF – 0E0000	64-Kbyte Block	77FFF – 70000	32-Kword Block
13	0DFFFF – 0D0000	64-Kbyte Block	6FFFF – 68000	32-Kword Block
12	0CFFFF – 0C0000	64-Kbyte Block	67FFF – 60000	32-Kword Block
11	0BFFFF – 0B0000	64-Kbyte Block	5FFFF – 58000	32-Kword Block
10	0AFFFF – 0A0000	64-Kbyte Block	57FFF – 50000	32-Kword Block
9	09FFFF – 090000	64-Kbyte Block	4FFFF – 48000	32-Kword Block
8	08FFFF – 080000	64-Kbyte Block	47FFF – 40000	32-Kword Block
7	07FFFF – 070000	64-Kbyte Block	3FFFF – 38000	32-Kword Block
6	06FFFF – 060000	64-Kbyte Block	37FFF – 30000	32-Kword Block
5	05FFFF – 050000	64-Kbyte Block	2FFFF – 28000	32-Kword Block
4	04FFFF – 040000	64-Kbyte Block	27FFF – 20000	32-Kword Block
3	03FFFF – 030000	64-Kbyte Block	1FFFF – 18000	32-Kword Block
2	02FFFF – 020000	64-Kbyte Block	17FFF – 10000	32-Kword Block
1	01FFFF – 010000	64-Kbyte Block	0FFFF – 08000	32-Kword Block
0	00FFFF – 000000	64-Kbyte Block	07FFF – 00000	32-Kword Block

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Figure 4. 28F016SV Memory Maps (Byte-Wide and Word-Wide Modes)

3.1 Extended Status Registers Memory Map

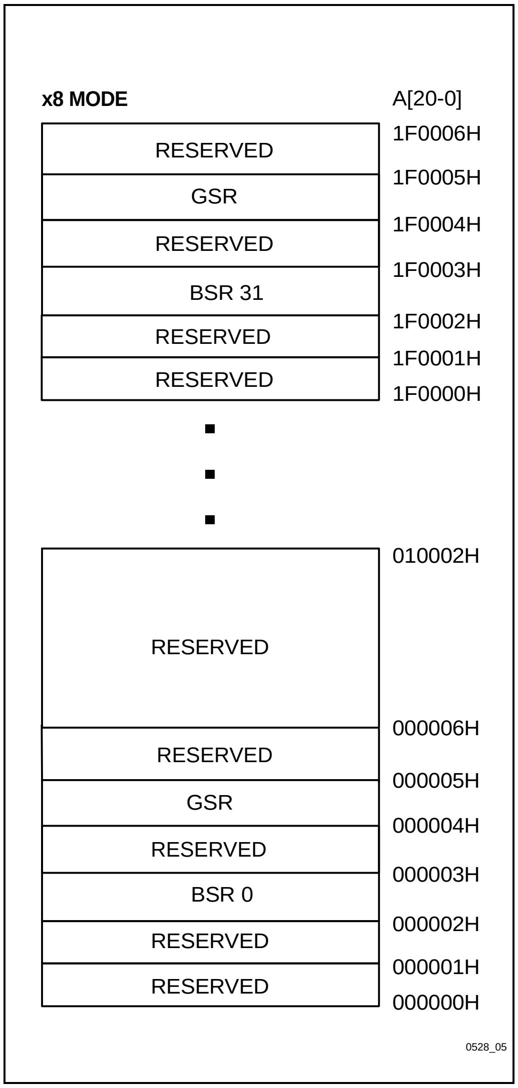


Figure 5. Extended Status Register Memory Map (Byte-Wide Mode)

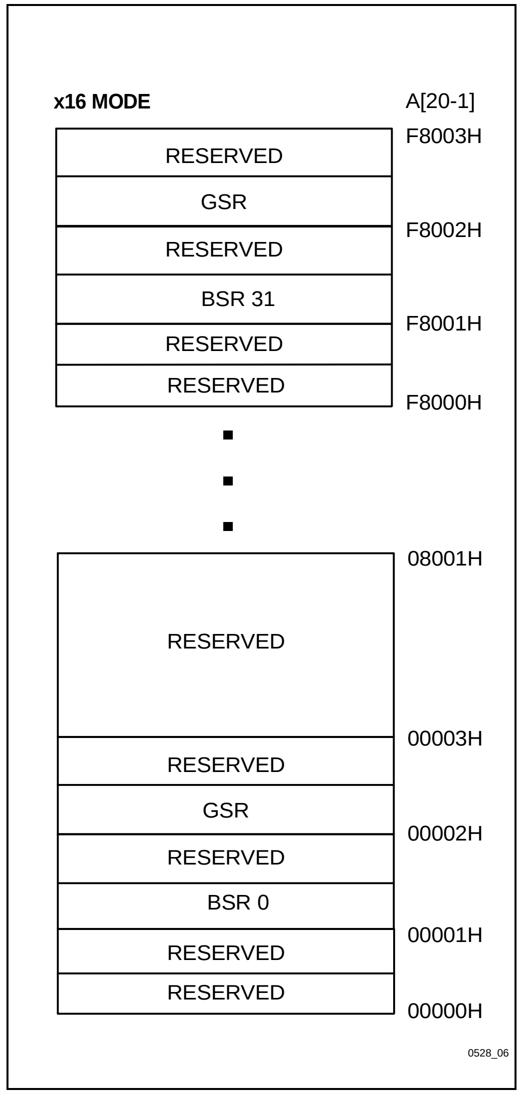


Figure 6. Extended Status Register Memory Map (Word-Wide Mode)

4.0 BUS OPERATIONS, COMMANDS AND STATUS REGISTER DEFINITIONS

4.1 Bus Operations for Word-Wide Mode (BYTE# = V_{IH})

Mode	Notes	RP#	CE_1#	CE_0#	OE#	WE#	A_1	DQ_{0-15}	RY/BY#
Read	1,2,7	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	D_{OUT}	X
Output Disable	1,6,7	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	High Z	X
Standby	1,6,7	V_{IH}	V_{IL} V_{IH} V_{IH}	V_{IH} V_{IL} V_{IH}	X	X	X	High Z	X
Deep Power-Down	1,3	V_{IL}	X	X	X	X	X	High Z	V_{OH}
Manufacturer ID	4	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	0089H	V_{OH}
Device ID	4,8	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	66A0H	V_{OH}
Write	1,5,6	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	D_{IN}	X

4.2 Bus Operations for Byte-Wide Mode (BYTE# = V_{IL})

Mode	Notes	RP#	CE_1#	CE_0#	OE#	WE#	A_0	DQ_{0-7}	RY/BY#
Read	1,2,7	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	D_{OUT}	X
Output Disable	1,6,7	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	High Z	X
Standby	1,6,7	V_{IH}	V_{IL} V_{IH} V_{IH}	V_{IH} V_{IL} V_{IH}	X	X	X	High Z	X
Deep Power-Down	1,3	V_{IL}	X	X	X	X	X	High Z	V_{OH}
Manufacturer ID	4	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	89H	V_{OH}
Device ID	4,8	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	A0H	V_{OH}
Write	1,5,6	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	D_{IN}	X

NOTES:

1. X can be V_{IH} or V_{IL} for address or control pins except for RY/BY#, which is either V_{OL} or V_{OH}.
2. RY/BY# output is open drain. When the WSM is ready, Erase is suspended or the device is in deep power-down mode. RY/BY# will be at V_{OH} if it is tied to V_{CC} through a resistor. RY/BY# at V_{OH} is independent of OE# while a WSM operation is in progress.
3. RP# at GND ± 0.2V ensures the lowest deep power-down current.
4. A_0 and A_1 at V_{IL} provide device manufacturer codes in x8 and x16 modes respectively. A_0 and A_1 at V_{IH} provide device ID codes in x8 and x16 modes respectively. All other addresses are set to zero.
5. Commands for erase, data program, or lock-block operations can only be completed successfully when $V_{PP} = V_{PPH1}$ or $V_{PP} = V_{PPH2}$.
6. While the WSM is running, RY/BY# in level-mode (default) stays at V_{OL} until all operations are complete. RY/BY# goes to V_{OH} when the WSM is not busy or in erase suspend mode.
7. RY/BY# may be at V_{OL} while the WSM is busy performing various operations (for example, a Status Register read during a program operation).
8. The 28F016SV shares an identical device identifier (66A0H in word-wide mode, A0H in byte-wide mode) with the 28F016SA. See application note *AP-393 28F016SV Compatibility with 28F016SA* for software and hardware techniques to differentiate between the 28F016SV and 28F016SA.

4.3 28F008SA—Compatible Mode Command Bus Definitions

Command	Notes	First Bus Cycle			Second Bus Cycle		
		Oper	Addr	Data(4)	Oper	Addr	Data(4)
Read Array		Write	X	xxFFH	Read	AA	AD
Intelligent Identifier	1	Write	X	xx90H	Read	IA	ID
Read Compatible Status Register	2	Write	X	xx70H	Read	X	CSRD
Clear Status Register	3	Write	X	xx50H			
Word/Byte Program		Write	X	xx40H	Write	PA	PD
Alternate Word/Byte Program		Write	X	xx10H	Write	PA	PD
Block Erase/Confirm		Write	X	xx20H	Write	BA	xxD0H
Erase Suspend/Resume		Write	X	xxB0H	Write	X	xxD0H

ADDRESS
AA = Array Address
BA = Block Address
IA = Identifier Address
PA = Program Address
X = Don't Care

DATA
AD = Array Data
CSRD = CSR Data
ID = Identifier Data
PD = Program Data

NOTES:

1. Following the Intelligent Identifier command, two Read operations access the manufacturer and device signature codes.
2. The CSR is automatically available after device enters data program, erase, or suspend operations.
3. Clears CSR.3, CSR.4 and CSR.5. Also clears GSR.5 and all BSR.5, BSR.4 and BSR.2 bits. See Status Register definitions.
4. The upper byte of the data bus (DQ_{8-15}) during command writes is a "Don't Care" in x16 operation of the device.

4.4 28F016SV—Performance Enhancement Command Bus Definitions

Command	Mode	Notes	First Bus Cycle			Second Bus Cycle			Third Bus Cycle		
			Oper	Addr	Data(13)	Oper	Addr	Data(13)	Oper	Addr	Data
Read Extended Status Register		1	Write	X	xx71H	Read	RA	GSRD BSRD			
Page Buffer Swap		7	Write	X	xx72H						
Read Page Buffer			Write	X	xx75H	Read	PBA	PD			
Single Load to Page Buffer			Write	X	xx74H	Write	PBA	PD			
Sequential Load to Page Buffer	x8	4,6,10	Write	X	xxE0H	Write	X	BCL	Write	X	BCH
	x16	4,5,6,10	Write	X	xxE0H	Write	X	WCL	Write	X	WCH
Page Buffer Write to Flash	x8	3,4,9,10	Write	X	xx0CH	Write	A_0	BC(L,H)	Write	PA	BC(H,L)
	x16	4,5,10	Write	X	xx0CH	Write	X	WCL	Write	PA	WCH
Two-Byte Program	x8	3	Write	X	xxFBH	Write	A_0	WD(L,H)	Write	PA	WD(H,L)
Lock Block/Confirm			Write	X	xx77H	Write	BA	xxD0H			
Upload Status Bits/Confirm		2	Write	X	xx97H	Write	X	xxD0H			
Upload Device Information/Confirm		11	Write	X	xx99H	Write	X	xxD0H			
Erase All Unlocked Blocks/Confirm			Write	X	xxA7H	Write	X	xxD0H			
RY/BY# Enable to Level-Mode		8	Write	X	xx96H	Write	X	xx01H			
RY/BY# Pulse-On-Write		8	Write	X	xx96H	Write	X	xx02H			
RY/BY# Pulse-On-Erase		8	Write	X	xx96H	Write	X	xx03H			
RY/BY# Disable		8	Write	X	xx96H	Write	X	xx04H			
RY/BY# Pulse-On-Write/Erase		8	Write	X	xx96H	Write	X	xx05H			
Sleep		12	Write	X	xxF0H						
Abort			Write	X	xx80H						

ADDRESS
BA = Block Address
PBA = Page Buffer Address
RA = Extended Register Address
PA = Program Address
X = Don't Care

DATA
AD = Array Data
PD = Page Buffer Data
BSRD = BSR Data
GSRD = GSR Data

WC (L,H) = Word Count (Low, High)
BC (L,H) = Byte Count (Low, High)
WD (L,H) = Write Data (Low, High)

NOTES:

1. RA can be the GSR address or any BSR address. See Figures 4 and 5 for Extended Status Register memory maps.
2. Upon device power-up, all BSR lock-bits come up locked. The Upload Status Bits command must be written to reflect the actual lock-bit status.
3. A_0 is automatically complemented to load second byte of data. BYTE# must be at V_{IL}.
   A_0 value determines which WD/BC is supplied first: A_0 = 0 looks at the WDL/BCL, A_0 = 1 looks at the WDH/BCH.
4. BCH/WCH must be at 00H for this product because of the 256-byte (128-word) Page Buffer size, and to avoid writing the Page Buffer contents to more than one 256-byte segment within an array block. They are simply shown for future Page Buffer expandability.
5. In x16 mode, only the lower byte DQ_{0-7} is used for WCL and WCH. The upper byte DQ_{8-15} is a don't care.
6. PBA and PD (whose count is given in cycles 2 and 3) are supplied starting in the fourth cycle, which is not shown.
7. This command allows the user to swap between available Page Buffers (0 or 1).
8. These commands reconfigure RY/BY# output to one of three pulse-modes or enable and disable the RY/BY# function.
9. Program address, PA, is the Destination address in the flash array which must match the Source address in the Page Buffer. Refer to the *16-Mbit Flash Product Family User's Manual*.
10. BCL = 00H corresponds to a byte count of 1. Similarly, WCL = 00H corresponds to a word count of 1.
11. After writing the Upload Device Information command and the Confirm command, the following information is output at Page Buffer addresses specified below:

Address	**Information**
06H, 07H (Byte Mode)	Device Revision Number
03H (Word Mode)	Device Revision Number
1EH (Byte Mode)	Device Configuration Code
0FH (DQ_{0-7})(Word Mode)	Device Configuration Code
1FH (Byte Mode)	Device Proliferation Code (01H)
0FH (DQ_{8-15})(Word Mode)	Device Proliferation Code (01H)

    A page buffer swap followed by a page buffer read sequence is necessary to access this information. The contents of all other Page Buffer locations, after the Upload Device Information command is written, are reserved for future implementation by Intel Corporation. See Section 4.8 for a description of the Device Configuration Code. This code also corresponds to data written to the 28F016SV after writing the RY/BY# Reconfiguration command.

12. To ensure that the 28F016SV's power consumption during sleep mode reaches the deep power-down current level, the system also needs to de-select the chip by taking either or both CE_0# or CE_1# high.
13. The upper byte of the data bus (DQ_{8-15}) during command writes is a "Don't Care" in x16 operation of the device.

4.5 Compatible Status Register

WSMS	ESS	ES	DWS	VPPS	R	R	R
7	6	5	4	3	2	1	0

	NOTES:
CSR.7 = WRITE STATE MACHINE STATUS 1 = Ready 0 = Busy	RY/BY# output or WSMS bit must be checked to determine completion of an operation (erase, erase suspend, or data program) before the appropriate Status bit (ESS, ES or DWS) is checked for success.
CSR.6 = ERASE-SUSPEND STATUS 1 = Erase Suspended 0 = Erase in Progress/Completed	
CSR.5 = ERASE STATUS 1 = Error in Block Erasure 0 = Successful Block Erase	If DWS and ES are set to “1” during an erase attempt, an improper command sequence was entered. Clear the CSR and attempt the operation again.
CSR.4 = DATA-WRITE STATUS 1 = Error in Data Program 0 = Data Program Successful	
CSR.3 = V_{PP} STATUS 1 = V_{PP} Error Detect, Operation Abort 0 = V_{PP} OK	The VPPS bit, unlike an A/D converter, does not provide continuous indication of V_{PP} level. The WSM interrogates V_{PP}’s level only after the Data Program or Erase command sequences have been entered, and informs the system if V_{PP} has not been switched on. VPPS is not guaranteed to report accurate feedback between V_{PPLK}(max) and V_{PPH1}(min), between V_{PPH1}(max) and V_{PPH2}(min) and above V_{PPH2}(max).
CSR.2–0 = RESERVED FOR FUTURE ENHANCEMENTS These bits are reserved for future use; mask them out when polling the CSR.	

4.6 Global Status Register

WSMS	OSS	DOS	DSS	QS	PBAS	PBS	PBSS
7	6	5	4	3	2	1	0

	NOTES:
GSR.7 = WRITE STATE MACHINE STATUS 1 = Ready 0 = Busy	[1] RY/BY# output or WSMS bit must be checked to determine completion of an operation (block lock, suspend, any RY/BY# reconfiguration, Upload Status Bits, erase or data program) before the appropriate Status bit (OSS or DOS) is checked for success.
GSR.6 = OPERATION SUSPEND STATUS 1 = Operation Suspended 0 = Operation in Progress/Completed	
GSR.5 = DEVICE OPERATION STATUS 1 = Operation Unsuccessful 0 = Operation Successful or Currently Running	
GSR.4 = DEVICE SLEEP STATUS 1 = Device in Sleep 0 = Device Not in Sleep	
MATRIX 5/4	
0 0 = Operation Successful or Currently Running	If operation currently running, then GSR.7 = 0.
0 1 = Device in Sleep Mode or Pending Sleep	If device pending sleep, then GSR.7 = 0.
1 0 = Operation Unsuccessful	
1 1 = Operation Unsuccessful or Aborted	Operation aborted: Unsuccessful due to Abort command.
GSR.3 = QUEUE STATUS 1 = Queue Full 0 = Queue Available	
GSR.2 = PAGE BUFFER AVAILABLE STATUS 1 = One or Two Page Buffers Available 0 = No Page Buffer Available	The device contains two Page Buffers.
GSR.1 = PAGE BUFFER STATUS 1 = Selected Page Buffer Ready 0 = Selected Page Buffer Busy	Selected Page Buffer is currently busy with WSM operation
GSR.0 = PAGE BUFFER SELECT STATUS 1 = Page Buffer 1 Selected 0 = Page Buffer 0 Selected	

NOTE:

1. When multiple operations are queued, checking BSR.7 only provides indication of completion for that particular block. GSR.7 provides indication when all queued operations are completed.

4.7 Block Status Register

BS	BLS	BOS	BOAS	QS	VPPS	VPPL	R
7	6	5	4	3	2	1	0

BSR.7 = BLOCK STATUS 1 = Ready 0 = Busy	**NOTES:** [1] RY/BY# output or BS bit must be checked to determine completion of an operation (block lock, suspend, erase or data program) before the appropriate Status bits (BOS, BLS) is checked for success.
BSR.6 = BLOCK LOCK STATUS 1 = Block Unlocked for Program/Erase 0 = Block Locked for Program/Erase	
BSR.5 = BLOCK OPERATION STATUS 1 = Operation Unsuccessful 0 = Operation Successful or Currently Running	
BSR.4 = BLOCK OPERATION ABORT STATUS 1 = Operation Aborted 0 = Operation Not Aborted	The BOAS bit will not be set until BSR.7 = 1.
MATRIX 5/4 0 0 = Operation Successful or Currently Running 0 1 = Not a Valid Combination 1 0 = Operation Unsuccessful 1 1 = Operation Aborted	Operation halted via Abort command.
BSR.3 = QUEUE STATUS 1 = Queue Full 0 = Queue Available	
BSR.2 = V_{PP} STATUS 1 = V_{PP} Error Detect, Operation Abort 0 = V_{PP} OK	
BSR.1 = V_{PP} LEVEL 1 = V_{PP} Detected at 5V ± 10% 0 = V_{PP} Detected at 12V ± 5%	BSR.1 is not guaranteed to report accurate feedback between the V_{PPH1} and V_{PPH2} voltage ranges. Programs and erases with V_{PP} between V_{PPLK}(max) and V_{PPH1}(min), between V_{PPH1}(max) and V_{PPH2}(min), and above V_{PPH2}(max) produce spurious results and should not be attempted. BSR.1 was a RESERVED bit on the 28F016SA.
BSR.0 = RESERVED FOR FUTURE ENHANCEMENTS This bits is reserved for future use; mask it out when polling the BSRs.	

NOTE:

1. When multiple operations are queued, checking BSR.7 only provides indication of completion or that particular block. GSR.7 provides indication when all queued operations are completed.

4.8 Device Configuration Code

R	R	R	R	R	RB2	RB1	RB0
7	6	5	4	3	2	1	0

DCC.2-DCC.0 = RY/BY# CONFIGURATION (RB2–RB0)
- 001 = Level Mode (Default)
- 010 = Pulse-On-Program
- 011 = Pulse-On-Erase
- 100 = RY/BY# Disabled
- 101 = Pulse-On-Program/Erase

NOTES:
Undocumented combinations of RB2–RB0 are reserved by Intel Corporation for future implementations and should not be used.

DCC.7–DCC.3 = RESERVED FOR FUTURE ENHANCEMENTS
These bits are reserved for future use; mask them out when reading the Device Configuration Code. Set these bits to “0” when writing the desired RY/BY# configuration to the device.

5.0 ELECTRICAL SPECIFICATIONS

NOTICE: This is a production datasheet. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

5.1 Absolute Maximum Ratings*

Temperature Under Bias ....0°C to +80°C

Storage Temperature ....–65°C to +125°C

**WARNING: Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only. Operation beyond the “Operating Conditions” is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

V_{CC} = 3.3V ± 0.3V Systems

Sym	Parameter	Notes	Min	Max	Units	Test Conditions
T_A	Operating Temperature, Commercial	1	0	70	°C	Ambient Temperature
V_{CC}	V_{CC} with Respect to GND	2	–0.2	7.0	V	
V_{PP}	V_{PP} Supply Voltage with Respect to GND	2,3	–0.2	14.0	V	
V	Voltage on Any Pin (except V_{CC},V_{PP}) with Respect to GND	2,5	–0.5	V_{CC} + 0.5	V	
I	Current into Any Non-Supply Pin	5		± 30	mA	
I_{OUT}	Output Short Circuit Current	4		100	mA	

V_{CC} = 5V ± 0.5V, 5V ± 0.25V Systems (6)

Sym	Parameter	Notes	Min	Max	Units	Test Conditions
T_A	Operating Temperature, Commercial	1	0	70	°C	Ambient Temperature
V_{CC}	V_{CC} with Respect to GND	2	–0.2	7.0	V	
V_{PP}	V_{PP} Supply Voltage with Respect to GND	2,3	–0.2	14.0	V	
V	Voltage on Any Pin (except V_{CC},V_{PP}) with Respect to GND	2,5	–2.0	7.0	V	
I	Current into Any Non-Supply Pin	5		± 30	mA	
I_{OUT}	Output Short Circuit Current	4		100	mA	

NOTES:

1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC voltage is –0.5V on input/output pins. During transitions, this level may undershoot to –2.0V for periods <20 ns. Maximum DC voltage on input/output pins is V_{CC} + 0.5V which, during transitions, may overshoot to V_{CC} + 2.0V for periods <20 ns.
3. Maximum DC voltage on V_{PP} may overshoot to +14.0V for periods <20 ns.
4. Output shorted for no more than one second. No more than one output shorted at a time.
5. This specification also applies to pins marked “NC.”
6. 5% V_{CC} specifications refer to the 28F016SV-065 and 28F016SV-070 in its high speed test configuration.

5.2 Capacitance

For a 3.3V ± 0.3V System:

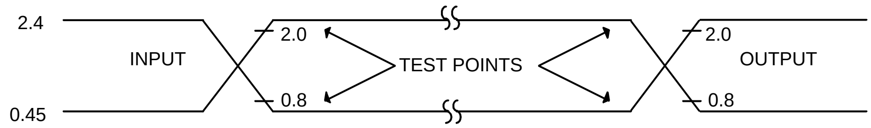
Sym	Parameter	Notes	Typ	Max	Units	Test Conditions
C_{IN}	Capacitance Looking into an Address/Control Pin	1	6	8	pF	T_A = +25°C, f = 1.0 MHz
C_{OUT}	Capacitance Looking into an Output Pin	1	8	12	pF	T_A = +25°C, f = 1.0 MHz
C_{LOAD}	Load Capacitance Driven by Outputs for Timing Specifications	1,2		50	pF	

For 5V ± 0.5V, 5V ± 0.25V System:

Sym	Parameter	Notes	Typ	Max	Units	Test Conditions
C_{IN}	Capacitance Looking into an Address/Control Pin	1	6	8	pF	T_A = +25°C, f = 1.0 MHz
C_{OUT}	Capacitance Looking into an Output Pin	1	8	12	pF	T_A = +25°C, f = 1.0 MHz
C_{LOAD}	Load Capacitance Driven by Outputs for Timing Specifications	1,2		100	pF	For V_{CC} = 5V ± 0.5V
				30	pF	For V_{CC} = 5V ± 0.25V

NOTE:

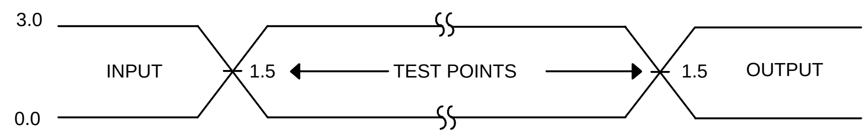
1. Sampled, not 100% tested. Guaranteed by design.
2. To obtain iBIS models for the 28F016SV, please contact your local Intel/Distribution Sales Office.



AC test inputs are driven at V_{OH} (2.4 VTTL) for a Logic "1" and V_{OL} (0.45 VTTL) for a Logic "0." Input timing begins at V_{IH} (2.0 VTTL) and V_{IL} (0.8 VTTL). Output timing ends at V_{IH} and V_{IL}. Input rise and fall times (10% to 90%) <10 ns.

0528_07

Figure 7. Transient Input/Output Reference Waveform for V_{CC} = 5V ± 10% (Standard Testing Configuration)(1)



AC test inputs are driven at 3.0V for a Logic "1" and 0.0V for a Logic "0." Input timing begins, and output timing ends, at 1.5V. Input rise and fall times (10% to 90%) <10 ns.

0528_08

Figure 8. Transient Input/Output Reference Waveform for V_{CC} = 3.3V ± 0.3V and V_{CC} = 5V ± 5% (High Speed Testing Configuration)(2)

NOTES:

1. Testing characteristics for 28F016SV-070 (Standard Testing Configuration) and 28F016SV-080.
2. Testing characteristics for 28F016SV-065/28F016SV-075 and 28F016SV-70 (High Speed Testing Configuration)/ 28F016SV-120.

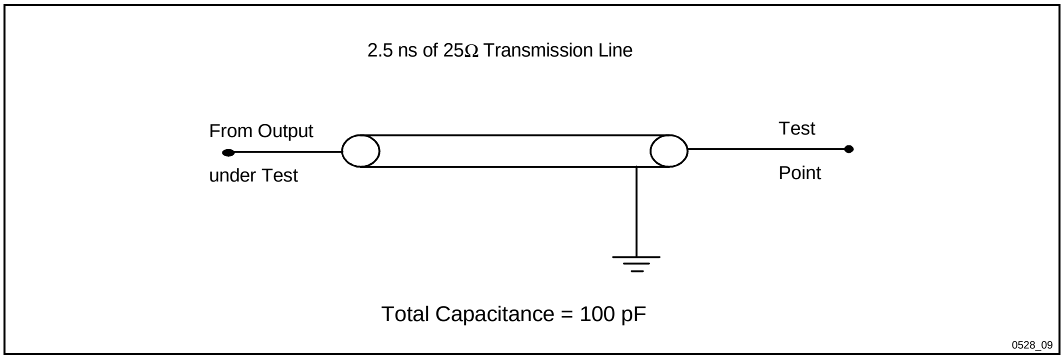


Figure 9. Transient Equivalent Testing Load Circuit (28F016SV-070/-080 at V_{CC} = 5V ± 10%)

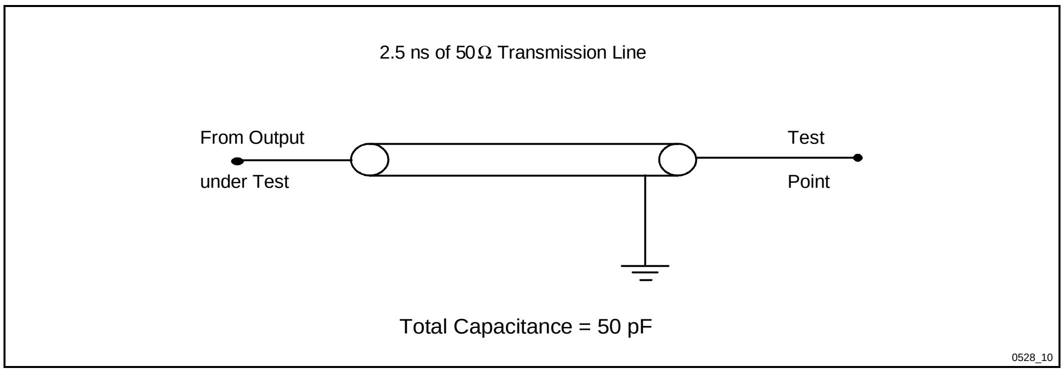


Figure 10. Transient Equivalent Testing Load Circuit (28F016SV-075/-120 at V_{CC} = 3.3V ± 0.3V)

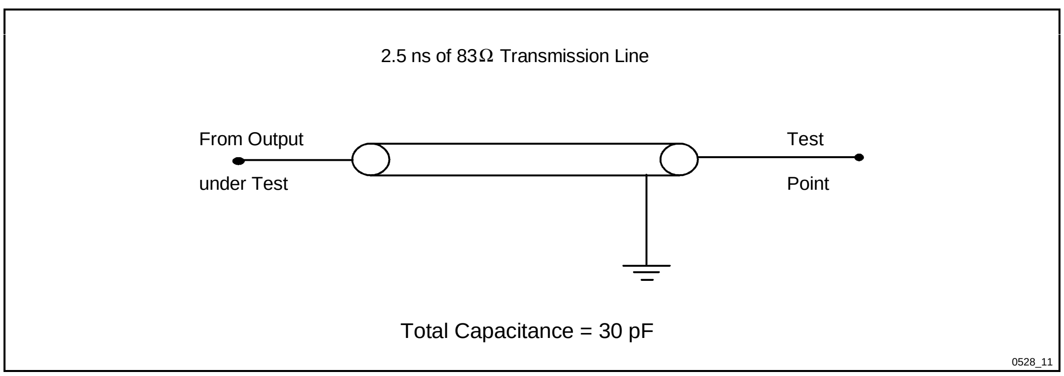


Figure 11. High Speed Transient Equivalent Testing Load Circuit (28F016SV-065/-070 at V_{CC} = 5V ± 5%)

5.3 DC Characteristics

V_{CC} = 3.3V ± 10%V, T_A = 0°C to +70°C, –40°C to +70°C
3/5# = Pin Set High for 3.3V Operations

Sym	Parameter	Temp Notes	Commercial Min	Commercial Typ	Commercial Max	Extended Min	Extended Typ	Extended Max	Units	Test Conditions
I_{LI}	Input Load Current	1			± 1			± 1	µA	V_{CC} = V_{CC} Max V_{IN} = V_{CC} or GND
I_{LO}	Output Leakage Current	1			± 10			± 10	µA	V_{CC} = V_{CC} Max V_{OUT} = V_{CC} or GND
I_{CCS}	V_{CC} Standby Current	1,5		70	130		70	130	µA	V_{CC} = V_{CC} Max CE_0#, CE_1#, RP# = V_{CC} ± 0.2V BYTE#, WP#, 3/5# = V_{CC} ±0.2V or GND ± 0.2V
				1	4		1	4	mA	V_{CC} = V_{CC} Max CE_0#, CE_1#, RP# = V_{IH} BYTE#, WP#, 3/5# = V_{IH} or V_{IL}
I_{CCD}	V_{CC} Deep Power-Down Current	1		2	10		5	15	µA	RP# = GND ± 0.2V BYTE# = V_{CC} ± 0.2V or GND ± 0.2V
$I_{CCR}1$	V_{CC} Read Current	1,4,5		40	50		40	55	mA	V_{CC} = V_{CC} Max CMOS: CE_0#, CE_1# = GND ± 0.2V, BYTE# = GND ± 0.2V or V_{CC} ± 0.2V, Inputs = GND ± 0.2V or V_{CC} ± 0.2V TTL: CE_0#, CE_1# = V_{IL}, BYTE# = V_{IL} or $V_{IH.}$ Inputs = V_{IL} or V_{IH} f = 8 MHz, I_{OUT} = 0 mA

5.3 DC Characteristics (Continued)

V_{CC} = 3.3V ± 10%V, T_A = 0°C to +70°C, –40°C to +70°C
3/5# = Pin Set High for 3.3V Operations

Sym	Parameter	Temp Notes	Commercial Min	Commercial Typ	Commercial Max	Extended Min	Extended Typ	Extended Max	Units	Test Conditions
$I_{CCR}2$	V_{CC} Read Current	1,4, 5,6		20	30		20	35	mA	$V_{CC} = V_{CC}$ Max CMOS: CE_0#, CE_1# = GND ± 0.2V, BYTE# = GND ± 0.2V or V_{CC} ± 0.2V, Inputs = GND ± 0.2V or V_{CC} ± 0.2V TTL: CE_0#, CE_1# = V_{IL}, BYTE# = V_{IL} or $V_{IH,}$ Inputs = V_{IL} or V_{IH} f = 4 MHz, I_{OUT} = 0 mA
I_{CCW}	V_{CC} Program Current for Word or Byte	1,6		8	12		8	12	mA	V_{PP} = 12V ± 5% Program in Progress
				8	17		8	17	mA	V_{PP} = 5V ± 10% Program in Progress
I_{CCE}	V_{CC} Block Erase Current	1,6		6	12		6	12	mA	V_{PP} = 12V ± 5% Block Erase in Progress
				9	17		9	17	mA	V_{PP} = 5V ± 10% Block Erase in Progress
I_{CCES}	V_{CC} Erase Suspend Current	1,2		1	4		1	4	mA	CE_0#, CE_1# = V_{IH} Block Erase Suspended
I_{PPS}	V_{PP} Standby/	1		± 1	± 10		± 3	± 10	µA	$V_{PP} \leq V_{CC}$
I_{PPR}	Read Current			30	200		70	200	µA	$V_{PP} > V_{CC}$
I_{PPD}	V_{PP} Deep Power-Down Current	1		0.2	5		0.2	5	µA	RP# = GND ± 0.2V

5.3 DC Characteristics (Continued)

V_{CC} = 3.3V ± 10%V, T_A = 0°C to +70°C, –40°C to +70°C
3/5# = Pin Set High for 3.3V Operations

Sym	Parameter	Temp Notes	Commercial Min	Commercial Typ	Commercial Max	Extended Min	Extended Typ	Extended Max	Units	Test Conditions
I_{PPW}	V_{PP} Program Current for Word or Byte	1,6		10	15		10	15	mA	V_{PP} = 12V ± 5% Program in Progress
				15	25		15	25	mA	V_{PP} = 5V ± 10% Program in Progress
I_{PPE}	V_{PP} Erase Current	1,6		4	10		4	10	mA	V_{PP} = 12V ± 5% Block Erase in Progress
				14	20		14	20	mA	V_{PP} = 5V ± 10% Block Erase in Progress
I_{PPES}	V_{PP} Erase Suspend Current	1		30	200		70	200	µA	V_{PP} = V_{PPH1} or V_{PPH2} Block Erase Suspended
V_{IL}	Input Low Voltage	6	–0.3		0.8			0.8	V	
V_{IH}	Input High Voltage	6	2.0		V_{CC} + 0.3			V_{CC} + 0.3	V	
V_{OL}	Output Low Voltage	6			0.4			0.4	V	V_{CC} = V_{CC} Min and I_{OL} = 4 mA

5.3 DC Characteristics (Continued)

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C, –40°C to +85°C

3/5# = Pin Set High for 3.3V Operations

Sym	Parameter	Temp Notes	Comm/Ext Min	Typ	Max	Units	Test Conditions
$V_{OH}1$	Output High Voltage	6	2.4			V	V_{CC} = V_{CC} Min I_{OH} = –2.0 mA
$V_{OH}2$		6	V_{CC}– 0.2			V	V_{CC} = V_{CC} Min I_{OH} = –100 µA
V_{PPLK}	V_{PP} Program/Erase Lock Voltage	3,6	0.0		1.5	V	
V_{PPH1}	V_{PP} during Program/Erase Operations	3	4.5	5.0	5.5	V	
V_{PPH2}	V_{PP} during Program/Erase Operations	3	11.4	12.0	12.6	V	
V_{LKO}	V_{CC} Program/Erase Lock Voltage		2.0			V	

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 3.3V, V_{PP} = 12V or 5V, T = +25°C. These currents are valid for all product versions (package and speeds).
2. I_{CCES} is specified with the device de-selected. If the device is read while in erase suspend mode, current draw is the sum of I_{CCES} and I_{CCR}.
3. Block erases, word/byte programs and lock block operations are inhibited when $V_{PP} \leq V_{PPLK}$ and not guaranteed in the ranges between V_{PPLK}(max) and V_{PPH1}(min), between V_{PPH1} (max) and V_{PPH2}(min) and above V_{PPH2}(max).
4. Automatic Power Savings (APS) reduces I_{CCR} to 3.0 mA typical in static operation.
5. CMOS Inputs are either V_{CC} ± 0.2V or GND ± 0.2V. TTL Inputs are either V_{IL} or V_{IH}.
6. Sampled, but not 100% tested. Guaranteed by design.

5.4 DC Characteristics

V_{CC} = 5V ± 0.5V, 5V ± 0.25V, T_A = 0°C to +70°C, –40°C to +85°C
3/5# = Pin Set Low for 5V Operations

Sym	Parameter	Temp	Commercial			Extended			Units	Test Conditions
		Notes	Min	Typ	Max	Min	Typ	Max		
I_{LI}	Input Load Current	1			± 1			± 1	µA	V_{CC} = V_{CC} Max V_{IN} = V_{CC} or GND
I_{LO}	Output Leakage Current	1			± 10			± 10	µA	V_{CC} = V_{CC} Max V_{OUT} = V_{CC} or GND
I_{CCS}	V_{CC} Standby Current	1,5		70	130		70	130	µA	V_{CC} = V_{CC} Max CE_0#, CE_1#, RP# = V_{CC} ± 0.2V BYTE#, WP#, 3/5# = V_{CC} ± 0.2V or GND ± 0.2V
				2	4		2	4	mA	V_{CC} = V_{CC} Max, CE_0#, CE_1#, RP# = V_{IH} BYTE#, WP#, 3/5# = V_{IH} or V_{IL}
I_{CCD}	V_{CC} Deep Power-Down Current	1		2	10		5	15	µA	RP# = GND ± 0.2V BYTE# = V_{CC} ± 0.2V or GND ± 0.2V
I_{CCR}1	V_{CC} Read Current	1,4,5		75	95		75	105	mA	V_{CC} = V_{CC} Max CMOS: CE_0#, CE_1# = GND ± 0.2V, BYTE# = GND ± 0.2V or V_{CC} ± 0.2V, Inputs = GND ± 0.2V or, V_{CC} ± 0.2V TTL: CE_0#, CE_1# = V_{IL}, BYTE# = V_{IL} or $V_{IH,}$ Inputs = V_{IL} or V_{IH} f = 10 MHz, I_{OUT} = 0 mA

5.4 DC Characteristics (Continued)

V_{CC} = 5V ± 0.5V, 5V ± 0.25V, T_A = 0°C to +70°C, –40°C to +85°C
3/5# = Pin Set Low for 5V Operations

Sym	Parameter	Temp Notes	Commercial Min	Commercial Typ	Commercial Max	Extended Min	Extended Typ	Extended Max	Units	Test Conditions
I_{CCR}2	V_{CC} Read Current	1,4,5,6		45	55		45	60	mA	V_{CC} = V_{CC} Max CMOS: CE_0#, CE_1# = GND ± 0.2V, BYTE# = GND ± 0.2V or V_{CC} ± 0.2V, Inputs = GND ± 0.2V or V_{CC} ± 0.2V TTL: CE_0#, CE_1# = V_{IL}, BYTE# = V_{IL} or V_{IH}, Inputs = V_{IL} or V_{IH} f = 5 MHz, I_{OUT} = 0 mA
I_{CCW}	V_{CC} Program Current for Word or Byte	1,6		25	35		25	35	mA	V_{PP} = 12V ± 5% Program in Progress
				25	40		25	40	mA	V_{PP} = 5V ± 10% Program in Progress
I_{CCE}	V_{CC} Block Erase Current	1,6		18	25		18	25	mA	V_{PP} = 12V ± 5% Block Erase in Progress
				20	30		20	30	mA	V_{PP} = 5V ± 10% Block Erase in Progress
I_{CCES}	V_{CC} Erase Suspend Current	1,2		2	4		2	4	mA	CE_0#, CE_1# = V_{IH} Block Erase Suspended
I_{PPS}	V_{PP} Standby /Read	1		± 1	± 10		± 3	± 10	µA	$V_{PP} \le V_{CC}$
I_{PPR}	Current			30	200		70	200	µA	$V_{PP} > V_{CC}$
I_{PPD}	V_{PP} Deep Power-Down Current	1		0.2	5		0.2	5	µA	RP# = GND ± 0.2V

5.4 DC Characteristics (Continued)

V_{CC} = 5V ± 0.5V, 5V ± 0.25V, T_A = 0°C to +70°C, –40°C to +85°C
3/5# = Pin Set Low for 5V Operations

Sym	Parameter	Temp Notes	Commercial Min	Commercial Typ	Commercial Max	Extended Min	Extended Typ	Extended Max	Units	Test Conditions
I_{PPW}	V_{PP} Program Current for Word or Byte	1,6		7	12		7	12	mA	V_{PP} = 12V ± 5% Program in Progress
				17	22		17	22	mA	V_{PP} = 5V ± 10% Program in Progress
I_{PPE}	V_{PP} Block Erase Current	1,6		5	10		5	10	mA	V_{PP} = 12V ± 5% Block Erase in Progress
				16	20		16	20	mA	V_{PP} = 5V ± 10% Block Erase in Progress
I_{PPES}	V_{PP} Erase Suspend Current	1		30	200		30	200	µA	V_{PP} = V_{PPH1} or V_{PPH2} Block Erase Suspended
V_{IL}	Input Low Voltage	6	–0.5		0.8			0.8	V	
V_{IH}	Input High Voltage	6	2.0		V_{CC}+ 0.5			V_{CC}+ 0.5	V	

5.4 DC Characteristics (Continued)

V_{CC} = 5V ± 0.5V, 5V ± 0.25V, T_A = 0°C to +70°C, –40°C to +85°C
3/5# = Pin Set Low for 5V Operations

Sym	Parameter	Temp Notes	Comm/Extended Min	Typ	Max	Units	Test Conditions
V_{OL}	Output Low Voltage	6			0.45	V	$V_{CC} = V_{CC}$ Min I_{OL} = 5.8 mA
$V_{OH}1$	Output High Voltage	6	0.85 V_{CC}			V	$V_{CC} = V_{CC}$ Min I_{OH} = –2.5 mA
$V_{OH}2$		6	V_{CC} – 0.4				$V_{CC} = V_{CC}$ Min I_{OH} = –100 µA
V_{PPLK}	V_{PP} Program/Erase Lock Voltage	3,6	0.0		1.5	V	
V_{PPH1}	V_{PP} during Program/Erase Operations		4.5	5.0	5.5	V	
V_{PPH2}	V_{PP} during Program/Erase Operations		11.4	12.0	12.6	V	
V_{LKO}	V_{CC} Program/Erase Lock Voltage		2.0			V	

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 5V, V_{PP} = 12V or 5V, T = 25°C. These currents are valid for all product versions (package and speeds) and are specified for a CMOS rise/fall time (10% to 90%) of <5 ns and a TTL rise/fall time of <10 ns.
2. I_{CCES} is specified with the device de-selected. If the device is read while in erase suspend mode, current draw is the sum of I_{CCES} and I_{CCR}.
3. Block erases, word/byte programs and lock block operations are inhibited when $V_{PP} \leq V_{PPLK}$ and not guaranteed in the ranges between V_{PPLK}(max) and V_{PPH1}(min), between V_{PPH1} (max) and V_{PPH2}(min) and above V_{PPH2}(max).
4. Automatic Power Saving (APS) reduces I_{CCR} to 1 mA typical in Static operation.
5. CMOS Inputs are either V_{CC} ± 0.2V or GND ± 0.2V. TTL Inputs are either V_{IL} or V_{IH}.
6. Sampled, not 100% tested. Guaranteed by design.

5.5 Timing Nomenclature

All 3.3V system timings are measured from where signals cross 1.5V.

For 5V systems use the standard JEDEC cross point definitions (standard testing) or from where signals cross 1.5V (high speed testing).

Each timing parameter consists of 5 characters. Some common examples are defined below:

t_{CE} t_{ELQV} time(t) from CE# (E) going low (L) to the outputs (Q) becoming valid (V)

t_{OE} t_{GLQV} time(t) from OE # (G) going low (L) to the outputs (Q) becoming valid (V)

t_{ACC} t_{AVQV} time(t) from address (A) valid (V) to the outputs (Q) becoming valid (V)

t_{AS} t_{AVWH} time(t) from address (A) valid (V) to WE# (W) going high (H)

t_{DH} t_{WHDX} time(t) from WE# (W) going high (H) to when the data (D) can become undefined (X)

	Pin Characters		Pin States
A	Address Inputs	H	High
D	Data Inputs	L	Low
Q	Data Outputs	V	Valid
E	CE# (Chip Enable)	X	Driven, but Not Necessarily Valid
F	BYTE# (Byte Enable)	Z	High Impedance
G	OE# (Output Enable)		
W	WE# (Write Enable)		
P	RP# (Deep Power-Down Pin)		
R	RY/BY# (Ready Busy)		
V	Any Voltage Level		
Y	3/5# Pin		
5V	V_{CC} at 4.5V Minimum		
3V	V_{CC} at 3.0V Minimum		

5.6 AC Characteristics—Read Only Operations(1)

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C, –40°C to +85°C

Sym	Parameter	Temp	Commercial		Extended		Commercial		Units
		Speed	–75		–100		–120		
		Notes	Min	Max	Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time		75 85(10)		100		120		ns
t_{AVQV}	Address to Output Delay			75 85(10)		100		120	ns
t_{ELQV}	CE# to Output Delay	2,8		75 85(10)		100		120	ns
t_{PHQV}	RP# High to Output Delay			480		620		620	ns
t_{GLQV}	OE# to Output Delay	2		40		45		45	ns
t_{ELQX}	CE# to Output in Low Z	3,8	0		0		0		ns
t_{EHQZ}	CE# to Output in High Z	3,8		30		50		50	ns
t_{GLQX}	OE# to Output in Low Z	3	0		0		0		ns
t_{GHQZ}	OE# to Output in High Z	3		20		20		20	ns
t_{OH}	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3,8	0		0		0		ns
t_{FLQV} t_{FHQV}	BYTE# to Output Delay	3		75 85(10)			100	120	ns
t_{FLQZ}	BYTE# Low to Output in High Z	3		30			30	30	ns
t_{ELFL} t_{ELFH}	CE# Low to BYTE# High or Low	3,8		5			5	5	ns

Extended Status Register Reads

t_{AVEL}	Address Setup to CE# Going Low	3,4, 8,9	0		0		0		ns
t_{AVGL}	Address Setup to OE# Going Low	3,4,9	0		0		0		ns

5.6 AC Characteristics—Read Only Operations(1) (Continued)

V_{CC} = 5V ± 0.5V, 5V ± 0.25V, T_A = 0°C to +70°C, –40°C to +85°C

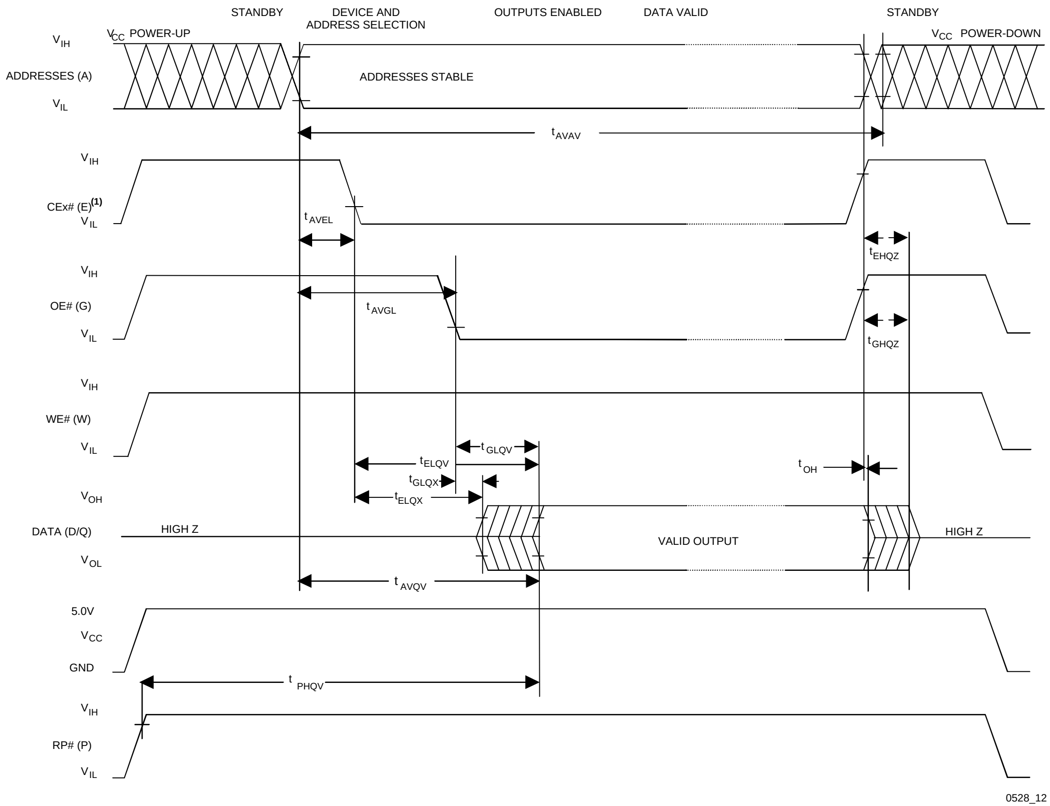
Sym	Parameter	Temp	Commercial				Comm/Ext		Units
		Speed	–65		–70		–80		
		V_{CC}	5V ± 5%V		5V ± 10%		5V ± 10%		
		Load	30 pF		50 pF		50 pF		
		Notes	Min	Max	Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time		65		70		80		ns
t_{AVQV}	Address to Output Delay			65		70		80	ns
t_{ELQV}	CE# to Output Delay	2,8		65		70		80	ns
t_{PHQV}	RP# to Output Delay			400		480(6) 400(7)		480	ns
t_{GLQV}	OE# to Output Delay	2		30		30(6) 35(7)		35	ns
t_{ELQX}	CE# to Output in Low Z	3,8	0		0		0		ns
t_{EHQZ}	CE# to Output in High Z	3,8		25		25		30	ns
t_{GLQX}	OE# to Output in Low Z	3	0		0		0		ns
t_{GHQZ}	OE# to Output in High Z	3		15		15		20	ns
t_{OH}	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3,8	0		0		0		ns
t_{FLQV} t_{FHQV}	BYTE# to Output Delay	3		65		70		80	ns
t_{FLQZ}	BYTE# Low to Output in High Z	3		25		25		30	ns
t_{ELFL} t_{ELFH}	CE# Low to BYTE# High or Low	3,8		5		5		5	ns

Extended Status Register Reads

t_{AVEL}	Address Setup to CE# Going Low	3,4,8,9	0		0		0		ns
t_{AVGL}	Address Setup to OE# Going Low	3,4,9	0		0		0		ns

NOTES:

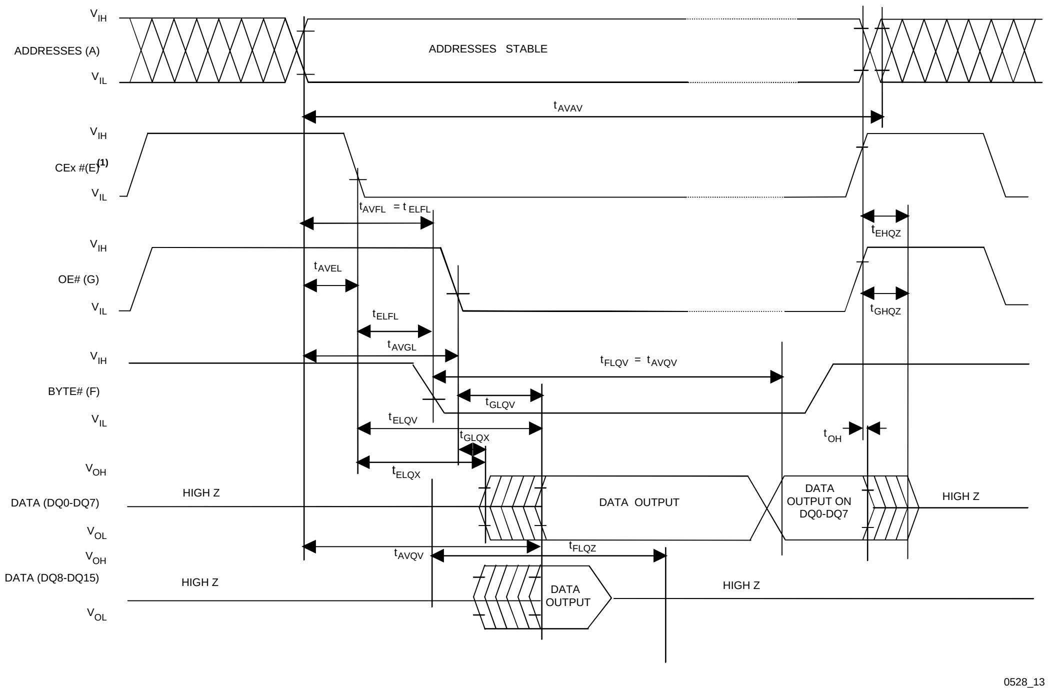
1. See AC Input/Output Reference Waveforms for timing measurements, Figures 7 and 8.
2. OE# may be delayed up to t_{ELQV}-t_{GLQV} after the falling edge of CE#, without impacting t_{ELQV}.
3. Sampled, not 100% tested. Guaranteed by design
4. This timing parameter is used to latch the correct BSR data onto the outputs.
5. Device speeds are defined as:
   65/70 ns at V_{CC} = 5V equivalent to
   75 ns at V_{CC} = 3.3V
   70/80 ns at V_{CC} = 5V equivalent to
   120 ns at V_{CC} = 3.3V
6. See the high speed AC Input/Output Reference Waveforms and AC Testing Load Circuit.
7. See the standard AC Input/Output Reference Waveforms and AC Testing Load Circuit.
8. CE_X# is defined as the latter of CE_0# or CE_1# going low, or the first of CE_0# or CE_1# going high.
9. The address setup requirement for Extended Status Register reads must only be met referenced to the falling edge of the last control signal to become active (CE_0#, CE_1# or OE#). For example, if CE_0# and CE_1# are activated prior to OE# for an Extended Status Register read, specification t_{AVGL} must be met. On the other hand, if either CE_0# or CE_1# (or both) are activated after OE#, specification t_{AVEL} must be referenced.
10. Page Buffer Reads only.



NOTE:

CE_X # is defined as the latter of CE_0# or CE_1# going low, or the first of CE_0# or CE_1# going high.

Figure 12. Read Timing Waveforms



NOTE:
CE_X # is defined as the latter of CE_0# or CE_1# going low, or the first of CE_0# or CE_1# going high.

Figure 13. BYTE# Timing Waveforms

5.7 Power-Up and Reset Timings

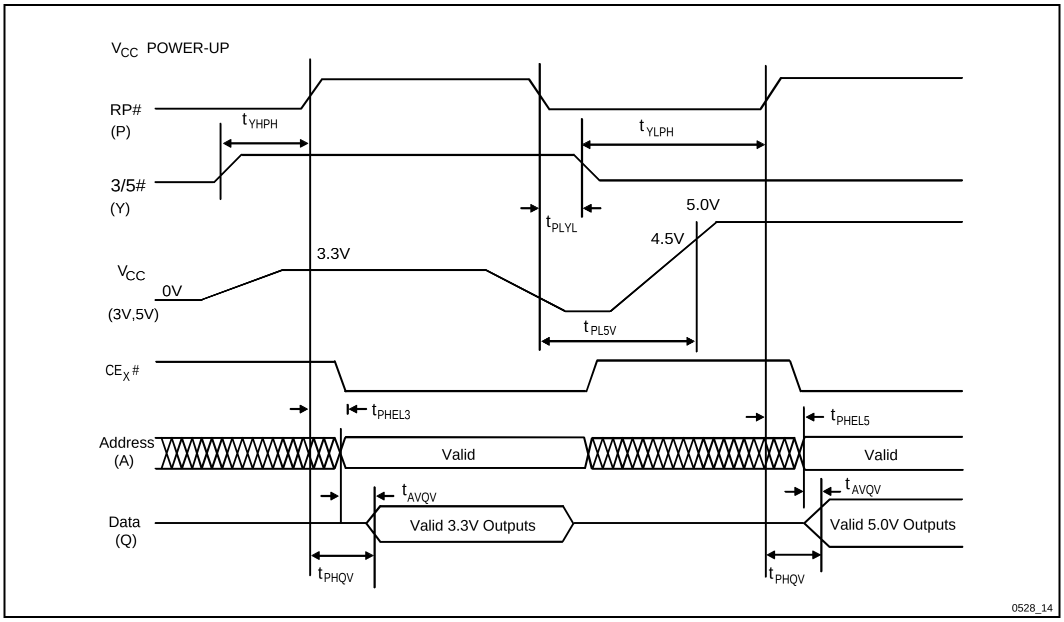


Figure 14. V_{CC} Power-Up and RP# Reset Waveforms

Symbol	Parameter	Notes	Min	Max	Unit
t_{PLYL} t_{PLYH}	RP# Low to 3/5# Low (High)		0		µs
t_{YLPH} t_{YHPH}	3/5# Low (High) to RP# High	1	2		µs
t_{PL5V} t_{PL3V}	RP# Low to V_{CC} at 4.5V minimum (to V_{CC} at 3.0V min or 3.6V max)	2	0		µs
t_{PHEL3}	RP# High to CE# Low (3.3V V_{CC})	1	405		ns
t_{PHEL5}	RP# High to CE# Low (5V V_{CC})	1	330		ns
t_{AVQV}	Address Valid to Data Valid for V_{CC} = 5V ± 10%	3		70	ns
t_{PHQV}	RP# High to Data Valid for V_{CC} = 5V ± 10%	3		400	ns

NOTES:

CE_0#, CE_1# and OE# are switched low after Power-Up.

1. The t_{YLPH} and/or t_{YHPH} times must be strictly followed to guarantee all other read and program specifications for the 28F016SV.
2. The power supply may start to switch concurrently with RP# going low.
3. The address access time and RP# high to data valid time are shown for 5V V_{CC} operation of the 28F016SV-070 (Standard Test Configuration). Refer to the AC Characteristics-Read Only Operations for 3.3V V_{CC} and 5V V_{CC} (High Speed Test Configuration) values.

5.8 AC Characteristics for WE#—Controlled Command Write Operations[1]

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C; –40°C to +85°C

Sym	Parameter	Temp	Commercial			Extended			Commercial			Unit
		Speed	–75			–100			–120			
		Notes	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{AVAV}	Write Cycle Time		75			100			120			ns
t_{VPWH}1,2	V_{PP} Setup to WE# Going High	3	100			100			100			ns
t_{PHEL}	RP# Setup to CE# Going Low	3,7	480			480			480			ns
t_{ELWL}	CE# Setup to WE# Going Low	3,7	0,10[12]			10			10			ns
t_{AVWH}	Address Setup to WE# Going High	2,6	60			70			75			ns
t_{DVWH}	Data Setup to WE# Going High	2,6	60			70			75			ns
t_{WLWH}	WE# Pulse Width		60			70			75			ns
t_{WHDX}	Data Hold from WE# High	2	5			10			10			ns
t_{WHAX}	Address Hold from WE# High	2	5			10			10			ns
t_{WHEH}	CE# Hold from WE# High	3,7	5			10			10			ns
t_{WHWL}	WE# Pulse Width High		15			30			45			ns
t_{GHWL}	Read Recovery before Write	3	0			0			0			ns
t_{WHRL}	WE# High to RY/BY# Going Low	3			100			100			100	ns
t_{RHPL}	RP# Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High	3	0			0			0			ns
t_{PHWL}	RP# High Recovery to WE# Going Low	3	0.480			1			1			µs
t_{WHGL}	Write Recovery before Read		55			75			95			ns
t_{QVVL}1,2	V_{PP} Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High	3	0			0			0			µs

5.8 AC Characteristics for WE#—Controlled Command Write Operations(1)
(Continued)

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C; –40°C to +85°C

Sym	Parameter	Temp	Commercial			Extended			Commercial			Unit
		Speed	–75			–100			–120			
		Notes	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{WHQV}1$	Duration of Program Operation	3,4,5, 11	5	9	TBD	5	9	TBD	5	9	TBD	µs
$t_{WHQV}2$	Duration of Block Erase Operation	3,4	0.3	0.8	10	0.3	0.8	10	0.3	0.8	10	sec

5.8 AC Characteristics for WE#—Controlled Command Write Operations(1)

(Continued)

V_{CC} = 5V ± 0.5V, 5V ± 0.25V, T_A = 0°C to +70°C, –40°C to +85°C

Sym	Parameter	Temp	Commercial						Extended			Unit
		Speed	–65			–70			–80			
		V_{CC}	5V ± 5%			5V ± 10%			5V ± 10%			
		Load	30 pF			50 pF			50 pF			
		Notes	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{AVAV}	Write Cycle Time		65			70			80			ns
$t_{VPWH}1$ $t_{VPWH}2$	V_{PP} Setup to WE# Going High	3	100			100			100			ns
t_{PHEL}	RP# Setup to CE# Going Low	3,7	300			480(9) 300(10)			480			ns
t_{ELWL}	CE# Setup to WE# Going Low	3,7	0			0			0			ns
t_{AVWH}	Address Setup to WE# Going High	2,6	40			50(9) 40(10)			50			ns
t_{DVWH}	Data Setup to WE# Going High	2,6	40			50(9) 40(10)			50			ns
t_{WLWH}	WE# Pulse Width		40			40(9) 45(10)			50			ns
t_{WHDX}	Data Hold from WE# High	2	0			0			0			ns
t_{WHAX}	Address Hold from WE# High	2	5			10			10			ns
t_{WHEH}	CE# Hold from WE# High	3,7	5			10(9) 5(10)			10			ns
t_{WHWL}	WE# Pulse Width High		15			30(9) 15(10)			30			ns
t_{GHWL}	Read Recovery before Write	3	0			0			0			ns
t_{WHRL}	WE# High to RY/BY# Going Low	3			100			100			100	ns
t_{RHPL}	RP# Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High	3	0			0			0			ns

5.8 AC Characteristics for WE#—Controlled Command Write Operations(1)

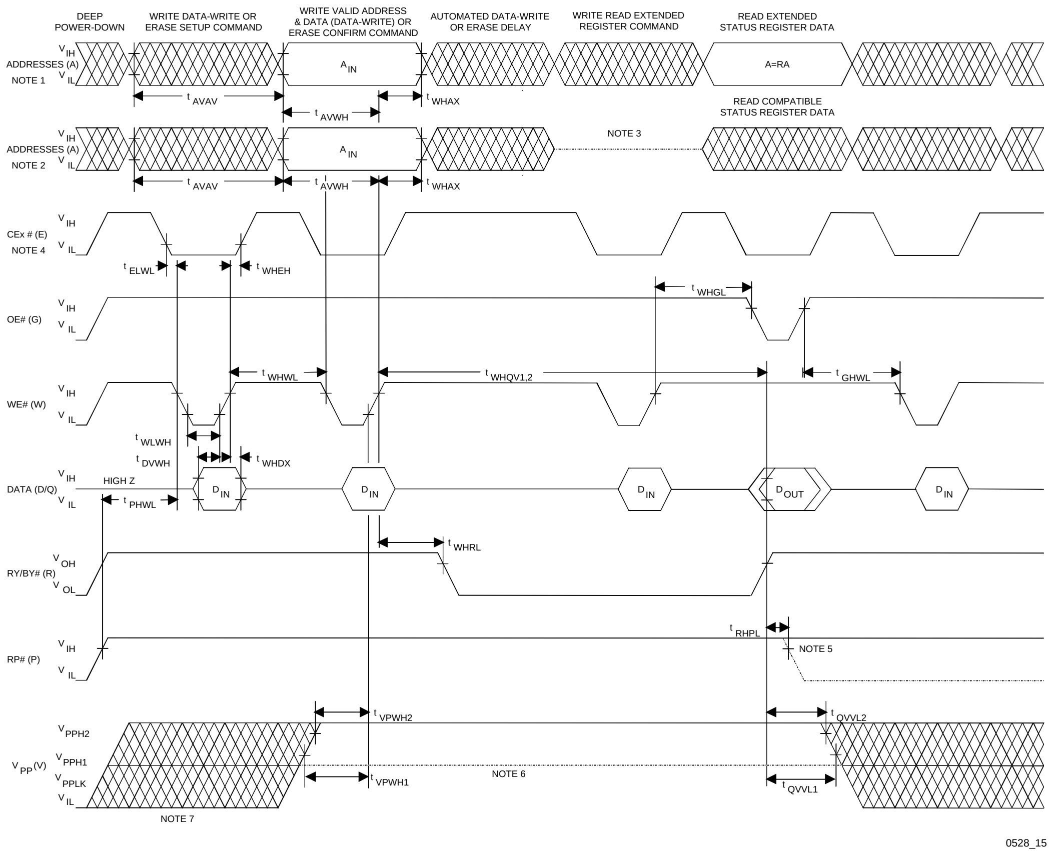
(Continued)

V_{CC} = 5V ± 0.5V, 5V ± 0.25V, T_A = 0°C to +70°C, –40°C to +85°C

Sym	Parameter	Temp	Commercial						Extended			Unit
		Speed	–65			–70			–80			
		V_{CC}	5V ± 5%			5V ± 10%			5V ± 10%			
		Load	30 pF			50 pF			50 pF			
		Notes	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PHWL}	RP# High Recovery to WE# Going Low	3	0.300			1(9) 0.300(10)			1			µs
t_{WHGL}	Write Recovery before Read		55			60			65			ns
$t_{QVVL}1$ $t_{QVVL}2$	V_{PP} Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High	3	0			0			0			µs
$t_{WHQV}1$	Duration of Program Operation	3,4,5, 11	4.5	6	TBD	4.5	6	TBD	4.5	6	TBD	µs
$t_{WHQV}2$	Duration of Block Erase Operation	3,4	0.3	0.6	10	0.3	0.6	10	0.3	0.6	10	sec

NOTES:

1. Read timings during program and erase are the same as for normal read.
2. Refer to command definition tables for valid address and data values.
3. Sampled, not 100% tested. Guaranteed by design.
4. Program/erase durations are measured to valid Status Register (CSR) Data. V_{PP} = 12V ± 0.6V.
5. Word/byte program operations are typically performed with 1 Programming Pulse.
6. Address and Data are latched on the rising edge of WE# for all command write operations.
7. CE_X# is defined as the latter of CE_0# or CE_1# going low, or the first of CE_0# or CE_1# going high.
8. Device speeds are defined as:
   65/70 ns at V_{CC} = 5V equivalent to
   75 ns at V_{CC} = 3.3V
   70/80 ns at V_{CC} = 5V equivalent to
   120 ns at V_{CC} = 3.3V
9. See the high speed AC Input/Output Reference Waveforms and AC Testing Load Circuit.
10. See the standard AC Input/Output Reference Waveforms and AC Testing Load Circuit.
11. The TBD information will be available in a technical paper. Please contact Intel's Application Hotline or your local sales office for more information.
12. Page Buffer Programs only.



NOTES:

1. This address string depicts data program/erase cycles with corresponding verification via ESRD.
2. This address string depicts data program/erase cycles with corresponding verification via CSRD.
3. This cycle is invalid when using CSRD for verification during data program/erase operations.
4. CE_X# is defined as the latter of CE_0# or CE_1# going low or the first of CE_0# or CE_1# going high.
5. RP# low transition is only to show t_{RHPL}; not valid for above read and program cycles.
6. V_{PP} voltage during program/erase operations valid at both 12V and 5V.
7. V_{PP} voltage equal to or below V_{PPLK} provides complete flash memory array protection.

Figure 15. AC Waveforms for Command Write Operations

5.9 AC Characteristics for CE#—Controlled Command Write Operations[1]

V_{CC} = 3.3V ± 0.3V, T_A = 0°C +70°C, –40°C +85°C

Sym	Parameter	Temp	Commercial			Extended			Commercial			Unit
		Speed	–80			–100			–120			
		Notes	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{AVAV}	Write Cycle Time		80			100			120			ns
t_{VPEH}1,2	V_{PP} Setup to CE# Going High	3,7	100			100			100			ns
t_{PHWL}	RP# Setup to WE# Going Low	3	480			480			480			ns
t_{WLEL}	WE# Setup to CE# Going Low	3,7	0			0			0			ns
t_{AVEH}	Address Setup to CE# Going High	2,6,7	60			70			75			ns
t_{DVEH}	Data Setup to CE# Going High	2,6,7	60			70			75			ns
t_{ELEH}	CE# Pulse Width	7	65			70			75			ns
t_{EHDX}	Data Hold from CE# High	2,7	10			10			10			ns
t_{EHAX}	Address Hold from CE# High	2,7	10			30			10			ns
t_{EHWH}	WE# hold from CE# High	3	5			0			10			ns
t_{EHEL}	CE# Pulse Width High	7	15					100	45			ns
t_{GHEL}	Read Recovery before Write	3	0			0			0			ns
t_{EHRL}	CE# High to RY/BY# Going Low	3,7			100	1					100	ns
t_{RHPL}	RP# Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High	3	0			75			0			ns
t_{PHEL}	RP# High Recovery to CE# Going Low	3,7	0.480			0			1			µs
t_{EHGL}	Write Recovery before Read		55						95			ns

5.9 AC Characteristics for CE#—Controlled Command Write Operations(1)

(Continued)

V_{CC} = 3.3V ± 0.3V, T_A = 0°C +70°C, –40°C +85°C

Sym	Parameter	Temp	Commercial			Extended			Commercial			Unit
		Speed	–80			–100			–120			
		Notes	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{QVVL}1,2	V_{PP} Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High	3	0						0			µs
t_{EHQV}1	Duration of Program Operation	3,4,5,11	5	9	TBD	5	9	TBD	5	9	TBD	µs
t_{EHQV}2	Duration of Block Erase Operation	3,4	0.3	0.8	10	0.3	0.8	10	0.3	0.8	10	sec

5.9 AC Characteristics for CE#—Controlled Command Write Operations(1)
(Continued)

V_{CC} = 5V ± 0.5V, 5V ± 0.25V, T_A = 0° to +70°C, –40°C to +85°C

Sym	Parameter	Temp	Commercial						Extended			Unit
		Speed	–65			–70			–80			
		V_{CC}	5V ± 5%			5V ± 10%			5V ± 10%			
		Load	30 pF			50 pF			50 pF			
		Notes	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{AVAV}	Write Cycle Time		65			70			80			ns
t_{VPEH}1,2	V_{PP} Setup to CE# Going High	3,7	100			100			100			ns
t_{PHWL}	RP# Setup to WE# Going Low	3	300			480(9) 300(10)			480			ns
t_{WLEL}	WE# Setup to CE# Going Low	3,7	0			0			0			ns
t_{AVEH}	Address Setup to CE# Going High	2,6,7	40			50(9) 45(10)			50			ns
t_{DVEH}	Data Setup to CE# Going High	2,6,7	40			50(9) 45(10)			50			ns
t_{ELEH}	CE# Pulse Width	7	45			45(9) 50(10)			50			ns
t_{EHDX}	Data Hold from CE# High	2,7	0			0			0			ns
t_{EHAX}	Address Hold from CE# High	2,7	10			10			10			ns
t_{EHWH}	WE# Hold from CE# High	3,7	5			10(9) 5(10)			10			ns
t_{EHEL}	CE# Pulse Width High	7	15			30(9) 15(10)			30			ns
t_{GHEL}	Read Recovery before Write	3	0			0			0			ns
t_{EHRL}	CE# High to RY/BY# Going Low	3,7			100			100			100	ns
t_{RHPL}	RP# Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High	3	0			0			0			ns

5.9 AC Characteristics for CE#—Controlled Command Write Operations(1)

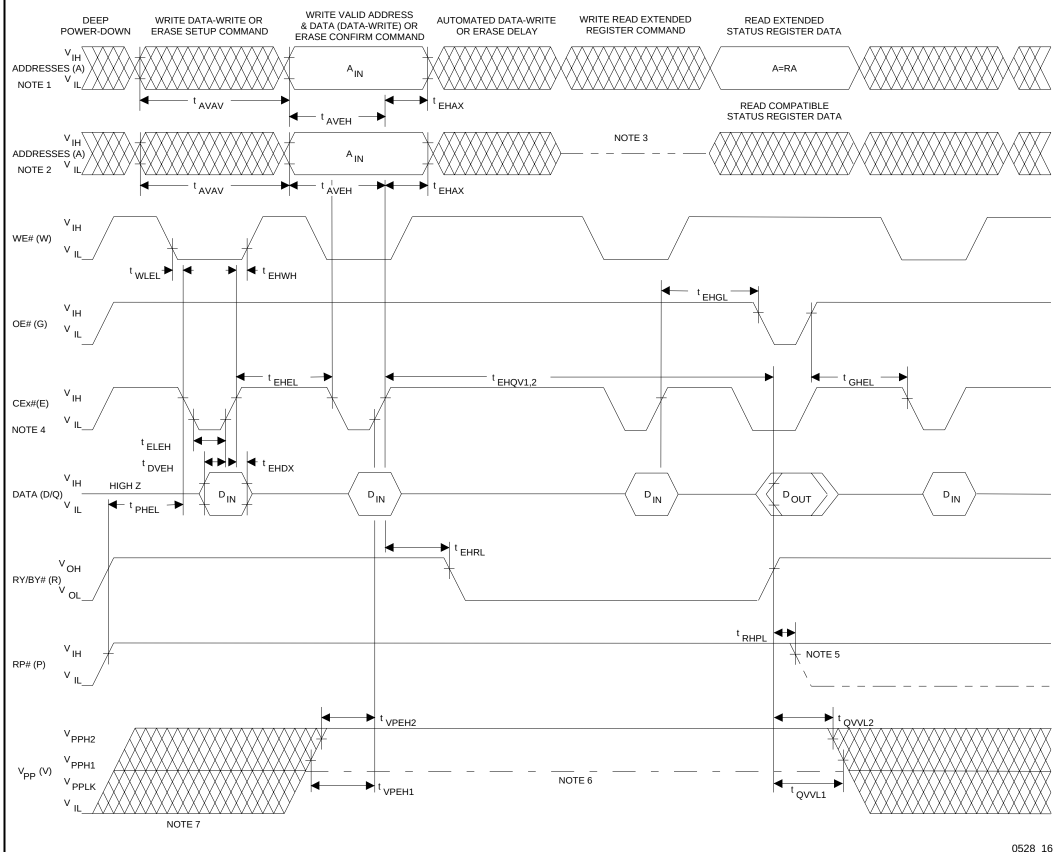
(Continued)

V_{CC} = 5V ± 0.5V, 5V ± 0.25V, T_A = 0° to +70°C, –40°C to +85°C

Sym	Parameter	Temp	Commercial						Extended			Unit
		Speed	–65			–70			–80			
		V_{CC}	5V ± 5%			5V ± 10%			5V ± 10%			
		Load	30 pF			50 pF			50 pF			
		Notes	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PHEL}	RP# High Recovery to CE# Going Low	3,7	0.300			1(9) 0.300(10)			1			µs
t_{EHGL}	Write Recovery before Read		55			60			65			ns
$t_{QVVL}1,2$	V_{PP} Hold from Valid Status Register (CSR, GSR, BSR) Data at RY/BY# High	3	0			0			0			µs
$t_{EHQV}1$	Duration of Program Operation	3,4,5,11	4.5	6	TBD	4.5	6	TBD	4.5	6	TBD	µs
$t_{EHQV}2$	Duration of Block Erase Operation	3,4	0.3	0.6	10	0.3	0.6	10	0.3	0.6	10	sec

NOTES:

1. Read timings during program and erase are the same as for normal read.
2. Refer to command definition tables for valid address and data values.
3. Sampled, not 100% tested. Guaranteed by design.
4. Program/erase durations are measured to valid Status Data. V_{PP} = 12V ± 0.6V.
5. Word/byte program operations are typically performed with 1 Programming Pulse.
6. Address and Data are latched on the rising edge of CE# for all command write operations.
7. CE_X# is defined as the latter of CE_0# or CE_1# going low, or the first of CE_0# or CE_1# going high.
8. Device speeds are defined as:
   65/70 ns at V_{CC} = 5V equivalent to
   75 ns at V_{CC} = 3.3V
   70/80 ns at V_{CC} = 5V equivalent to
   120 ns at V_{CC} = 3.3V
9. See the high speed AC Input/Output Reference Waveforms and AC Testing Load Circuit.
10. See the standard AC Input/Output Reference Waveforms and AC Testing Load Circuit.
11. The TBD information will be available in a technical paper. Please contact Intel's Application Hotline or your local sales office for more information.



NOTES:

1. This address string depicts data program/erase cycles with corresponding verification via ESRD.
2. This address string depicts data program/erase cycles with corresponding verification via CSRD.
3. This cycle is invalid when using CSRD for verification during data program/erase operations.
4. CE_X# is defined as the latter of CE_0# or CE_1# going low or the first of CE_0# or CE_1# going high.
5. RP# low transition is only to show t_{RHPL}; not valid for above read and write cycles.
6. V_{PP} voltage during program/erase operations valid at both 12V and 5V.
7. V_{PP} voltage equal to or below V_{PPLK} provides complete flash memory array protection.

Figure 16. Alternate AC Waveforms for Command Write Operations

5.10 AC Characteristics for WE#—Controlled Page Buffer Write Operations(1)

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C, –40°C to +85°C

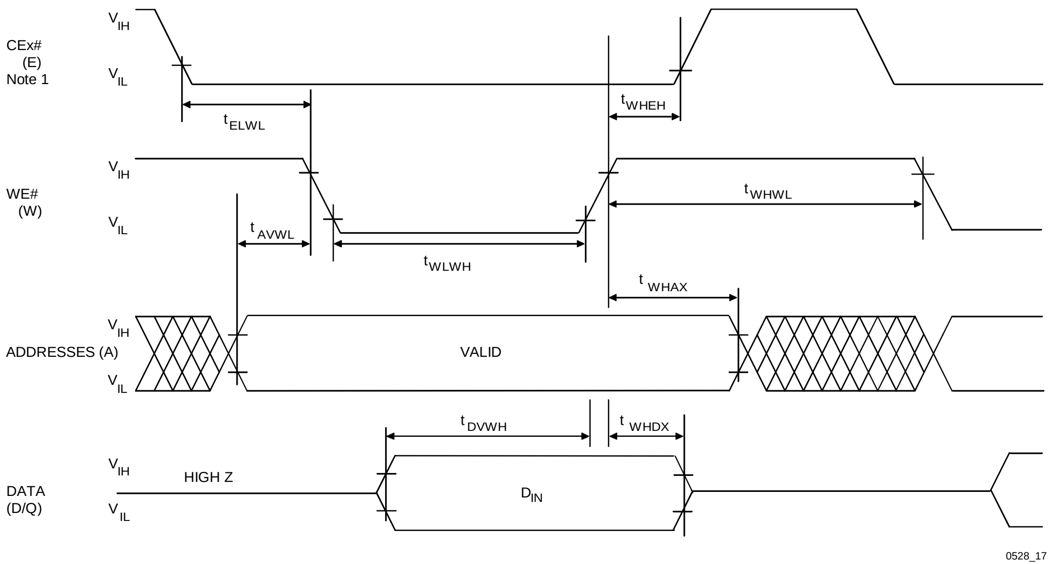
Sym	Parameter	Temp	Commercial/Extended			Unit
		Speed	–75, –100, –120			
		Notes	Min	Typ	Max	
t_{AVWL}	Address Setup to WE# Going Low	2	0			ns

V_{CC} = 5V ± 0.5V, 5V ± 0.25V, T_A = 0°C to +70°C, –40°C to +85°C

Sym	Parameter	Temp	Commercial						Comm/Ext			Unit
		Speed	–65			–70			–80			
		V_{CC}	5V ± 5%			5V ± 10%			5V ± 10%			
		Load	30 pF			50 pF			50 pF			
		Notes	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{AVWL}	Address Setup to WE# Going Low	2	0			0			0			ns

NOTES:

1. All other specifications for WE#—Controlled Write Operations can be found in section 5.8.
2. Address must be valid during the entire WE# low pulse.
3. Device speeds are defined as:
   65/70 ns at V_{CC} = 5V equivalent to
   75 ns at V_{CC} = 3.3V
   70/80 ns at V_{CC} = 5V equivalent to
   120 ns at V_{CC} = 3.3V
4. See the high speed AC Input/Output Reference Waveforms and AC Testing Load Circuit.
5. See the standard AC Input/Output Reference Waveforms and AC Testing Load Circuit.



NOTE:

1. CE_X# is defined as the latter of CE_0# or CE_1# going low, or the first of CE_0# or CE_1# going high.

Figure 17. WE#—Controlled Page Buffer Write Timing Waveforms (Loading Data to the Page Buffer)

5.11 AC Characteristics for CE#—Controlled Page Buffer Write Operations[1]

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C, –40°C to +85°C

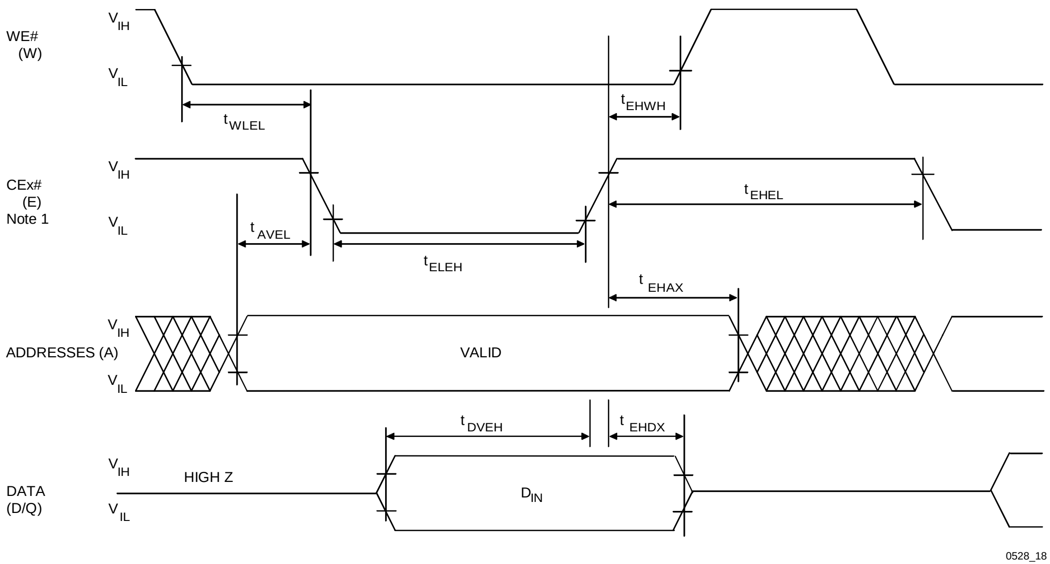
Sym	Parameter	Temp	Commercial/Extended			Unit
		Speed	–75, –100, –120			
		Notes	Min	Typ	Max	
t_{AVEL}	Address Setup to CE# Going Low	2,3	0			ns

V_{CC} = 5V ± 0.5V, 5V ± 0.25V, T_A = 0°C to +70°C, –40°C to +85°C

Sym	Parameter	Temp	Commercial						Comm/Ext			Unit
		Speed	–65			–70			–80			
		V_{CC}	5V ± 5%			5V ± 10%			5V ± 10%			
		Load	30 pF			50 pF			50 pF			
		Notes	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{AVEL}	Address Setup to CE# Going Low	2,3	0			0			0			ns

NOTES:

1. All other specifications for CE#—Controlled Write Operations can be found in Section 5.9.
2. Address must be valid during the entire WE# low pulse.
3. CE_X# is defined as the latter of CE_0# or CE_1# going low, or the first of CE_0# or CE_1# going high.
4. Device speeds are defined as:
   65/70 ns at V_{CC} = 5V equivalent to
   75 ns at V_{CC} = 3.3V
   70/80 ns at V_{CC} = 5V equivalent to
   120 ns at V_{CC} = 3.3V
5. See the high speed AC Input/Output Reference Waveforms and AC Testing Load Circuit.
6. See the standard AC Input/Output Reference Waveforms and AC Testing Load Circuit.



NOTE:

1. CEx# is defined as the latter of CE_0# or CE_1# going low, or the first of CE_0# or CE_1# going high.

Figure 18. CE#—Controlled Page Buffer Write Timing Waveforms (Loading Data to the Page Buffer)

5.12 Erase and Word/Byte Program Performance[3,5]

V_{CC} = 3.3V ± 0.3V, V_{PP} = 5V ± 0.5V, T_A = 0°C to +70°C

Symbol	Parameter	Notes	Min	Typ[1]	Max	Units	Test Conditions
	Page Buffer Byte Write Time	2,6,7	TBD	8.0	TBD	µs	
	Page Buffer Word Write Time	2,6,7	TBD	16.0	TBD	µs	
t_{WHRH}1A	Byte Program Time	2,7	TBD	29.0	TBD	µs	
t_{WHRH}1B	Word Program Time	2,7	TBD	35.0	TBD	µs	
t_{WHRH}2	Block Program Time	2,7	TBD	1.9	TBD	sec	Byte Prog. Mode
t_{WHRH}3	Block Program Time	2,7	TBD	1.2	TBD	sec	Word Prog. Mode
	Block Erase Time	2,7	TBD	1.4	TBD	sec	
	Full Chip Erase Time	2,7	TBD	44.8	TBD	sec	
	Erase Suspend Latency Time to Read	4	1.0	12	75	µs	
	Auto Erase Suspend Latency Time to Program		4.0	15	80	µs	

V_{CC} = 3.3V ± 0.3V, V_{PP} = 12V ± 0.6V, T_A = 0°C to +70°C

Symbol	Parameter	Notes	Min	Typ[1]	Max	Units	Test Conditions
	Page Buffer Byte Write Time	2,6,7	TBD	2.2	TBD	µs	
	Page Buffer Word Write Time	2,6,7	TBD	4.4	TBD	µs	
t_{WHRH}1	Word/Byte Program Time	2,7	5	9	TBD	µs	
t_{WHRH}2	Block Program Time	2,7	TBD	0.6	2.1	sec	Byte Prog. Mode
t_{WHRH}3	Block Program Time	2,7	TBD	0.3	1.0	sec	Word Prog. Mode
	Block Erase Time	2	0.3	0.8	10	sec	
	Full Chip Erase Time	2,7	TBD	25.6	TBD	sec	
	Erase Suspend Latency Time to Read	4	1.0	9	55	µs	
	Auto Erase Suspend Latency Time to Program		4.0	12	60	µs	

5.12 Erase and Word/Byte Program Performance(3,5) (Continued)

V_{CC} = 5V ± 0.5V, 5V ± 0.25V, V_{PP} = 5V ± 0.5V, T_A = 0°C to +70°C

Symbol	Parameter	Notes	Min	Typ(1)	Max	Units	Test Conditions
	Page Buffer Byte Write Time	2,6,7	TBD	8.0	TBD	µs	
	Page Buffer Word Write Time	2,6,7	TBD	16.0	TBD	µs	
t_{WHRH}1A	Byte Program Time	2,7	TBD	20	TBD	µs	
t_{WHRH}1B	Word Program Time	2,7	TBD	25	TBD	µs	
t_{WHRH}2	Block Program Time	2,7	TBD	1.4	TBD	sec	Byte Prog. Mode
t_{WHRH}3	Block Program Time	2,7	TBD	0.85	TBD	sec	Word Prog. Mode
	Block Erase Time	2,7	TBD	1.0	TBD	sec	
	Full Chip Erase Time	2,7	TBD	32.0	TBD	sec	
	Erase Suspend Latency Time to Read	4	1.0	9	55	µs	
	Auto Erase Suspend Latency Time to Program		3.0	12	60	µs	

V_{CC} = 5V ± 0.5V, 5V ± 0.25V, V_{PP} = 12V ± 0.6V, T_A = 0°C to +70°C

Symbol	Parameter	Notes	Min	Typ(1)	Max	Units	Test Conditions
	Page Buffer Byte Write Time	2,6,7	TBD	2.1	TBD	µs	
	Page Buffer Word Write Time	2,6,7	TBD	4.1	TBD	µs	
t_{WHRH}1	Word/Byte Program Time	2,7	4.5	6	TBD	µs	
t_{WHRH}2	Block Program Time	2,7	TBD	0.4	2.1	sec	Byte Prog. Mode
t_{WHRH}3	Block Program Time	2,7	TBD	0.2	1.0	sec	Word Prog. Mode
	Block Erase Time	2	0.3	0.6	10	sec	
	Full Chip Erase Time	2,7	TBD	19.2	TBD	sec	
	Erase Suspend Latency Time to Read	4	1.0	7	40	µs	
	Auto Erase Suspend Latency Time to Program		3.0	10	45	µs	

NOTES:

1. +25°C, and nominal voltages.
2. Excludes system-level overhead.
3. These performance numbers are valid for all speed versions.
4. Specification applies to interrupt latency for single block erase. Suspend latency for erase all unlocked blocks operation extends the maximum latency time to 270 µs.
5. Sampled, but not 100% tested. Guaranteed by design.
6. Assumes using the full Page Buffer to Program to Flash (256 bytes or 128 words).
7. The TBD information will be available in a technical paper. Please contact Intel's Application Hotline or your local sales office for more information.

6.0 MECHANICAL SPECIFICATIONS

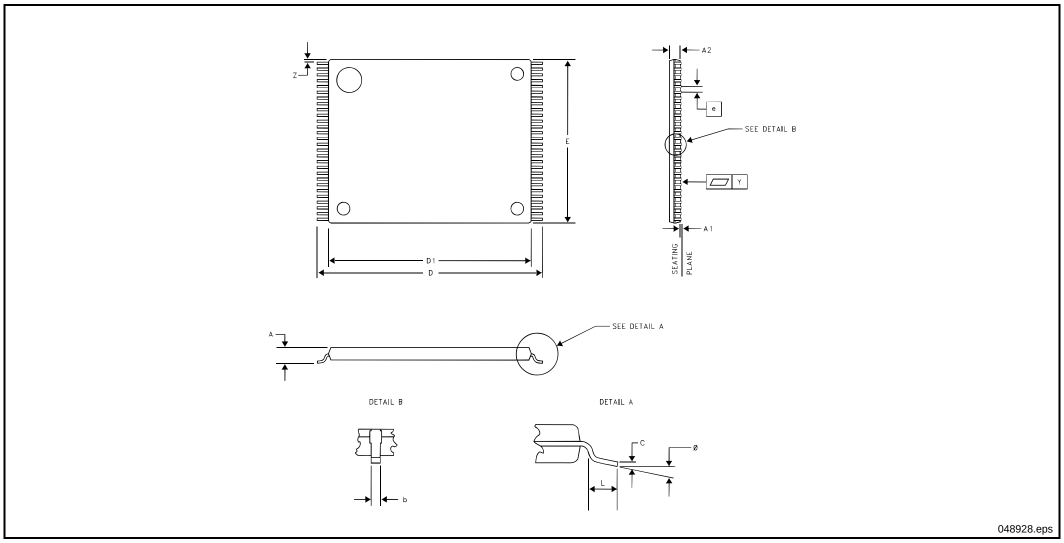


Figure 19. Mechanical Specifications of the 28F016SV 56-Lead TSOP Type I Package

Family: Thin Small Out-Line Package				
Symbol	**Millimeters**			**Notes**
	Minimum	**Nominal**	**Maximum**	
A			1.20	
A_1	0.050			
A_2	0.965	0.995	1.025	
b	0.100	0.150	0.200	
c	0.115	0.125	0.135	
D_1	18.20	18.40	18.60	
E	13.80	14.00	14.20	
e		0.50		
D	19.80	20.00	20.20	
L	0.500	0.600	0.700	
N		56		
∅	0°	3°	5°	
Y			0.100	
Z	0.150	0.250	0.350	

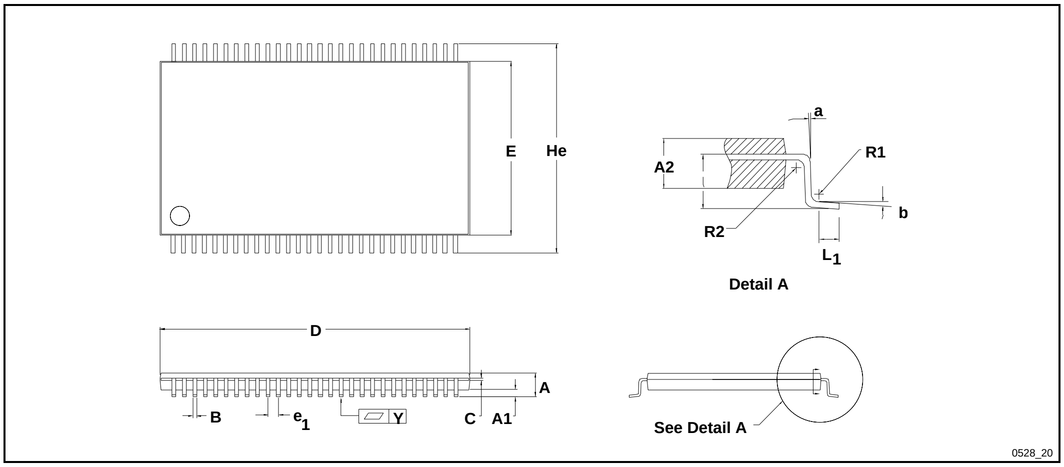
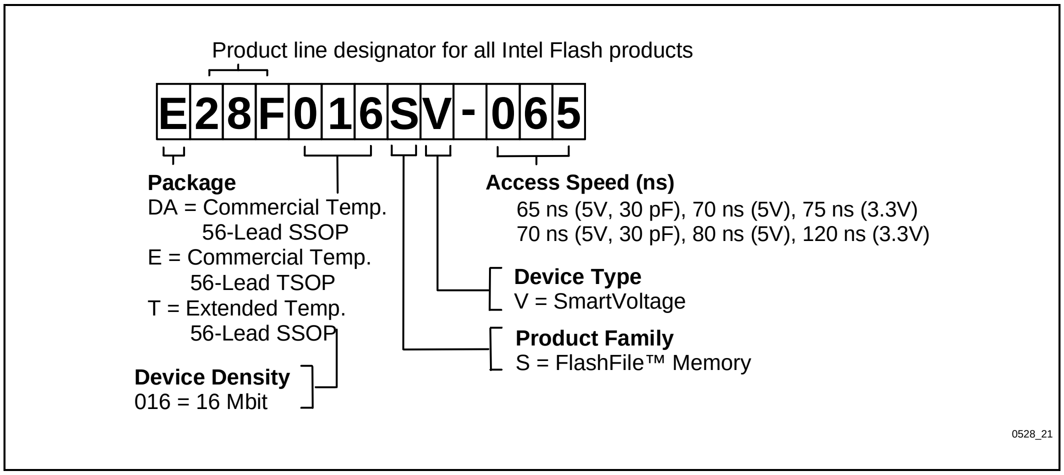


Figure 20. Mechanical Specifications of the 28F016SV 56-Lead SSOP Type I Package

Family: Shrink Small Out-Line Package				
Symbol	**Millimeters**			**Notes**
	Minimum	**Nominal**	**Maximum**	
A		1.80	1.90	
A1	0.47	0.52	0.57	
A2	1.18	1.28	1.38	
B	0.25	0.30	0.40	
C	0.13	0.15	0.20	
D	23.40	23.70	24.00	
E	13.10	13.30	13.50	
e_1		0.80		
He	15.70	16.00	16.30	
N		56		
L_1	0.45	0.50	0.55	
Y			0.10	
a	2°	3°	4°	
b	3°	4°	5°	
R1	0.15	0.20	0.25	
R2	0.15	0.20	0.25	

APPENDIX A
DEVICE NOMENCLATURE AND ORDERING INFORMATION



Option	Order Code	Valid Combinations		
		V_{CC} = 3.3V ± 0.3V, 50 pF load, 1.5V I/O Levels(1)	V_{CC} = 5V ± 10%, 100 pF load TTL I/O Levels(1)	V_{CC} = 5V ± 5%, 30 pF load 1.5V I/O Levels(1)
1	E28F016SV 070	E28F016SV-120	E28F016SV-080	E28F016SV-070
2	E28F016SV 065	E28F016SV-075	E28F016SV-070	E28F016SV-065
3	DA28F016SV 070	DA28F016SV-120	DA28F016SV-080	DA28F016SV-070
4	DA28F016SV 065	DA28F016SV-075	DA28F016SV-070	DA28F016SV-065
5	DT28F016SV 080	DT28F016SV-100	DT28F016SV-080	DT28F016SV-080

NOTE:

1. See Section 5.2 for Transient Input/Output Reference Waveforms and Testing Load Circuits.

APPENDIX B
ADDITIONAL INFORMATION(1,2)

Order Number	Document/Tool
297372	*16-Mbit Flash Product Family User's Manual*
290429	*28F008SA Datasheet*
290490	*DD28F032SA 32-Mbit (2 bit x 16, 4 Mbit x 8) FlashFile™ Memory Datasheet)*
292092	*AP-357 Power Supply Solutions for Flash Memory*
292123	*AP-374 Flash Memory Write Protection Techniques*
292126	*AP-377 16-Mbit Flash Product Family Software Drivers, 28F016SA/28F016SV/28F016XS/28F016XD*
292144	*AP-393 28F016SV Compatibility with 28F016SA*
292159	*AP-607 Multi-Site Layout Planning with Intel's FlashFile™ Components, Including ROM Capability*
292163	*AP-610 Flash Memory In-System Code and Data Update Techniques*
292165	*AB-62 Compiled Code Optimizations for Flash Memories*
294016	*ER-33 ETOX™ Flash Memory Technology—Insight to Intel's Fourth Generation Process Innovation*
297508	FLASHBuilder Utility
Contact Intel/Distribution Sales Office	Flash Cycling Utility
Contact Intel/Distribution Sales Office	28F016SV iBIS Model
Contact Intel/Distribution Sales Office	28F016SV VHDL
Contact Intel/Distribution Sales Office	28F016SV Timing Designer Library Files
Contact Intel/Distribution Sales Office	28F016SV Orcad and ViewLogic Schematic Symbols

NOTES:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.Intel.com for technical documentation and tools.