The future...today.

EDH 8808AC
70/10/12/15 LP
Monolithic

8Kx8 Static RAM
CMOS, Low Power
Monolithic

The EDH 8808AC-LP is a high performance, low power CMOS Static RAM organized as 8192 words by 8 bits each. In addition to 13 address inputs and 8 common data inputs and outputs, the device contains 4 control lines. The E1 and E2 lines perform chip enable functions and automatically power down the device when proper logic levels are applied. The G and W lines facilitate read and write operations.

The EDH 8808AC-LP offers battery back-up data retention capability at V_{DD} equal to 2V.

All inputs and outputs are TTL compatible and operate from a single 5V supply.

All EDI Military Components are 100% processed to the test method of MIL-STD-883 Class B.

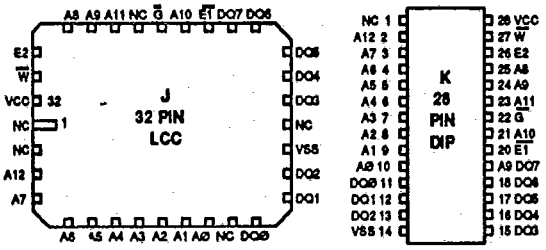
Features

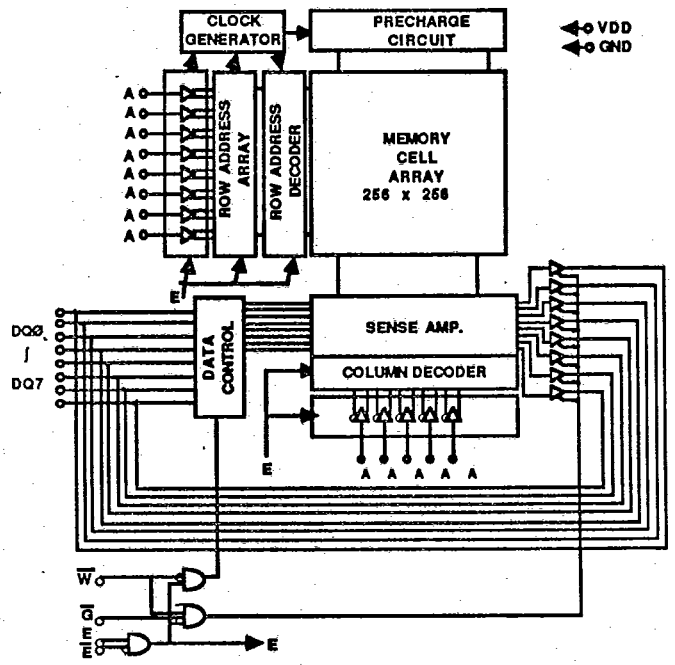
64K bit CMOS Static RAM
Organized as 8,192 x8 Bits
- Access Times of 70,100, 120 and 150ns
- $\overline{E}$ and $\overline{G}$ Functions for Bus Control
- Data Retention Function
- Low Power Operation
  - Active: 250mW
  - Standby: 250µW
- TTL Compatible Inputs and Outputs

JEDEC Approved Pinout
- 32 Pin Leadless Chip Carrier
- 28 Pin Dual-in-line Package

Single 5V(±10%) Supply Operation

Pin Configurations and Block Diagram





Pin Names

$\overline{A0}$-A 12	Address Inputs
E1	Chip Enable
$\overline{E2}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQØ-DQ7	Data Input/Output
V_{CC}	Power (+5V ±10%)
V_{SS}	Ground

Absolute Maximum Ratings*

Voltage on any pin relative to V_{SS}	-0.3V to 7.0V
Operating Temperature T_A (Ambient)	
Industrial	-40°C to +85°C
Military	-55°C to +125°C
Storage Temperature (Ambient/Ceramic)	-65°C to +150°C
Power Dissipation	1W
Output Current	20mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	Ø	Ø	Ø	V
Input High Voltage	V_{IH}	2.2	--	6.0	V
Input Low Voltage	V_{IL}	-0.3	--	0.8	V

DC Electrical Characteristics

(T_A = -55°C to +125°C; V_{CC} = 5.0V ±10%)

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power Supply Current	I_{CC1}	$\overline{E1}$= V_{IL}, $I_{I/O}$ = ØmA E2=V_{IH}, Min Cycle	--	50	80	mA
Standby (TTL) Power Supply Current	I_{CC2}	$\overline{E1}$≥ V_{IH} or E2≤ V_{IL}	--	2	10† 4††	mA mA
Full Standby Power Supply Current	I_{CC3}	$\overline{E1}$≥ V_{CC}-0.2V or E2≤0.2V V_{IN} ≥V_{CC}-0.2V or V_{IN} ≤0.2V	--	50	2000† 400††	µA µA
Input Leakage Current	I_{IL}	V_{IN} = ØV to V_{CC}	--	--	5	µA
Output Leakage Current	I_{OL}	$V_{I/O}$ = ØV to V_{CC} E1=V_{IH} or E2=V_{IL} or G=V_{IH}	--	--	5	µA
Output High Voltage	V_{OH}	I_{OH} = -1.0mA	2.4	--	--	V
Output Low Voltage	V_{OL}	I_{OL}= 2.1mA	--	--	0.4	V

*Typical = T_A = 25°C, V_{CC} = 5.0V

†70/100ns; ††120/150ns

Truth Table

$\overline{G}$	$\overline{E1}$	E2	$\overline{W}$	Mode	Output	Power
X	H	X	X	Standby	High Z	I_{CC2},I_{CC3}
X	X	L	X	Standby	High Z	I_{CC2}, I_{CC3}
H	L	H	H	Output Deselect	High Z	I_{CC1}
L	L	H	H	READ	D_{OUT}	I_{CC1}
X	L	H	L	WRITE	D_{IN}	I_{CC1}

Capacitance

($f = 1.0MHz$, $V_{IN} = V_{CC}$ or V_{SS})

Parameter	Sym	Max		Unit
		LCC	DIP	
Input Capacitance (except D/Q)	C_I	6	10	pF
Capacitance on D/Q pins	$C_{D/Q}$	8	12	pF

A.C. Test Conditions

Input Pulse Levels ..... V_{SS} to 3.0V
Input Rise and Fall Times 5ns
Input and Output Timing Levels 1.5V
Output Load ..... 1 TTL, $C_L = 100pF$

AC Characteristics
Read Cycle

(T_A = -55°C to +125°C; V_{CC} = 5.0V ±10%)

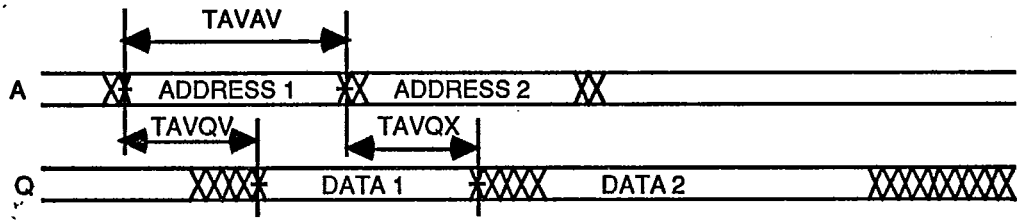
Parameter	Sym		70 ns Min	70 ns Max	100ns Min	100ns Max	Units
Read Cycle Time	TAVAV		70		100		ns
Address Access Time	TAVQV			70		100	ns
Chip Enable Access Time	TE1LQV	$\overline{E1}$		70		100	ns
	TE2HQV	E2		70		100	ns
Chip Enable to Output Low Z	TE1LQX	$\overline{E1}$	5		10		ns
	TE2HQX	E2	5		10		ns
Output Enable to Output Valid	TGLQV			45		50	ns
Output Enable to Output in Low Z	TGLQX		5		10		ns
Chip Enable to Output in High Z	TE1HQZ	$\overline{E1}$		35		35	ns
	TE2LQZ	E2		35		35	ns
Output Enable to Output in High Z	TGHQZ			35		35	ns
Output Hold from Address Change	TAVQX		10		10		ns

AC Characteristics
Read Cycle

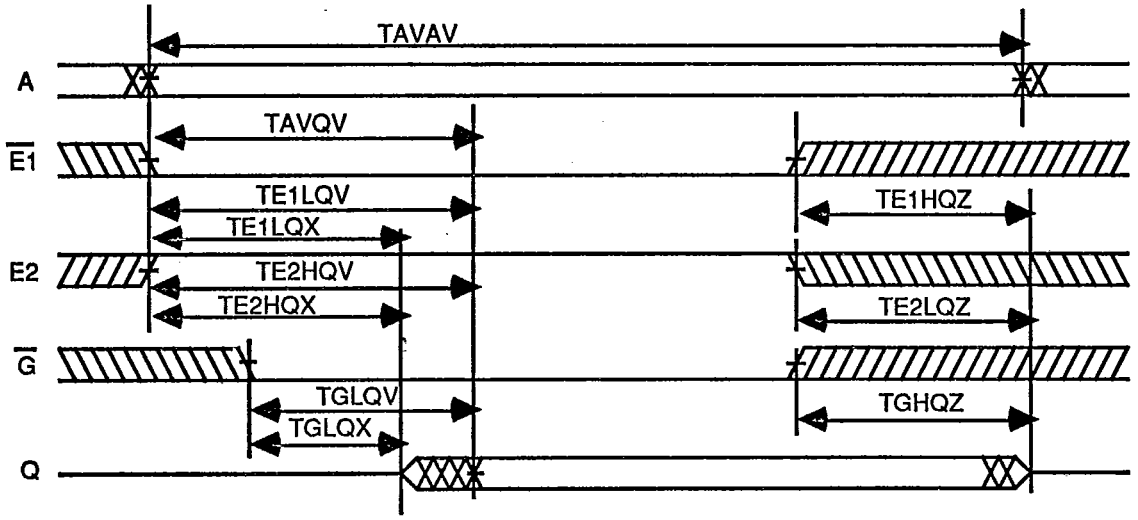
(T_A = -55°C to +125°C; V_{CC} = 5.0V ±10%)

Parameter	Sym		120 ns Min	120 ns Max	150ns Min	150ns Max	Units
Read Cycle Time	TAVAV		120		150		ns
Address Access Time	TAVQV			120		150	ns
Chip Enable Access Time	TE1LQV	$\overline{E1}$		120		150	ns
	TE2HQV	E2		120		150	ns
Chip Enable to Output Low Z	TE1LQX	$\overline{E1}$	10		15		ns
	TE2HQX	E2	10		15		ns
Output Enable to Output Valid	TGLQV			60		70	ns
Output Enable to Output in Low Z	TGLQX		10		15		ns
Chip Enable to Output in High Z	TE1HQZ	$\overline{E1}$		40		50	ns
	TE2LQZ	E2		40		50	ns
Output Enable to Output in High Z	TGHQZ			40		50	ns
Output Hold from Address Change	TAVQX		10		10		ns

READ CYCLE 1
$\overline{W}$, E2 HIGH; $\overline{G}$, $\overline{E1}$ LOW



READ CYCLE 2
$\overline{W}$ HIGH



Write Cycle

(T_A = -55°C to +125°C; V_{CC} = 5.0V ±10%)

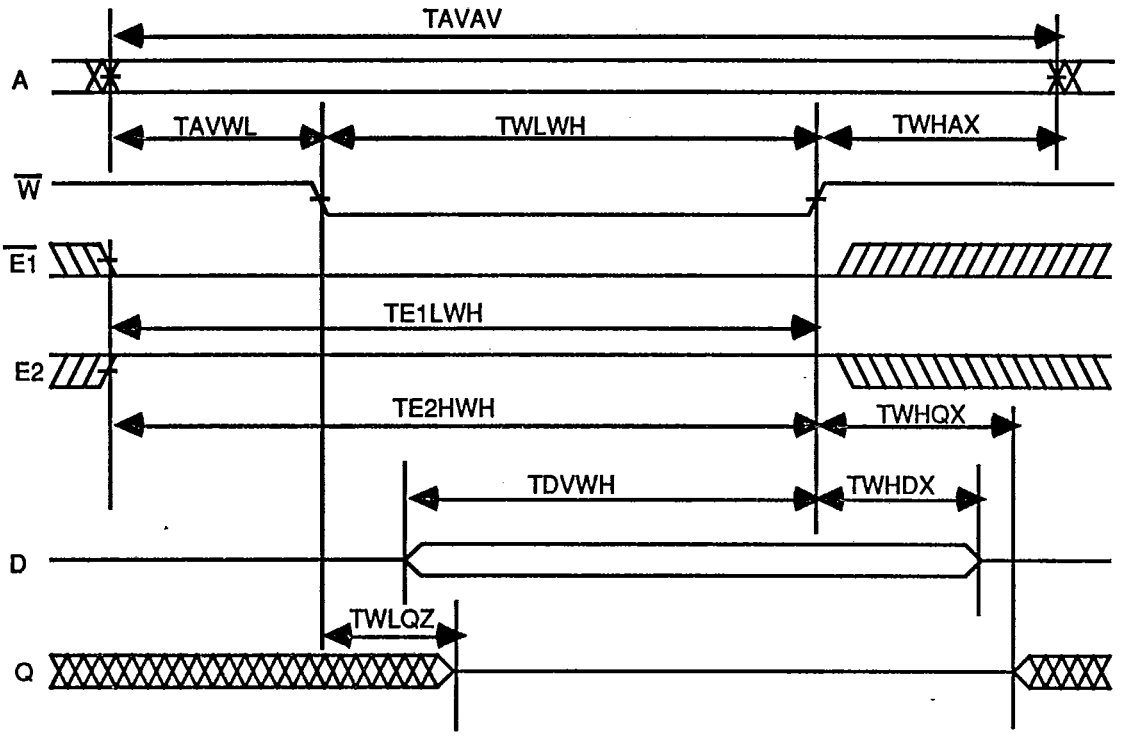
Parameter	Sym		70ns Min	70ns Max	100ns Min	100ns Max	Unit
Write Cycle Time	TAVAV		70		100		ns
Chip Enable to End of Write	TE1LWH	$\overline{E1}$	65		80		ns
	TE2HWH	E2	65		80		ns
Address Setup Time	TAVWL	$\overline{W}$	5		5		ns
	TAVE1L	$\overline{E1}$	5		5		ns
	TAVE2H	E2	5		5		ns
Write Pulse Width	TWLWH	$\overline{W}$	45		60		ns
	TE1LE1H	$\overline{E1}$	45		60		ns
	TE2HE2L	E2	60		60		ns
Write Recovery Time	TWHAX	$\overline{W}$	5		5		ns
	TE1HAX	$\overline{E1}$	5		5		ns
	TE2LAX	E2	5		5		ns
Data Hold Time	TWHDX	$\overline{W}$	5		5		ns
	TE1HDX	$\overline{E1}$	5		5		ns
	TE2LDX	E2	5		5		ns
Write to Output in High Z	TWLQZ			30		35	ns
Data to Write Time	TDVWH	$\overline{W}$	30		35		ns
	TDVE1H	$\overline{E1}$	30		35		ns
	TDVE2L	E2	30		35		ns
Output Active from End of Write	TWHQX		5		10		ns

Write Cycle

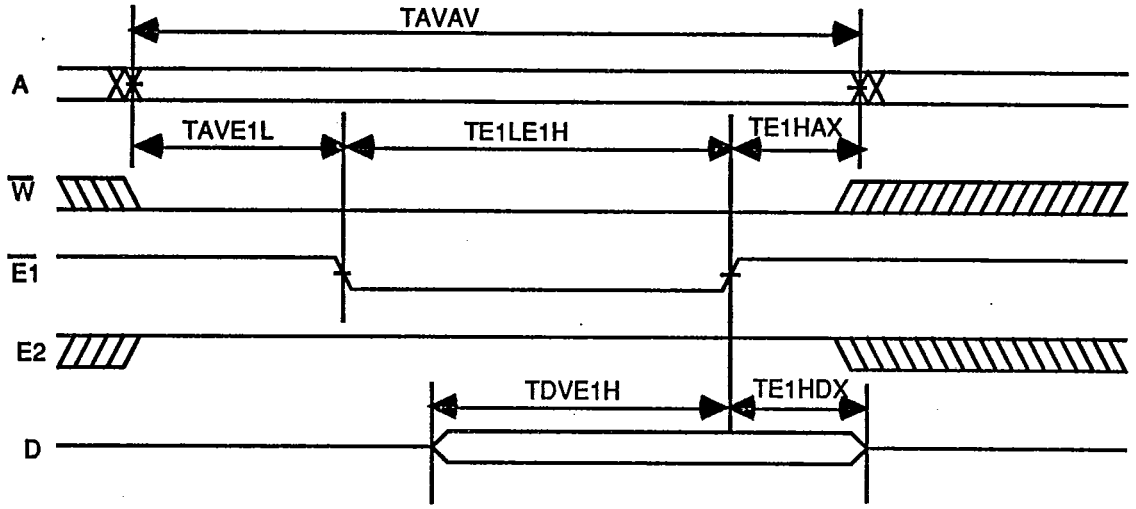
(T_A = -55°C to +125°C; V_{CC} = 5.0V ±10%)

Parameter	Sym		120ns Min	120ns Max	150 ns Min	150 ns Max	Units
Write Cycle Time	TAVAV		120		150		ns
Chip Enable to End of Write	TE1LWH	$\overline{E1}$	85		100		ns
	TE2HWH	E2	85		100		ns
Address Setup Time	TAVWL	$\overline{W}$	5		5		ns
	TAVE1L	$\overline{E1}$	5		5		ns
	TAVE2H	E2	5		5		ns
Write Pulse Width	TWLWH	$\overline{W}$	70		90		ns
	TE1LE1H	$\overline{E1}$	85		100		ns
	TE2HE2L	E2	85		100		ns
Write Recovery Time	TWHAX	$\overline{W}$	5		5		ns
	TE1HAX	$\overline{E1}$	5		5		ns
	TE2LAX	E2	5		5		ns
Data Hold Time	TWHDX	$\overline{W}$	5		5		ns
	TE1HDX	$\overline{E1}$	5		5		ns
	TE2LDX	E2	5		5		ns
Write to Output in High Z	TWLQZ			40		50	ns
Data to Write Time	TDVWH	$\overline{W}$	40		50		ns
	TDVE1H	$\overline{E1}$	40		50		ns
	TDVE2L	E2	40		50		ns
Output Active from End of Write	TWHQX		10		15		ns

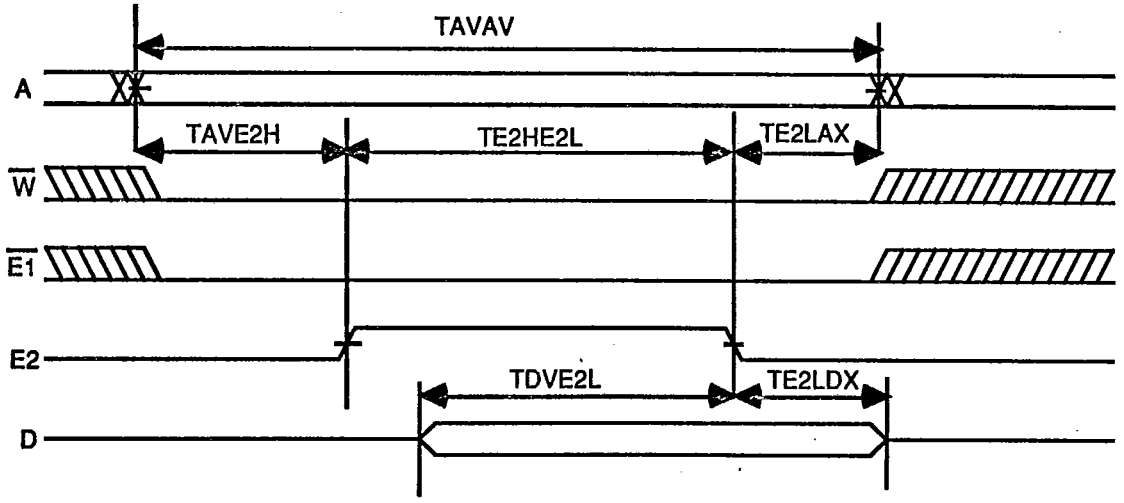
WRITE CYCLE 1
LATE WRITE



WRITE CYCLE 2
EARLY WRITE
$\overline{E1}$ CONTROLLED



WRITE CYCLE 3
EARLY WRITE
E2 CONTROLLED



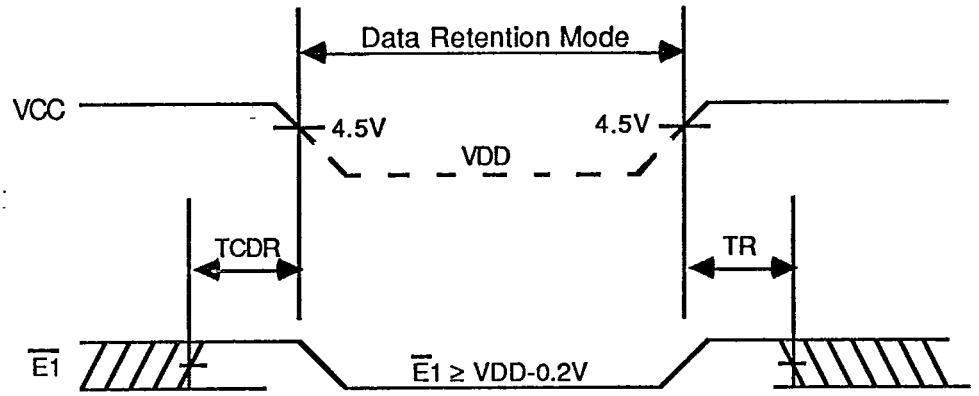
Data Retention Characteristics

(T_A = 0°C to +70°C or -55°C to +125°C)

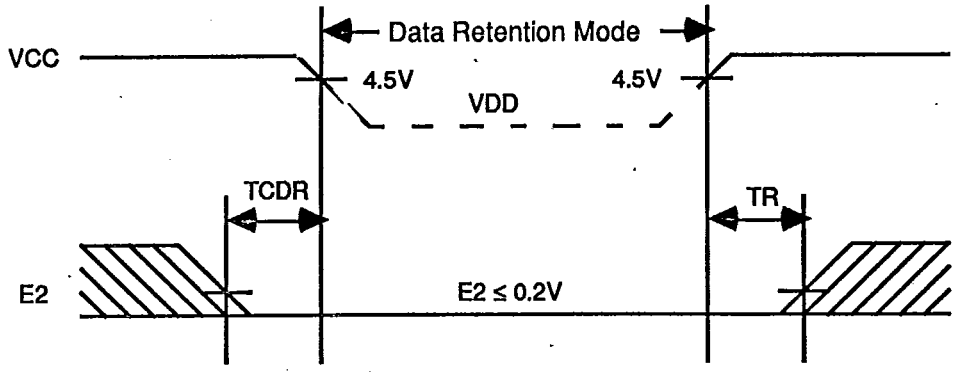
Characteristics	Sym	Test Conditions	Min	Typ	Max	Uni
Data Retention Voltage	V_{DD}	$\overline{E1} \geq V_{DD}$ -0.2V E2 ≤0.2V $V_{IN} \geq V_{DD}$-0.2V or $V_{IN} \leq 0.2V$	2.0			V
Data Retention Quiescent Current	I_{CCDR}	V_{DD} = 2.0V		25	250† 100††	µA
Chip Disable to Data Retention Time	TCDR		0			ns
Operation Recovery Time	TR		TAVAV*			ns

*TAVAV = READ CYCLE TIME †70/100ns; ††120/150ns

Data Retention Waveform
$\overline{E1}$ Controlled

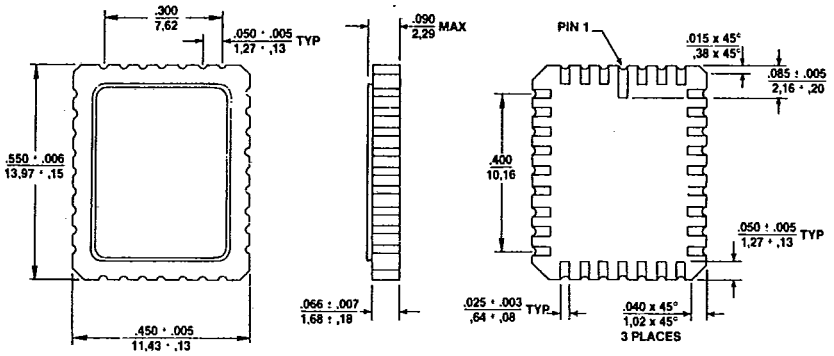


Data Retention Waveform
E2 Controlled

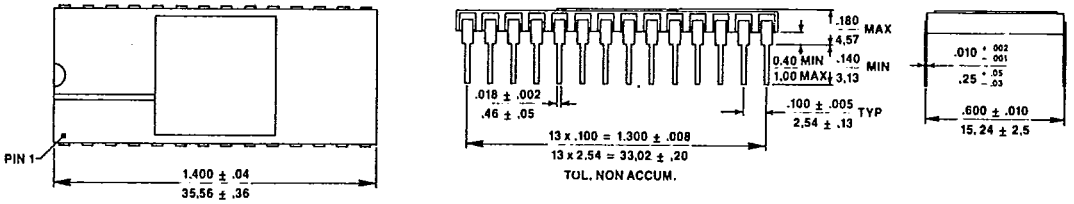


Package Description

J Package
32 Pin
Leadless Chip Carrier
Ceramic



K Package
28 Pin
Dual-in-line
Sidebrazed, Ceramic



Ordering Information

Part Number	Speed (ns)	Pkg.	Temp Range	Part Number	Speed (ns)	Pkg.	Temp Range
EDH 8808AC-15LP KMHR	150	K	Military	EDH 8808AC-15P KI	150	K	Industrial
EDH 8808AC-12LP KMHR	120	K	Military	EDH 8808AC-12LP KI	120	K	Industrial
EDH 8808AC-10LP KMHR	100	K	Military	EDH 8808AC-10LPKI	100	K	Industrial
EDH 8808AC-70LP KMHR	70	K	Military	EDH 8808AC-70LPKI	70	K	Industrial
EDH 8808AC-15LP JMHR	150	J	Military	EDH 8808AC-15LP JI	150	J	Industrial
EDH 8808AC-12LP JMHR	120	J	Military	EDH 8808AC-12LPJI	120	J	Industrial
EDH 8808AC-10LP JMHR	100	J	Military	E DH 808AC-10LPJI	100	J	Industrial
EDH 8808AC-70LP JMHR	70	J	Military	EDH 8808AC-70LPJI	70	J	Industrial

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