FULLFIP2
User Reference Manual

ALS 50262 d–en

First issue: 03–1994
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Meaning of terms that may be used in this document / Notice to readers

WARNING

Warning notices are used to emphasize that hazardous voltages, currents, temperatures, or other conditions that could cause personal injury exist or may be associated with use of a particular equipment.

In situations where inattention could cause either personal injury or damage to equipment, a Warning notice is used.

Caution

Caution notices are used where there is a risk of damage to equipment for example.

Note

Notes merely call attention to information that is especially significant to understanding and operating the equipment.

Index letter	Date	Nature of revision
a	03–1993	1st issue approved
b	06–1996	Revision
c	02–2000	ALSTOM branding of manual
d	08–2000	Chapter 4 Electrical characteristics, Network bit rate 5 Mbit/s

Revisions

1. PURPOSE OF MANUAL AND DOCUMENTED VERSION

This manual describes the FULLFIP2 component. The FULLFIP2 communication coprocessor imprements most of the link and application protocols of the WorldFIP fieldbus.

2. CONTENT OF THIS MANUAL

Chapter 1: Overview – This chapter provides a presentation of FULLFIP2 and its features.

Chapter 2: Pin assignments – Pin assignments and pin description for the FULLFIP2 coprocessor in a PLCC84 or a MQFP100.

Chapter 3: Functional description – Description of the Memory Access Controller, the user system interface and the network interface.

Chapter 4: Electrical characteristics.

Chapter 5: Physical dimensions.

Chapter 6: Application notes – Interfacing with the Motorola 6800 microprocessor, the Intel 80C1888 microprocessor, the external private memory and the line transceiver.

Chapter 7: Board design rules.

3. WE WELCOME YOUR COMMENTS AND SUGGESTIONS

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Preface

Reader's comments

ALS 50262 d–en	*FULLFIP2 User Reference Manual*

Your main job is:

- ☐ System designer
- ☐ Distributor
- ☐ System integrator
- ☐ Installer
- ☐ Programmer
- ☐ Maintenance
- ☐ Operator
- ☐ Other (specify below)

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All comments will be considered by qualified personnel.

REMARKS

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Reader's comments

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Chapter 1 Overview

1. GENERAL PRESENTATION

The FULLFIP2 component is a communication coprocessor implementing most of the link and application protocols of the WorldFIP fieldbus. It has been designed with VLSI TECHNOLOGY silicon compiler tools. The circuit contains more than 160,000 transistors in high density 0.8–µm C–MOS technology.

The FULLFIP2 chip is the second generation of the FULLFIP integrated circuit; it enhances communication performances by integrating the possibility to operate at the physical layer in conformance with the IEC standard and by increasing the network transmission rate.

This circuit is intended to equip any field device having a certain intelligence level such as PLC, I/O mux, Drive, Console,... capable of managing a great number of variables, including intelligent sensors and actuators.

It implements a set of periodic and aperiodic buffer transfer and messaging services of the data link layer, as well as for a station supporting the arbitrator function as for a slave station. It also supports the MPS application layer services including promptness, refreshment, and synchronization mechanisms. It can process up to 4096 identifiers among the 65536 possible on the network.

For this purpose it must have a private memory which can reach a size of 2 Mbytes. The objects handled by the circuit which constitutes the local data base are stored in this memory address space.

The circuit is microprogrammed. A part of the microprogram is located in an internal ROM while the remaining part is loaded into the internal RAM from the external private memory.

It is interfaced through a bus of type ’8–bit peripheral device’ with the ’user’ processor in charge of running the application software.

The user requests and the network events may be totally asynchronous as any database access conflict is solved by internal algorithms.

On the network side, FULLFIP2 is connected to the WorldFIP bus by a line driver which can be doubled to ensure medium redundancy. The circuit implements a FIP standardized full–duplex UART whose transmission rate is selectable among the following values: 31.25 Kbit/s, 1 Mbit/s, 2.5 Mbit/s and 5 Mbit/s.

The transmit and receive signals on the network interface are encoded data sequence (Manchester Biphase L).

The FULLFIP2 component implements several profiles of the MAU–MDS function (Medium Attachement Unit) that the different standards have in common.

STANDARD	IEC 61158–2	CENELEC EN50170 AFNOR/UTE NFC46–604
PROFILES	31.25 Kbit/s Wire / Voltage mode	CH–S1 profile
	1 Mbit/s Wire / Voltage mode	CH–S2 profile
	2.5 Mbit/s Wire / Voltage mode	CH–S3 profile
	5 Mbit/s Wire / Voltage mode	will be added in the next version of the 61158–2 standard

Table 1.1 – Profiles implemented in FULLFIP2

The circuit is available in two packages:

- 84–pin plastic leaded chip carrier (PLCC84), pin to pin compatible with the first FULLFIP chip generation,
- 100–pin metric quad flat pack (MQFP100), a more compact plastic package.

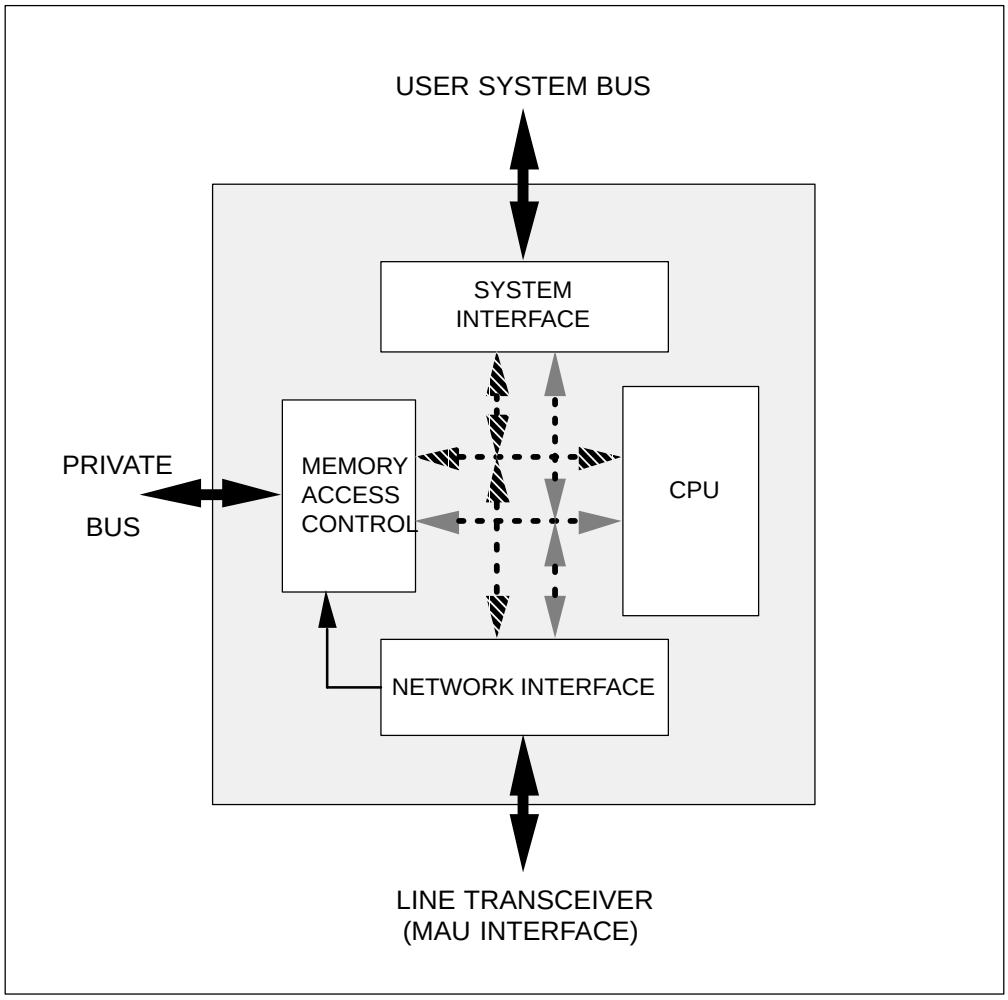


Figure 1.1 – FULLFIP2 Circuit Principle Block Diagram

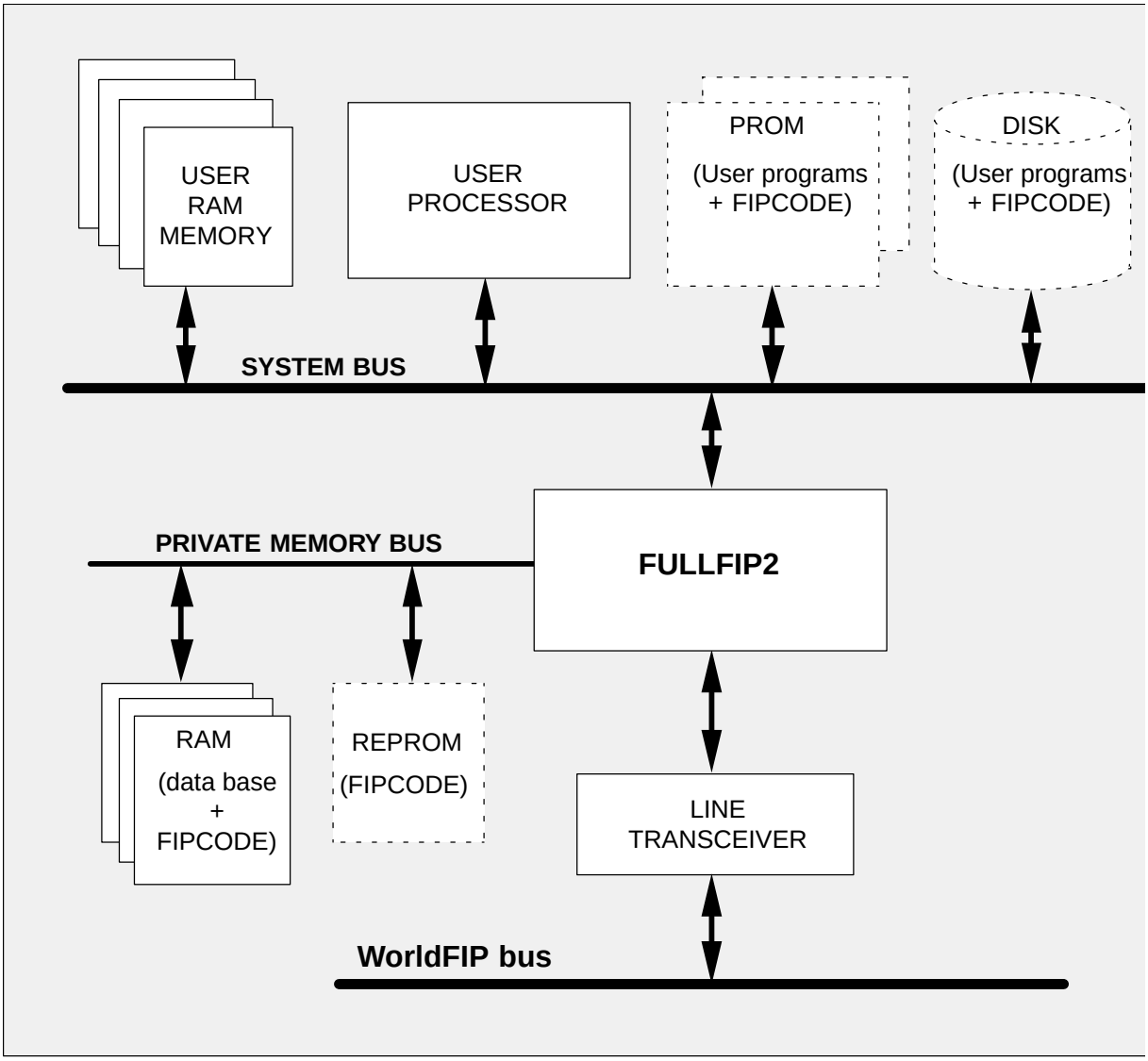


Figure 1.2 – Block diagram of a network subscriber

2. FEATURES

- compatible with standards AFNOR UTE NFC 46–601–7; CENELEC EN 50170 and IEC 1158,
- configurable as simple station, as well as, Bus Arbitrator and station,
- handles up to 4096 identifiers,
- bit rate from 31.25 Kbit/s to 5 Mbit/s,
- clock frequency operation up to 80 MHz,
- 8–bit Data Bus User Interface,
- direct interface with the line transceiver,
- private memory up to 2 Mbytes,
- extended temperature range –40°C + 85°C,
- available as a 84 PLCC or 100 MQFP.

Chapter 2 Pin assignments

1. PINOUT DIAGRAMS

1.1. PLCC84 package

The FULLFIP2 component is packaged in a PLCC84 or in a MQFP100.

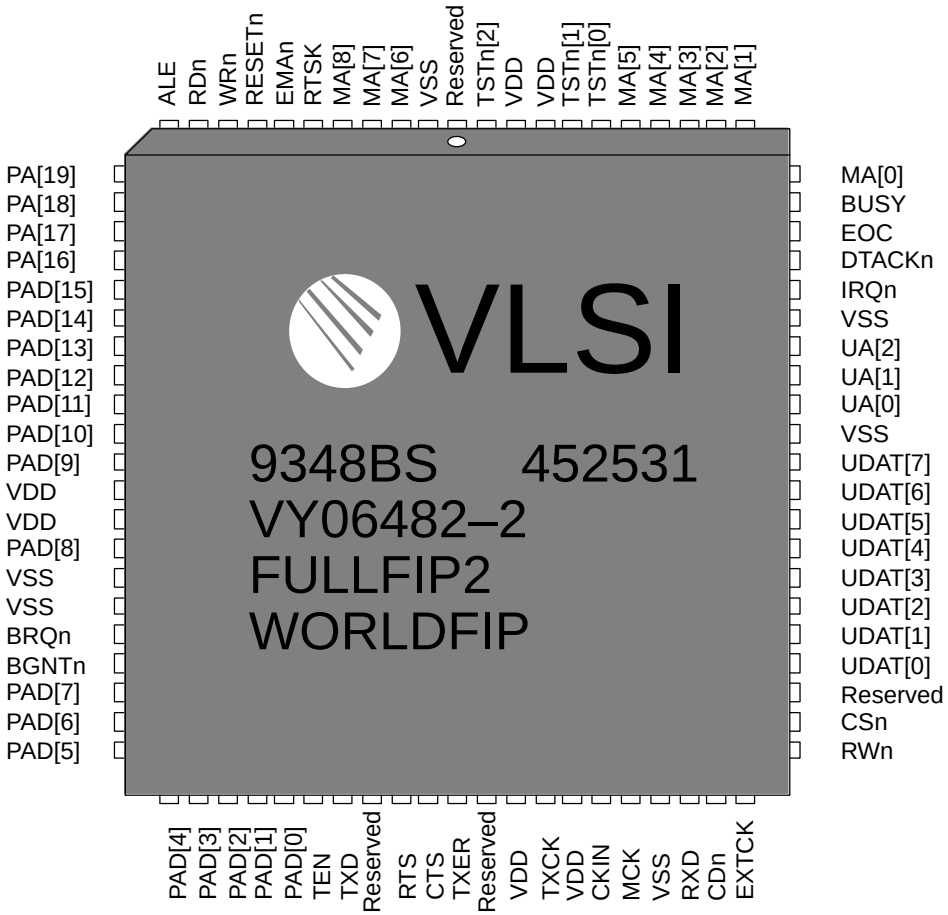


Figure 2.1 – FULLFIP2 pinout diagram – PLCC84 package – Top view

1.2. MQFP100 package

Figure 2.2 – FULLFIP2 pinout diagram – MQFP100 package – Top view

2. PIN DESCRIPTION

2.1. PLCC84 package

No.	Pin	Type	Io max	Description
1	Reserved	3–s. output	2 mA	Reserved – (TSTCK in the first generation)
2	VSS	Supply		System ground 0 V – Periphery
3	MA[6]	3–s. output	2 mA	MICRO_ADDRESS – Microprogram address
4	MA[7]	3–s. output	2 mA	MICRO_ADDRESS – Microprogram address
5	MA[8]	3–s. output	2 mA	MICRO_ADDRESS – Microprogram address
6	RTSK	3–s. output	2 mA	RUNNING TASK
7	EMAn	Pullup input		ENABLE MICRO_ADDRESS – MA bus validation
8	RESETn	Trigger input		RESET – Circuit initialization
9	WRn	Output	4 mA	WRITE STROBE – Writing signal for private memory
10	RDn	Output	4 mA	READ STROBE – Reading signal for private memory
11	ALE	Output	4 mA	ADDRESS LATCH ENABLE – Address validation
12	PA[19]	3–s. output	4 mA	PRIVATE ADDRESS – Private bus address
13	PA[18]	3–s. output	4 mA	PRIVATE ADDRESS – Private bus address
14	PA[17]	3–s. output	4 mA	PRIVATE ADDRESS – Private bus address
15	PA[16]	3–s. output	4 mA	PRIVATE ADDRESS – Private bus address
16	PAD[15]	I/O	4 mA	PRIVATE ADDRESS/DATA – Multiplexed Address/Data
17	PAD[14]	I/O	4 mA	PRIVATE ADDRESS/DATA – Multiplexed Address/Data
18	PAD[13]	I/O	4 mA	PRIVATE ADDRESS/DATA – Multiplexed Address/Data
19	PAD[12]	I/O	4 mA	PRIVATE ADDRESS/DATA – Multiplexed Address/Data
20	PAD[11]	I/O	4 mA	PRIVATE ADDRESS/DATA – Multiplexed Address/Data
21	PAD[10]	I/O	4 mA	PRIVATE ADDRESS/DATA – Multiplexed Address/Data
22	PAD[9]	I/O	4 mA	PRIVATE ADDRESS/DATA – Multiplexed Address/Data
23	VDD	Supply		Supply voltage +5 V – Core
24	VDD	Supply		Supply voltage +5 V – Periphery
25	PAD[8]	I/O	4 mA	PRIVATE ADDRESS/DATA – Multiplexed Address/Data
26	VSS	Supply		System ground 0 V – Periphery
27	VSS	Supply		System ground 0 V – Core
28	BRQn	Output	2 mA	BUS REQUEST – Bus access request
29	BGNTn	Input		BUS GRANT – Bus access grant
30	PAD[7]	I/O	4 mA	PRIVATE ADDRESS/DATA – Multiplexed Address/Data
31	PAD[6]	I/O	4 mA	PRIVATE ADDRESS/DATA – Multiplexed Address/Data
32	PAD[5]	I/O	4 mA	PRIVATE ADDRESS/DATA – Multiplexed Address/Data
33	PAD[4]	I/O	4 mA	PRIVATE ADDRESS/DATA – Multiplexed Address/Data
34	PAD[3]	I/O	4 mA	PRIVATE ADDRESS/DATA – Multiplexed Address/Data
35	PAD[2]	I/O	4 mA	PRIVATE ADDRESS/DATA – Multiplexed Address/Data
36	PAD[1]	I/O	4 mA	PRIVATE ADDRESS/DATA – Multiplexed Address/Data
37	PAD[0]	I/O	4 mA	PRIVATE ADDRESS/DATA – Multiplexed Address/Data
38	TEN	Output	2 mA	TRANSMIT ENABLE – Transmitter validation
39	TXD	Output	2 mA	SERIAL DATA OUT
40	Reserved	Output	2 mA	Reserved (TEN2 in the first generation)
41	RTS	Output	2 mA	REQUEST TO SEND
42	CTS	Input		CLEAR TO SEND
43	TXER	Input		TRANSMIT ERROR – Error on transmitter

Table 2.1 – FULLFIP2 pin description – PLCC84 package

No.	Pin	Type	Io max	Description
44	Reserved	Input		Reserved (TXER2 in the first generation)
45	VDD	Supply		Supply voltage +5 V – Core
46	TXCK	I/O	2 mA	TRANSMIT CLOCK
47	VDD	Supply		Supply voltage +5 V – Periphery
48	CKIN	Input		CLOCK INPUT – Basic clock
49	MCK	Output	2 mA	MASTER CLOCK – Main clock output
50	VSS	Supply		System ground 0 V – Periphery
51	RXD	Input		SERIAL DATA IN
52	CDn	Input		CARRIER DETECT
53	EXTCK	Pulldown input		EXTERNAL TEST CLOCK – External test clock selection
54	RWn	Input		READ/WRITE – Read/write selection on system bus
55	CSn	Input		CHIP SELECT
56	Reserved	Input		Reserved – (DSn in the first generation)
57	UDAT[0]	I/O	4 mA	USER DATA – System bus data
58	UDAT[1]	I/O	4 mA	USER DATA – System bus data
59	UDAT[2]	I/O	4 mA	USER DATA – System bus data
60	UDAT[3]	I/O	4 mA	USER DATA – System bus data
61	UDAT[4]	I/O	4 mA	USER DATA – System bus data
62	UDAT[5]	I/O	4 mA	USER DATA – System bus data
63	UDAT[6]	I/O	4 mA	USER DATA – System bus data
64	UDAT[7]	I/O	4 mA	USER DATA – System bus data
65	VSS	Supply		System ground 0 V – Core
66	UA[0]	Input		USER ADDRESS – System bus address
67	UA[1]	Input		USER ADDRESS – System bus address
68	UA[2]	Input		USER ADDRESS – System bus address
69	VSS	Supply		System ground 0 V – Core
70	IRQn	Output	2 mA	INTERRUPT REQUEST
71	DTACKn	3–s. output	2 mA	DATA ACKNOWLEDGE – Access acknowledge
72	EOC	Output	2 mA	END OF CYCLE – End of Bus Arbitrator cycle
73	BUSY	Output	4 mA	CHIP BUSY – Working transaction
74	MA[0]	3–s. output	4 mA	MICRO_ADDRESS – Microprogram address
75	MA[1]	3–s. output	4 mA	MICRO_ADDRESS – Microprogram address
76	MA[2]	3–s. output	4 mA	MICRO_ADDRESS – Microprogram address
77	MA[3]	3–s. output	4 mA	MICRO_ADDRESS – Microprogram address
78	MA[4]	3–s. output	4 mA	MICRO_ADDRESS – Microprogram address
79	MA[5]	3–s. output	4 mA	MICRO_ADDRESS – Microprogram address
80	TSTn[0]	Pullup input		TEST INPUT – Test mode control
81	TSTn[1]	Pullup input		TEST INPUT – Test mode control
82	VDD	Supply		Supply voltage +5 V – Periphery
83	VDD	Supply		Supply voltage +5 V – Core
84	TSTn[2]	Pullup input		TEST INPUT – Test mode control

Note 1: FULLFIP2 is designed using CMOS technology ; all input signals are TTL compatible and all ouput signals are CMOS compatible.
Note 2: RESETn is a Schmitt–Trigger input. Initialization of the FULLFIP2 component is performed by keeping RESETn to the low level during 32T (T = 1/CKIN).
Note 3: Internal pullups are implemented on inputs in order to avoid floating input signals but they do not fix a definite input level. It will be then necessary to add external pullup/down elements.
Note 4: The pins PA[19:16] become tri–stated whenever BGNTn is high.
Note 5: All pins of type 'output', except MCK, become tri–stated whenever TSTn[1] is low.

Table 2.1 – FULLFIP2 pin description – PLCC84 package (continued)

2.2. MQFP100 package

No.	Pin	Type	Io max	Description
1	n.c.	Input		Unused
2	n.c.	Input		Unused
3	n.c.	Input		Unused
4	n.c.	Input		Unused
5	PA[19]	3–s. output	4 mA	PRIVATE ADDRESS – Private bus address
6	PA[18]	3–s. output	4 mA	PRIVATE ADDRESS – Private bus address
7	PA[17]	3–s. output	4 mA	PRIVATE ADDRESS – Private bus address
8	PA[16]	3–s. output	4 mA	PRIVATE ADDRESS – Private bus address
9	PAD[15]	I/O	4 mA	PRIVATE ADDRESS/DATA – Multiplexed Address/Data
10	PAD[14]	I/O	4 mA	PRIVATE ADDRESS/DATA – Multiplexed Address/Data
11	PAD[13]	I/O	4 mA	PRIVATE ADDRESS/DATA – Multiplexed Address/Data
12	PAD[12]	I/O	4 mA	PRIVATE ADDRESS/DATA – Multiplexed Address/Data
13	PAD[11]	I/O	4 mA	PRIVATE ADDRESS/DATA – Multiplexed Address/Data
14	PAD[10]	I/O	4 mA	PRIVATE ADDRESS/DATA – Multiplexed Address/Data
15	PAD[9]	I/O	4 mA	PRIVATE ADDRESS/DATA – Multiplexed Address/Data
16	VDD	Supply		Supply voltage +5 V – Core
17	n.c.	Input		Unused
18	VDD	Supply		Supply voltage +5 V – Periphery
19	PAD[8]	I/O	4 mA	PRIVATE ADDRESS/DATA – Multiplexed Address/Data
20	VSS	Supply		System ground 0 V – Periphery
21	VSS	Supply		System ground 0 V – Core
22	BRQn	Output	2 mA	BUS REQUEST – Bus access request
23	BGNTn	Input		BUS GRANT – Bus access grant
24	PAD[7]	I/O	4 mA	PRIVATE ADDRESS/DATA – Multiplexed Address/Data
25	PAD[6]	I/O	4 mA	PRIVATE ADDRESS/DATA – Multiplexed Address/Data
26	PAD[5]	I/O	4 mA	PRIVATE ADDRESS/DATA – Multiplexed Address/Data
27	n.c.	Input		Unused
28	n.c.	Input		Unused
29	n.c.	Input		Unused
30	n.c.	Input		Unused
31	PAD[4]	I/O	4 mA	PRIVATE ADDRESS/DATA – Multiplexed Address/Data
32	PAD[3]	I/O	4 mA	PRIVATE ADDRESS/DATA – Multiplexed Address/Data
33	PAD[2]	I/O	4 mA	PRIVATE ADDRESS/DATA – Multiplexed Address/Data
34	PAD[1]	I/O	4 mA	PRIVATE ADDRESS/DATA – Multiplexed Address/Data
35	PAD[0]	I/O	4 mA	PRIVATE ADDRESS/DATA – Multiplexed Address/Data
36	TEN	Output	2 mA	TRANSMIT ENABLE – Transmitter validation
37	TXD	Output	2 mA	SERIAL DATA OUT
38	Reserved	Output	2 mA	Reserved (TEN2 in the first generation)
39	RTS	Output	2 mA	REQUEST TO SEND
40	CTS	Input		CLEAR TO SEND
41	TXER	Input		TRANSMIT ERROR – Error on transmitter
42	Reserved	Input		Reserved (TXER2 in the first generation)
43	VDD	Supply		Supply voltage +5 V – Core
44	TXCK	I/O	2 mA	TRANSMIT CLOCK
45	VDD	Supply		Supply voltage +5 v – Periphery
46	CKIN	Input		CLOCK INPUT – Basic clock

Table 2.2 – FULLFIP2 pin description – MQFP100 package

No.	Pin	Type	Io max	Description
47	MCK	Output	2 mA	MASTER CLOCK – Main clock output
48	VSS	Supply		System ground 0 V – Periphery
49	RXD	Input		SERIAL DATA IN
50	CDn	Input		CARRIER DETECT
51	EXTCK	Pulldown input		EXTERNAL TEST CLOCK – External test clock selection
52	n.c.	Input		Unused
53	n.c.	Input		Unused
54	n.c.	Input		Unused
55	RWn	Input		READ/WRITE – Read/Write selection on system bus
56	CSn	Input		CHIP SELECT
57	Reserved	Input		Reserved – (DSn in the first generation)
58	UDAT[0]	I/O	4 mA	USER DATA – System bus data
59	UDAT[1]	I/O	4 mA	USER DATA – System bus data
60	UDAT[2]	I/O	4 mA	USER DATA – System bus data
61	UDAT[3]	I/O	4 mA	USER DATA – System bus data
62	UDAT[4]	I/O	4 mA	USER DATA – System bus data
63	UDAT[5]	I/O	4 mA	USER DATA – System bus data
64	UDAT[6]	I/O	4 mA	USER DATA – System bus data
65	UDAT[7]	I/O	4 mA	USER DATA – System bus data
66	VSS	Supply		System ground 0 V – Core
67	n.c.	Input		Unused
68	UA[0]	Input		USER ADDRESS – System bus address
69	UA[1]	Input		USER ADDRESS – System bus address
70	UA[2]	Input		USER ADDRESS – System bus address
71	VSS	Supply		System ground 0 V – Core
72	IRQn	Output	2 mA	INTERRUPT REQUEST
73	DTACKn	3–s. output	2 mA	DATA ACKNOWLEDGE – Access acknowledge
74	EOC	Output	2 mA	END OF CYCLE – End of Bus Arbitrator cycle
75	BUSY	Output	4 mA	CHIP BUSY – Working transaction
76	MA[0]	3–s. output	4 mA	MICRO_ADDRESS – Microprogram addresss
77	n.c.	Input		Unused
78	n.c.	Input		Unused
79	n.c.	Input		Unused
80	MA[1]	3–s. output	4 mA	MICRO_ADDRESS – Microprogram address
81	MA[2]	3–s. output	4 mA	MICRO_ADDRESS – Microprogram address
82	MA[3]	3–s. output	4 mA	MICRO_ADDRESS – Microprogram address
83	MA[4]	3–s. output	4 mA	MICRO_ADDRESS – Microprogram address
84	MA[5]	3–s. output	4 mA	MICRO_ADDRESS – Microprogram address
85	TSTn[0]	Pullup input		TEST INPUT – Test mode control
86	TSTn[1]	Pullup input		TEST INPUT – Test mode control
87	VDD	Supply		Supply voltage +5 V – Periphery
88	VDD	Supply		Supply voltage +5 V – Core
89	TSTn[2]	Pullup input		TEST INPUT – Test mode control
90	Reserved	3–s. output	2 mA	Reserved – (TSTCK in the first generation)
91	VSS	Supply		System ground 0 V – Periphery
92	MA[6]	3–s. output	2 mA	MICRO_ADDRESS – Microprogram address
93	MA[7]	3–s. output	2 mA	MICRO_ADDRESS – Microprogram address

Table 2.2 – FULLFIP2 pin description – MQFP100 package (continued)

No.	Pin	Type	Io max	Description
94	MA[8]	3–s. output	2 mA	MICRO_ADDRESS – Microprogram address
95	RTSK	3–s. output	2 mA	RUNNING TASK
96	EMAn	Pullup input		ENABLE MICRO_ADDRESS – MA bus validation
97	RESETn	Trigger input		RESET – Circuit initialization
98	WRn	Output	4 mA	WRITE STROBE – Writing signal for private memory
99	RDn	Output	4 mA	READ STROBE – Reading signal for private memory
100	ALE	Output	4 mA	ADDRESS LATCH ENABLE – Address validation

Note 1: FULLFIP2 is designed using CMOS technology ; all input signals are TTL compatible and all ouput signals are CMOS compatible.

Note 2: RESETn is a Schmitt–Trigger input. Initialization of the FULLFIP2 component is performed by keeping RESETn to the low level during 32T (T = 1/CKIN).

Note 3: Internal pullups are implemented on inputs in order to avoid floating input signals but they do not fix a definite input level. It will be then necessary to add external pullup/down elements.

Note 4: The pins PA[19:16] become tri–stated whenever BGNTn is high.

Note 5: All pins of type ’output’, except MCK, become tri–stated whenever TSTn[1] is low.

Table 2.2 – FULLFIP2 pin description – MQFP100 package (continued)

Chapter 3 Functional description

1. MEMORY ACCESS CONTROLLER

1.1. General presentation

The memory access controller is the interface between the core of the FULLFIP2 circuit and the external private memory. It handles three access channels: the A and B channels are under the control of the central unit, the C channel is reserved for the identifier search device of the network manager.

The figure 5 shows the block diagram of the external private memory access controller.

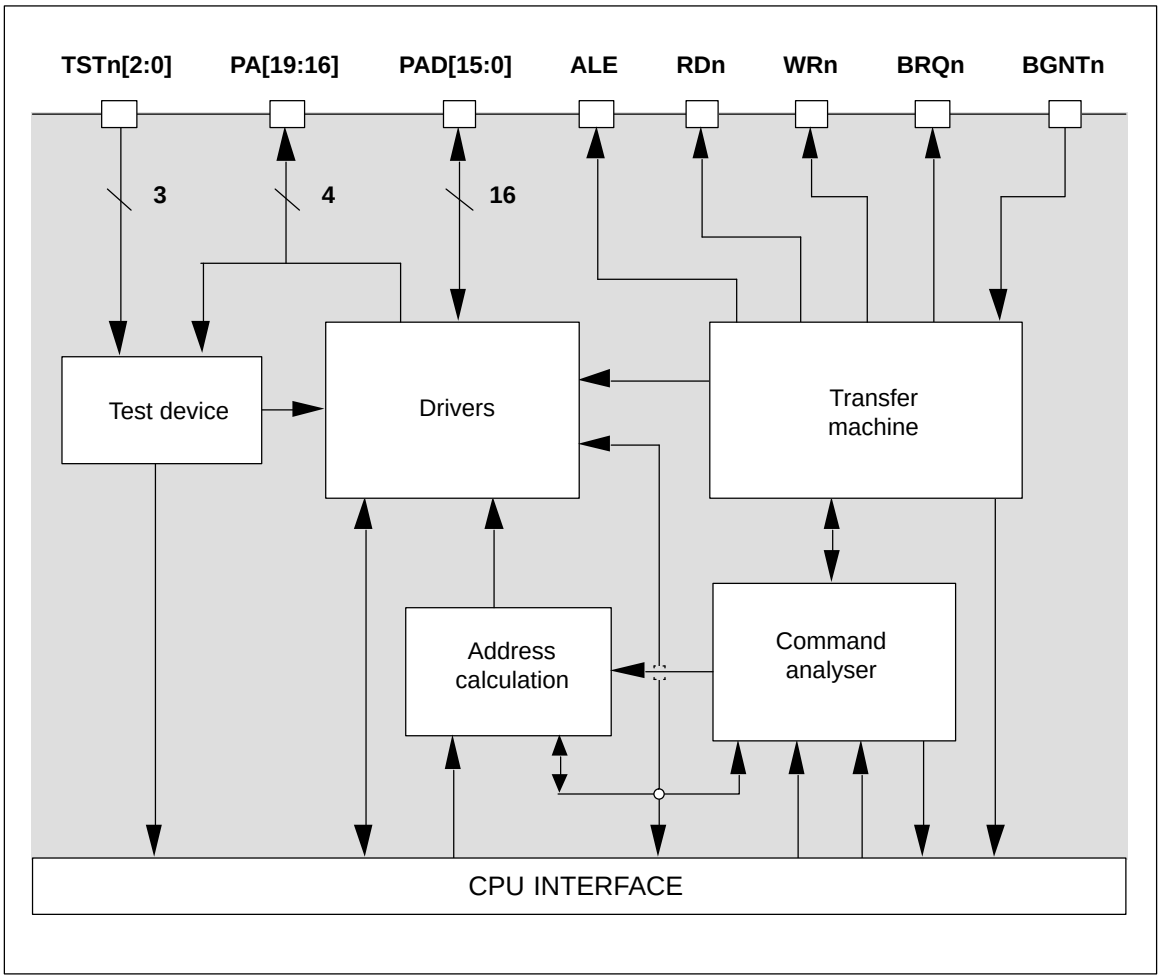


Figure 3.1 – Memory access controller block diagram

1.2. Signal description

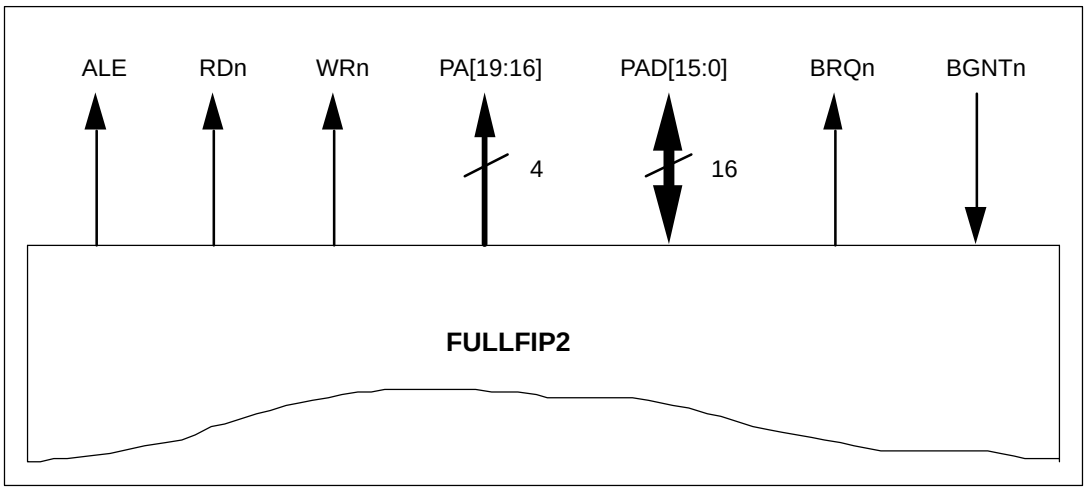


Figure 3.2 – Electrical interface with the memory bus

1.3. Functional model

The external private memory may be sized between 32 Kword and 1 Mword of 16–bit words (external private memory address bus width sized to 20 bits).

The external private memory is used to store :

- the FULLFIP2 microcode (FIPCODE),
- the data base management structures,
- the data base contents.

The external private memory may be composed of RAM memory chip only, but in some implementations, the microcode may be kept permanently in a REPROM memory chip and the remaining information located in RAM memory.

In any case, it is recommended to design the RAM private memory with static RAM chips without wait state for which microcode operating is guaranteed.

The Table 3.1 lists the time access requirements for static RAM or REPROM memory chips.

Basic clock frequency (CKIN input)	Maximum access time for memory chips (static RAM or REPROM)
40 MHz	120 ns
64 MHz	70 ns
80 MHz	55 ns

Table 3.1 – Access time requirements for memory chip

These read/write operations are performed with or without wait state as shown in the Figure 3.3, Figure 3.4, Figure 3.5 and Figure 3.6.

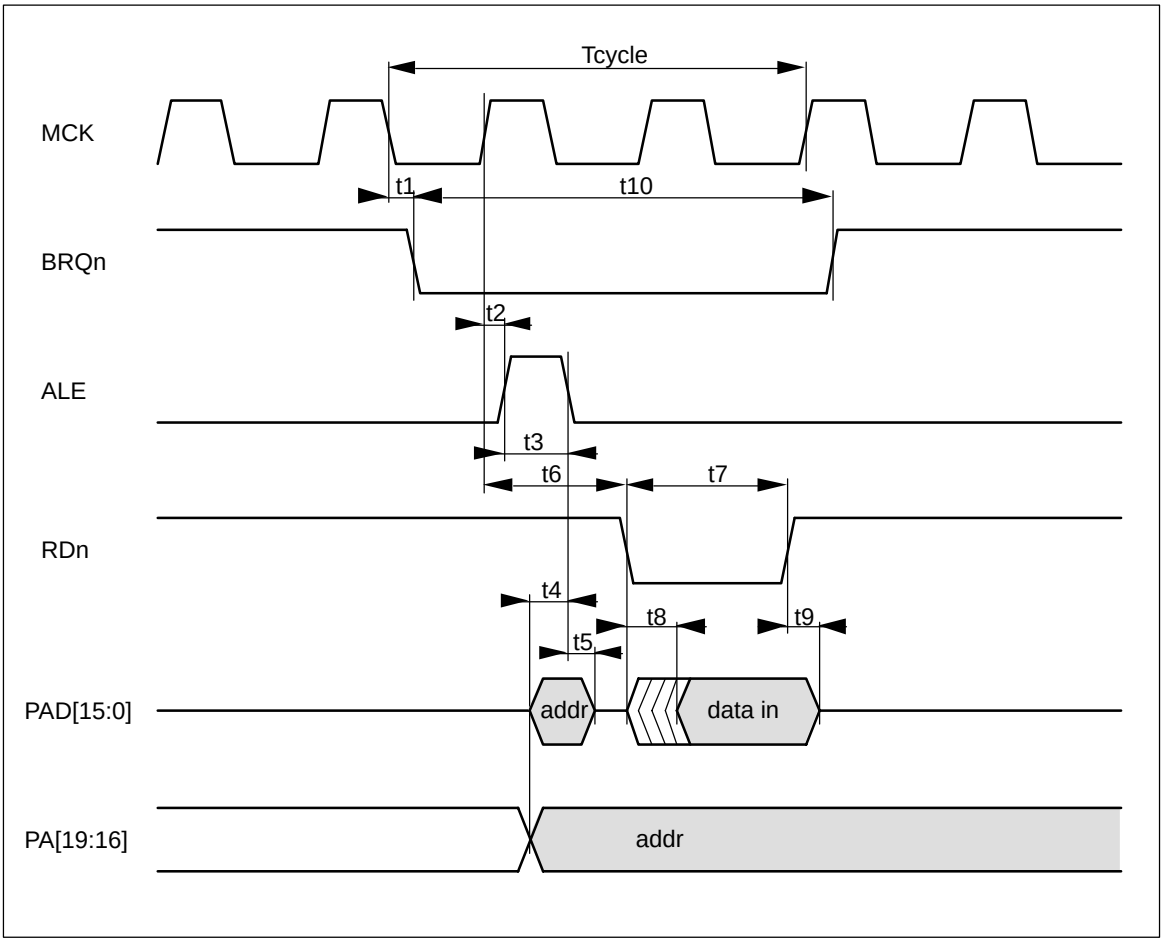
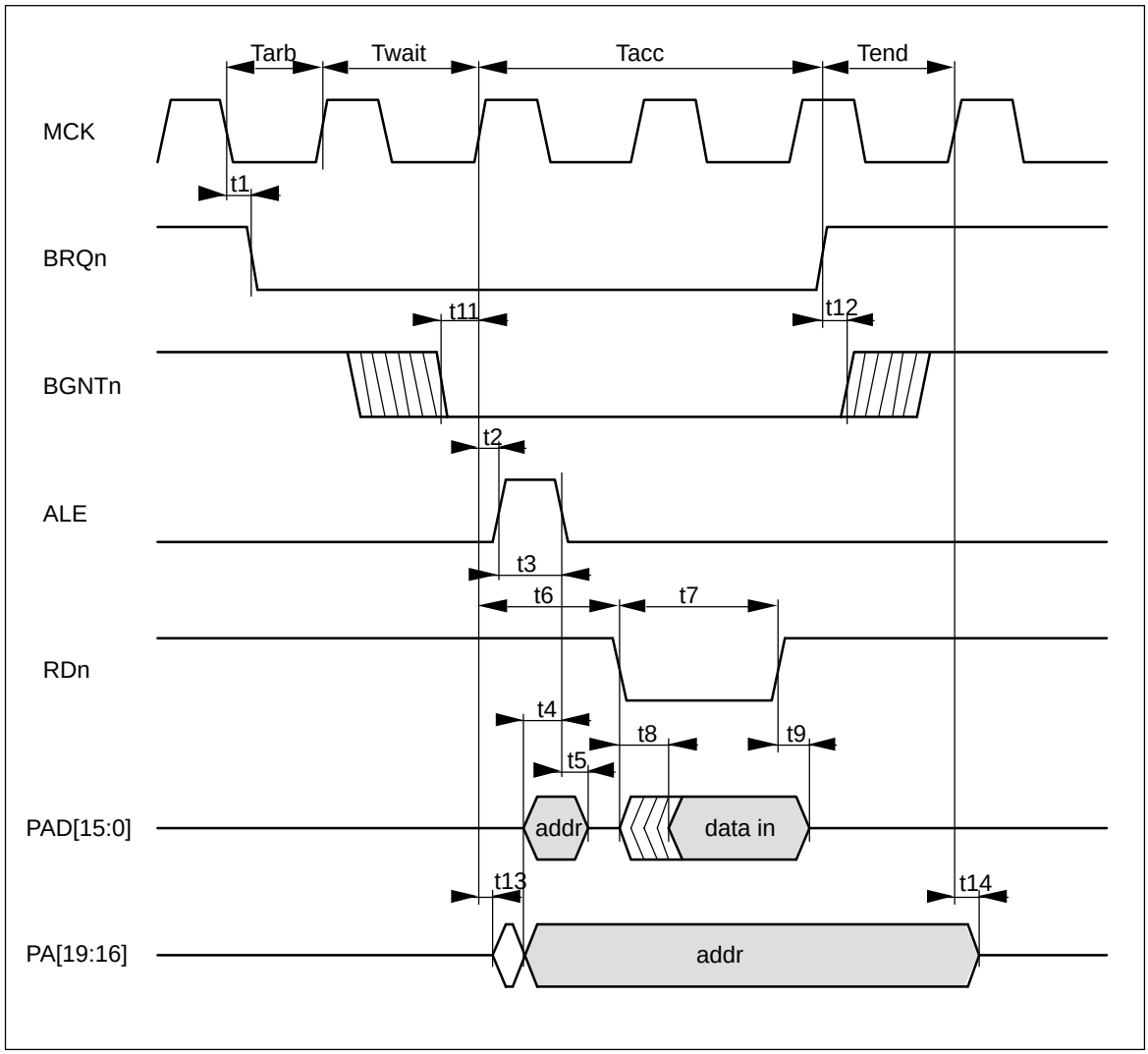


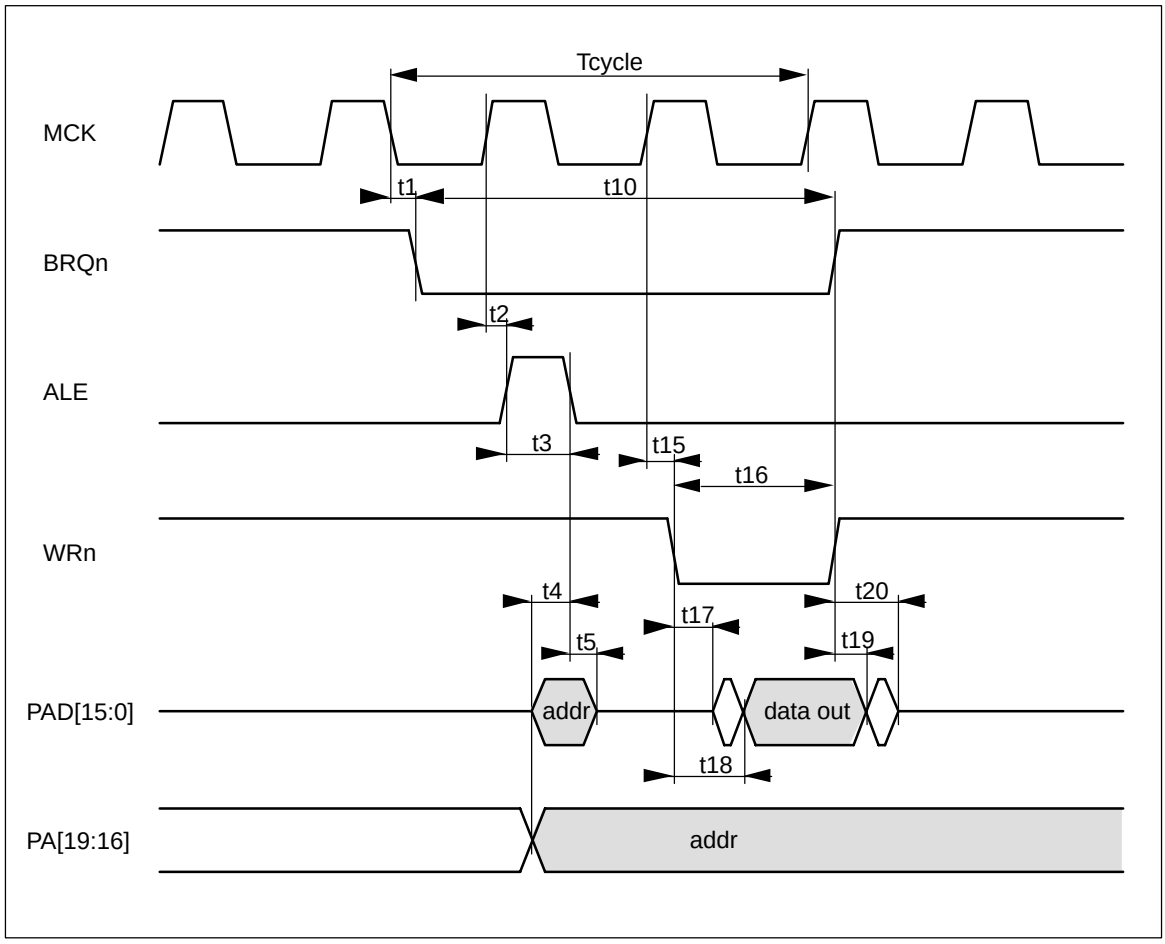
Figure 3.3 – Read cycle from private memory without wait state – Timing diagram

Note 1: BGNTn is permanently low.
Note 2: The MCK period is equal to 5T, the low state to 3T and the high state to 2T.
Note 3: Duration of a read cycle is : Tcycle = 13T
Note 4: T = 25 ns @ CKIN = 40 MHz
15.625 ns @ CKIN = 64 MHz
12.5 ns @ CKIN = 80 MHz



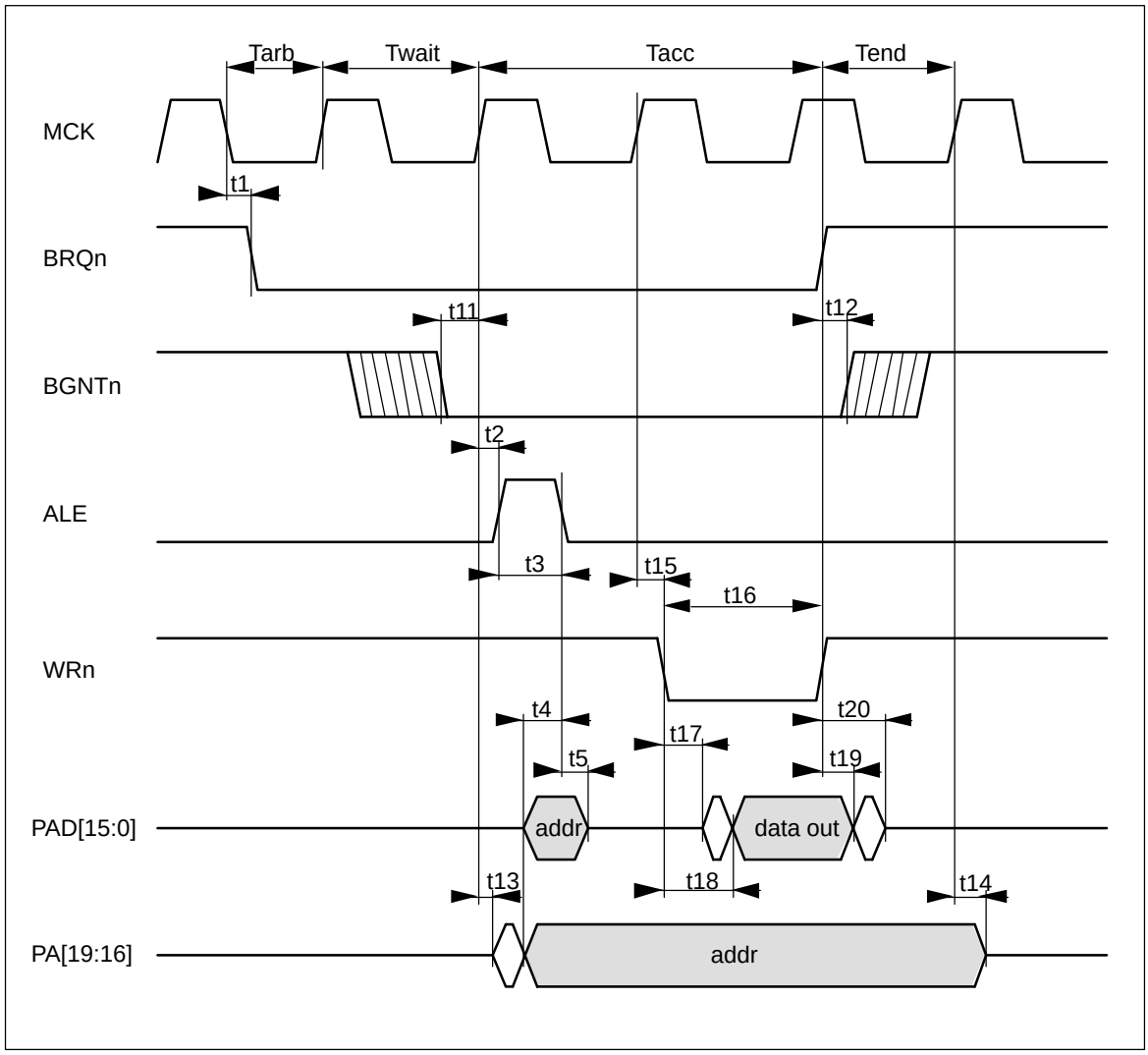
Note 1: The MCK period is equal to 5T, the low state to 3T and the high state to 2T.
Note 2: Duration of a read cycle is :
Tcycle = Tarb + *n* x Twait + Tacc + Tend
where *n* is the number of wait states
Tarb = 3T
Twait = 5T
Tacc = 11T
Tend = 4T
In other words, Tcycle = 18T + *n* x 5T
Note 3: T = 25 ns @ CKIN = 40 MHz
15.625 ns @ CKIN = 64 MHz
12.5 ns @ CKIN = 80 MHz

Figure 3.4 – Read cycle from private memory with wait state – Timing diagram



Note 1: BGNTn is permanently low.
Note 2: The MCK period is equal to 5T, the low state to 3T and the high state to 2T.
Note 3: Duration of a write cycle is : Tcycle = 13T
Note 4: T = 25 ns @ CKIN = 40 MHz
15.625 ns @ CKIN = 64 MHz
12.5 ns @ CKIN = 80 MHz

Figure 3.5 – Write cycle in private memory without wait state – Timing diagram



Note 1: The MCK period is equal to 5T, the low state to 3T and the high state to 2T.
Note 2: Duration of a read cycle is :
Tcycle = Tarb + *n* x Twait + Tacc + Tend
where *n* is the number of wait states
Tarb = 3T
Twait = 5T
Tacc = 11T
Tend = 4T
In other words,
Tcycle = 18T + *n* x 5T
Note 3: T = 25 ns @ CKIN = 40 MHz
15.625 ns @ CKIN = 64 MHz
12.5 ns @ CKIN = 80 MHz

Figure 3.6 – Write cycle in private memory with wait state – Timing diagram

Symbol	Description	Min	Max
t1	BRQn active delay	– 2 ns	15 ns
t2	ALE active delay	– 2 ns	8 ns
t3	ALE pulse width	2T – 5 ns	2T + 5 ns
t4	Address valid to ALE low	2T – 10 ns	
t5	ALE low to Address hold	2 ns	
t6	Read active delay	3T – 2 ns	3T + 8 ns
t7	Read pulse width	5T – 5ns	5T + 5 ns
t8	Read active to data valid		3T – 7 ns
t9	Data hold after read	0 ns	
t10	Read or write cycle time	13T – 5 ns	13T + 5 ns
t11	BGNTn active setup time	T + 5 ns	
t12	BRQn to BGNTn hold time	0 ns	2T
t13	PA[19:16] low Z delay	– 2 ns	5 ns
t14	PA[19:16] high Z delay	– 5 ns	3 ns
t15	Write active delay	– 2 ns	8 ns
t16	Write pulse width	5T – 5 ns	5T + 5 ns
t17	Write active to PAD[15:0] low Z	0 ns	12 ns
t18	Write active to data valid	0 ns	T + 12 ns
t19	Data hold after write	4 ns	
t20	Write inactive to PAD[15:0] high Z	T – 5 ns	T + 5 ns

Note 1: T = 25 ns @ CKIN = 40 MHz
15.625 ns @ CKIN = 64 MHz
12.5 ns @ CKIN = 80 MHz
Note 2: Output load on PA[19:16], PAD[15:0], ALE, BRQn, WRn, RDn: 30 pF

Table 3.2 – Read & write cycle in private memory – Timing values

2. USER SYSTEM INTERFACE

2.1. General presentation

The data transfer between the circuit and the user processor is handled using an usual asynchronous protocol. The transfer requests are activated by CSn. The circuit sends an acknowledge by DTACKn for transfer completion. The transfers are performed byte after byte.

The circuit is seen by the user processor as a collection of registers which can be selected by the UA[2:0] address bus and the RWn read/write signal.

2.2. Signal description

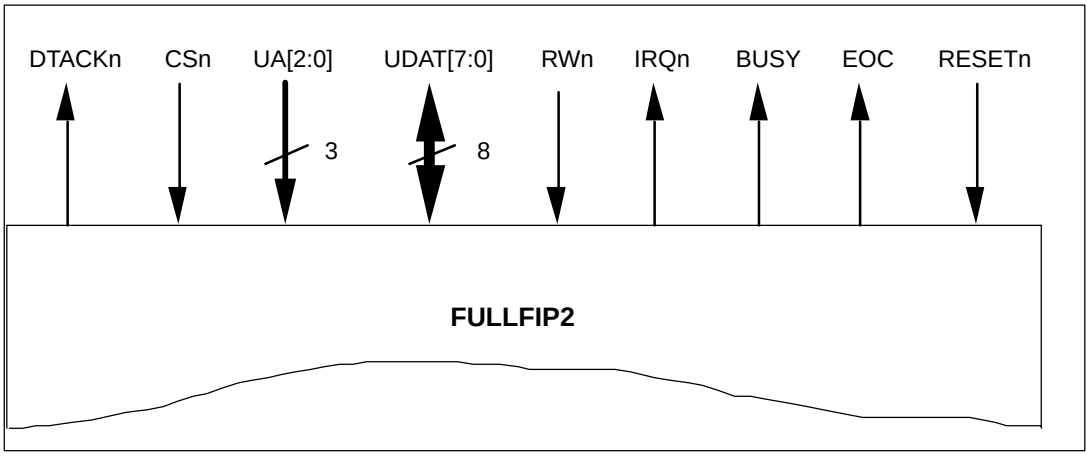


Figure 3.7 – Electrical interface with the user system bus

2.3. Functional model

The circuit model as seen by the user may be summarized as a set of 6 write registers, 4 read registers and a ’bidirectional’ FIFO capable of beeing programmed either in read mode or in write mode. At a given time the FIFO is unidirectional.

Presentation of this functional model is given in the Figure 3.8.

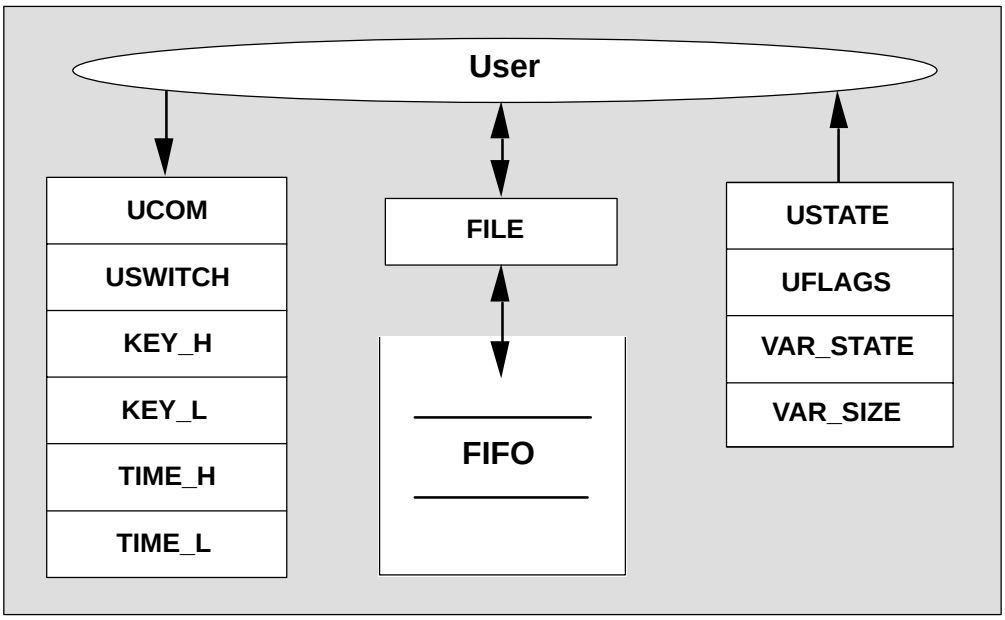


Figure 3.8 – Functional model of the user system interface

The registers are selected by UA[2:0] as shown in the Table 3.3.

UA[2:0]	RWn	Status registers	RWn	Command registers
0 0 0 b	1	USTATE	0	UCOM
0 0 1 b	1	UFLAGS	0	USWITCH
0 1 0 b	1	VAR_STATE	0	KEY_H
0 1 1 b	1	VAR_SIZE	0	KEY_L
1 0 0 b	1	Unused	0	TIME_H
1 0 1 b	1	Unused	0	TIME_L
1 1 0 b	1	Unused	0	Unused
1 1 1 b	1	FILE	0	FILE

Table 3.3 – Register selector

The registers are monodirectional: they are defined either in read mode or in write mode. Some registers are grouped together two by two in order to form 16–bit words, that is the case for the KEY and TIME registers.

The TIME_L and TIME_H registers are used in order to modify the value of the internal real–time counter which permits to synchronize the time managed by the circuit from the user time. The internal time is encoded with 16 bits, the elementary time period is programmable between 0.1 and 5 ms.

The registers of report are grouped into 2 words (USTATE and UFLAGS) which represent the global status of the circuit and the statuses of a variable. This latter one is valid only when a variable has been selected.

The USTATE register groups all the booleans which represent the global status of the interface as, for instance, the BUSY, EOC and IRQn signals.

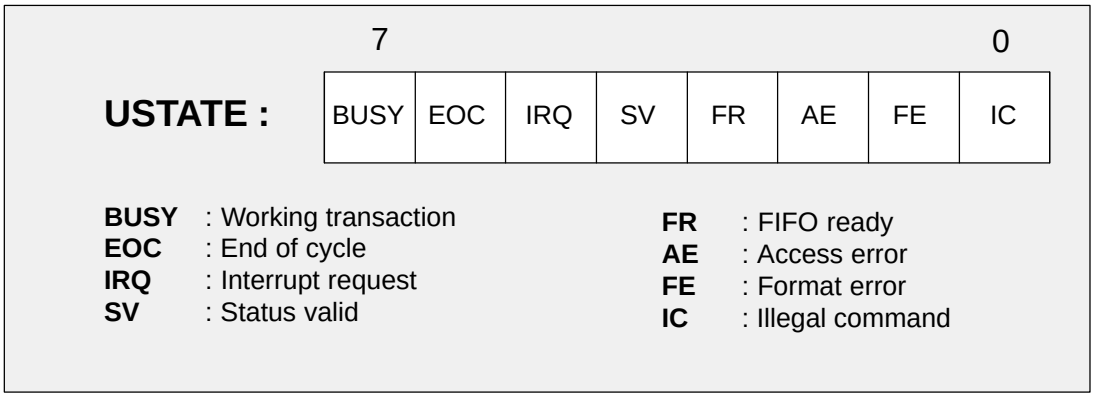


Figure 3.9 – Format of the USTATE register

The UFLAGS register is exclusively updated by the internal program in relation with the objects configured in the external memory of the FULLFIP2.

The VAR_STATE register groups together the statuses inherent to a transaction on a variable identified or not by the circuit. A transaction can be either a set of reads or a set of writes concerning the same communication variable.

The VAR_SIZE register contains the configured size of the processed object. It may concern either the exact number of bytes the user must write or the maximum number of bytes he can read or write, depending on the circumstances.

The user may access to a variable only within a transaction. A transaction is composed of three phases that are ’opening’, ’access to a variable’ and ’closing’.

During the opening phase the FULLFIP2 circuit searches the local data base for the variable and assign a DMA channel between the system interface and the private memory. This channel is used during all the access phase to the variable and is killed when the transaction is closed.

The KEY_L and KEY_H registers allow the user to transmit a 16–bit parameter which defines the object concerned by the transaction. This parameter is generally the access key to the variable.

The user controls the different phases of the transaction by means of 8–bit orders placed into the UCOM command register. The commands identified by the circuit are divided into 3 groups differentiated by their prefix. The prefix encoded with the 3 most significant bits of the command is the only field to be directly identified by the system interface hardware. The remaining part of the command is interpreted by the FULLFIP2 internal microcode. According to the program some commands may be not identified: in this case an error code is sent back to the user through the VAR_STATE register.

The system interface monitors the command sequence and prevents the simultaneous opening of several transactions. If an opening command is detected while BUSY is set active then the IC bit of USTATE is set to 1.

Note

This error is persistent until the USTATE register is read.

UCOM[7:5]	Group	Description
0 0 0 b	**CLOSE**	**Closing a transaction**
0 0 1 b **0 1 0 b** **0 1 1 b**	**READ COMMAND**	**Opening a reading transaction**
1 0 0 b **1 0 1 b** **1 1 0 b** **1 1 1 b**	**WRITE COMMAND**	**Opening a writing transaction**

Table 3.4 – Groups of identified commands

The circuit can process up to 96 read type commands and up to 128 write type commands.

The circuit controls the user access to certain registers in order to preserve the data integrity. That can concern the VAR_STATE and VAR_SIZE registers and the FIFO.

The user can read VAR_STATE and VAR_SIZE only within a transaction and only when the SV bit of USTATE is set active. The content of the registers is not significant if these conditions are not met.

The circuit controls the accesses to these registers as follows :

- **Outside a transaction**

  The BUSY and SV bits of USTATE are zero and an access to VAR_STATE and VAR_SIZE causes an error indicated by the AE bit of USTATE.

  Note

  This error is persistent until the USTATE register is read.

  Although there is an error, the content of the selected register is available to the user at the maximum speed of the interface.

- **At the opening of a transaction**

  The BUSY bit is set active but SV is not yet active. In this case, the accesses to VAR_STATE and VAR_SIZE are delayed until the activation of SV. The DTACKn signal is activated only after the register validation. CSn can be desactivated only after DTACKn activation.

- **During a transaction**

  The BUSY and SV bits are set active and the access is performed at the maximum speed of the interface.

  Concerning the FIFO, the user can access to it through the FILE register only within a transaction and only when the FR bit of USTATE is set active. Moreover the accesses to a variable are limited to its configured size. The values read in the registers are not significant and the written values are ignored if these conditions are not met.

  The circuit controls the accesses to the FIFO as follows :

- **Outside a transaction**

  The BUSY and FR bits of USTATE are zero and an access to the FIFO causes an error indicated by the AE bit of USTATE.

Note

This error is persistent until the USTATE register is read.

In read mode, although there is an error, the content of the first byte of the FIFO is available to the user at the maximum speed of the interface.

- **At the opening of a read transaction**

  The BUSY bit is set active but FR is not yet. In this case, the accesses to the FIFO are delayed until the rise of FR. The DTACKn signal is activated only after the internal writing of a byte into the FIFO. CSn can be deactivated only after DTACKn activation.

- **During a write or read transaction**

  If the FR bit is set active the access is performed at the maximum speed of the interface, if not, it is delayed until the FIFO is available again.

  If a size overflow is detected, the FE bit of USTATE is set active and the accesses are ignored. The FE bit shall be reset by the CLOSE command. In read mode the last valid byte is provided to the user without delay whatever the FIFO status.

  If a read is performed after the opening of a write transaction, or if a write is performed after the opening of a read transaction, the AE bit of USTATE is set active and the accesses are ignored.

Note

This error is persistent until the USTATE register is read.

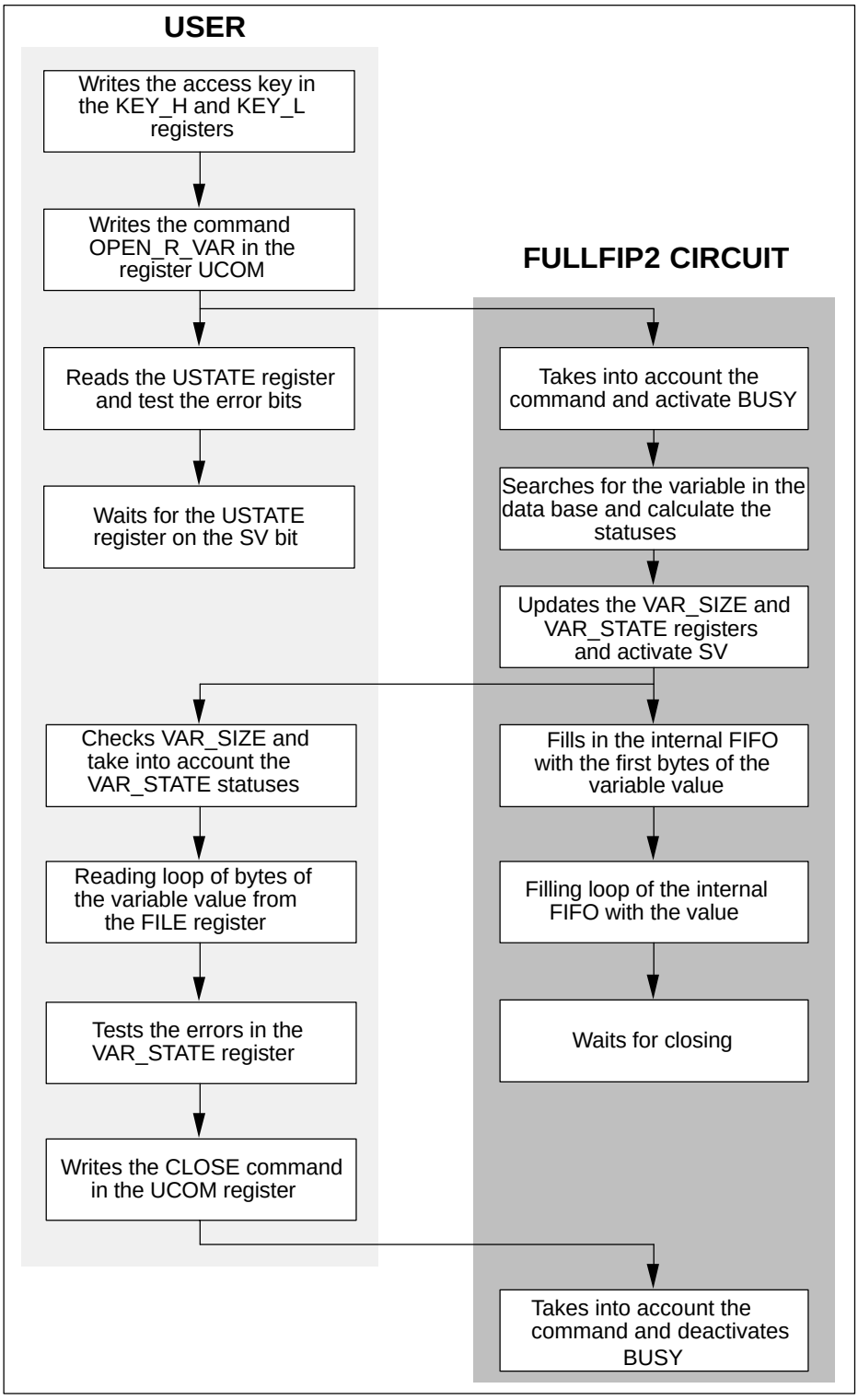


Figure 3.10 – User read transaction

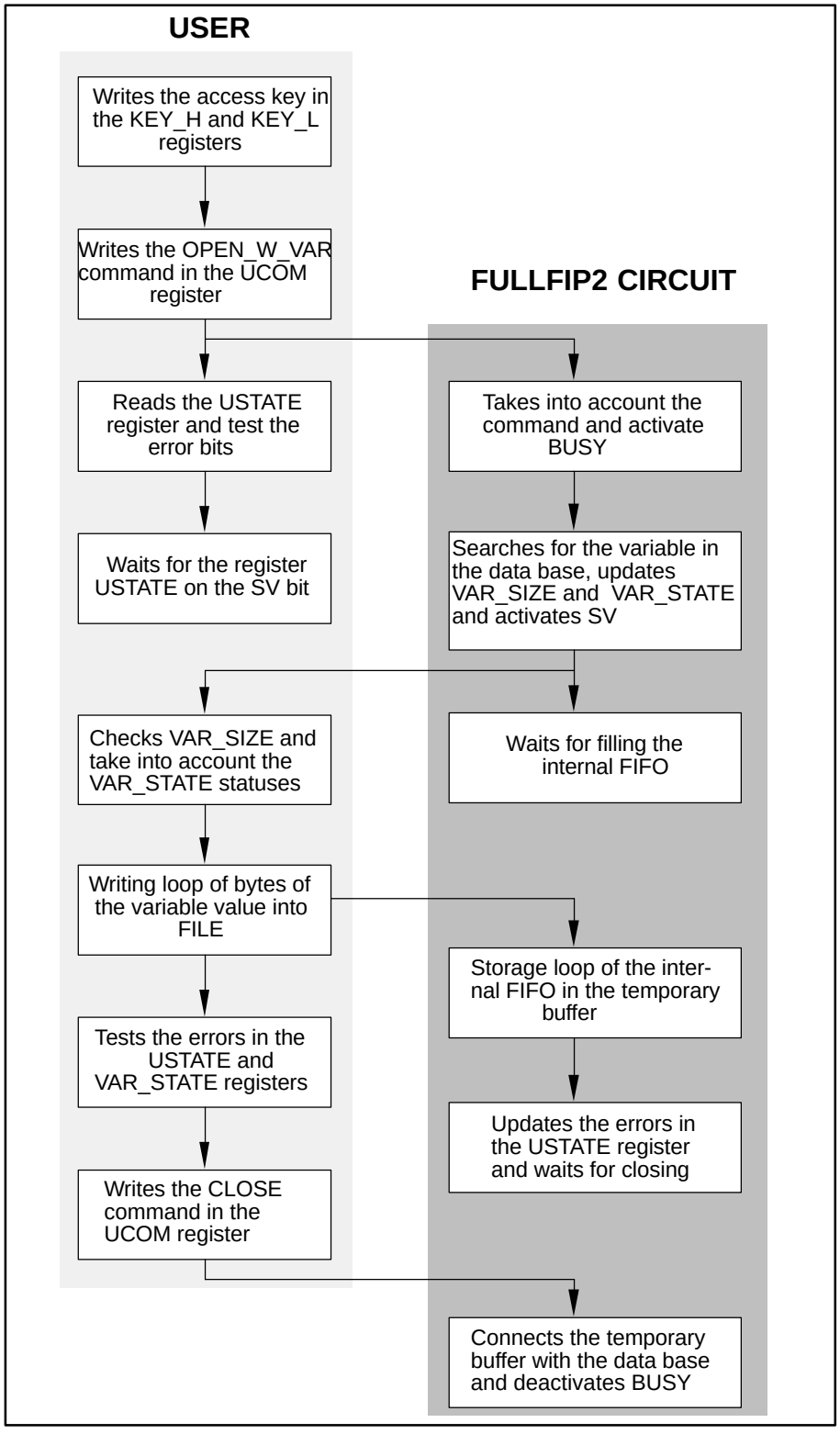


Figure 3.11 – User write transaction

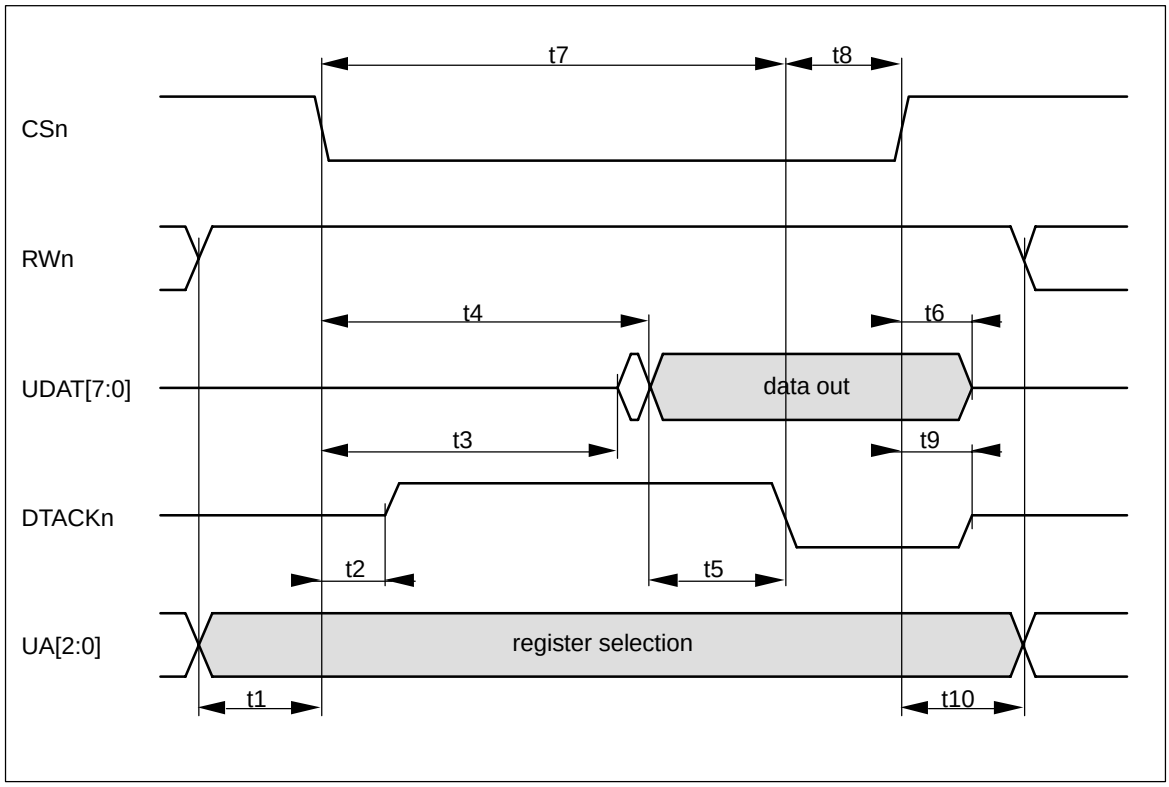


Figure 3.12 – User read cycle – Timing diagram

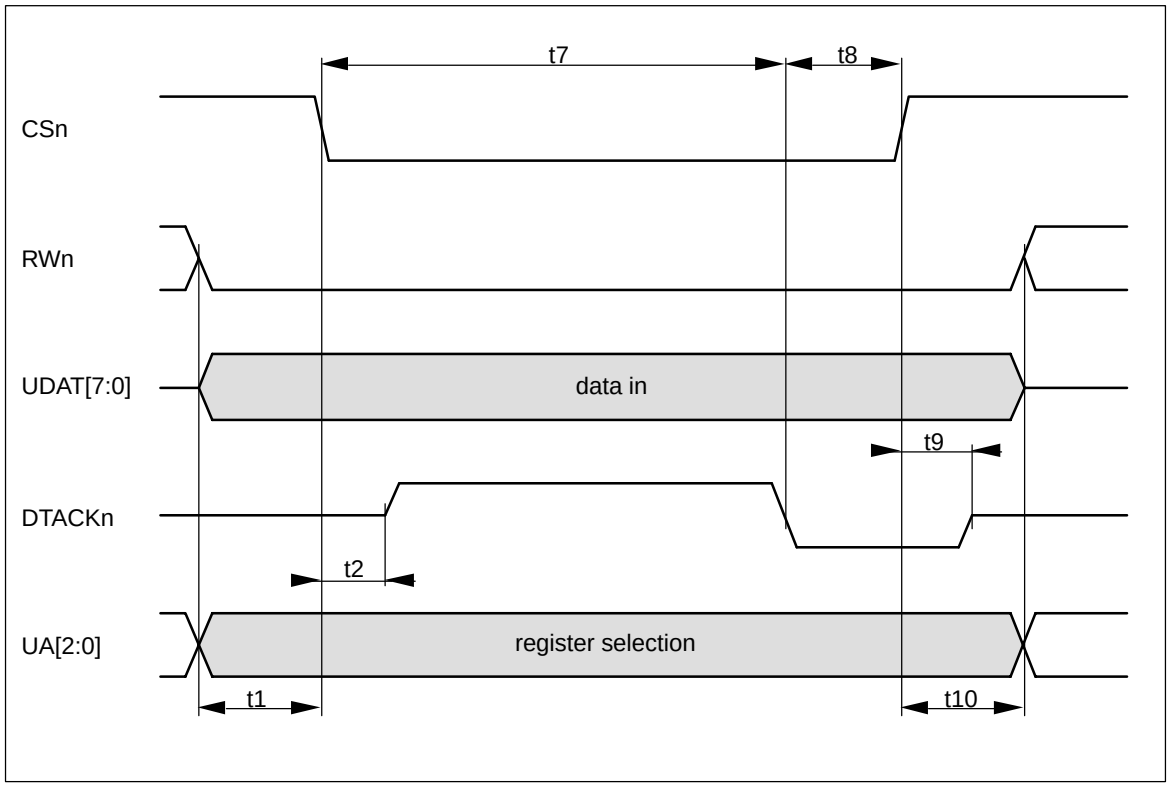


Figure 3.13 – User write cycle – Timing diagram

Symbol	Description	Min	Max
t1	UA[2:0], UDAT[7:0] (in write mode) and RWn hold time to CSn low	5 ns	
t2	CSn low to DTACKn high	0 ns	
t3	CSn low to UDAT[7:0] low Z	0 ns	
t4 (Note 1)	CSn low to UDAT[7:0] valid		8 T + 40 ns (Note 2)
t5	UDAT[7:0] valid to DTACKn low	0 ns	
t6	CSn high to UDAT[7:0] high Z	0 ns	
t7 (Note 1)	CSn low to DTACKn low		8 T + 40 ns (Note 2)
t8	DTACKn low to CSn high	0 ns	
t9	CSn high to DTACKn high Z	0 ns	
t10	UA[2:0], UDAT[7:0] (in write mode) and RWn hold time from CSn high	0 ns	

Note 1: When accessing the FILE, VAR_SIZE or VAR_STATE registers, while these registers are not ready (i.e. access is performed without preliminary polling of the USTATE register), access cycles are delayed until the registers become ready. In this case the above mentionned delay is not guaranteed anymore.
Note 2:T = 25 ns @ CKIN = 40 MHz
15.625 ns @ CKIN = 64 MHz
12.5 ns @ CKIN = 80 MHz
Note 3: DTACKn is tri–stated outside the user access cycles. It must be pulled up externally using a 1–KΩ resistor connected to VDD.
Note 4: Output load on UDAT[7:0], BUSY, EOC, DTACKn, IRQn: 50 pF

Table 3.5 – User read and write cycle – Timing values

3. NETWORK INTERFACE

3.1. General presentation

The network interface provides the transmission and reception functions of the frames and the clock generation. Moreover it relieves the central unit of all the critical time tasks in particular the identifier search, the timer management and the pre–interpretation of the network transaction in receive mode.

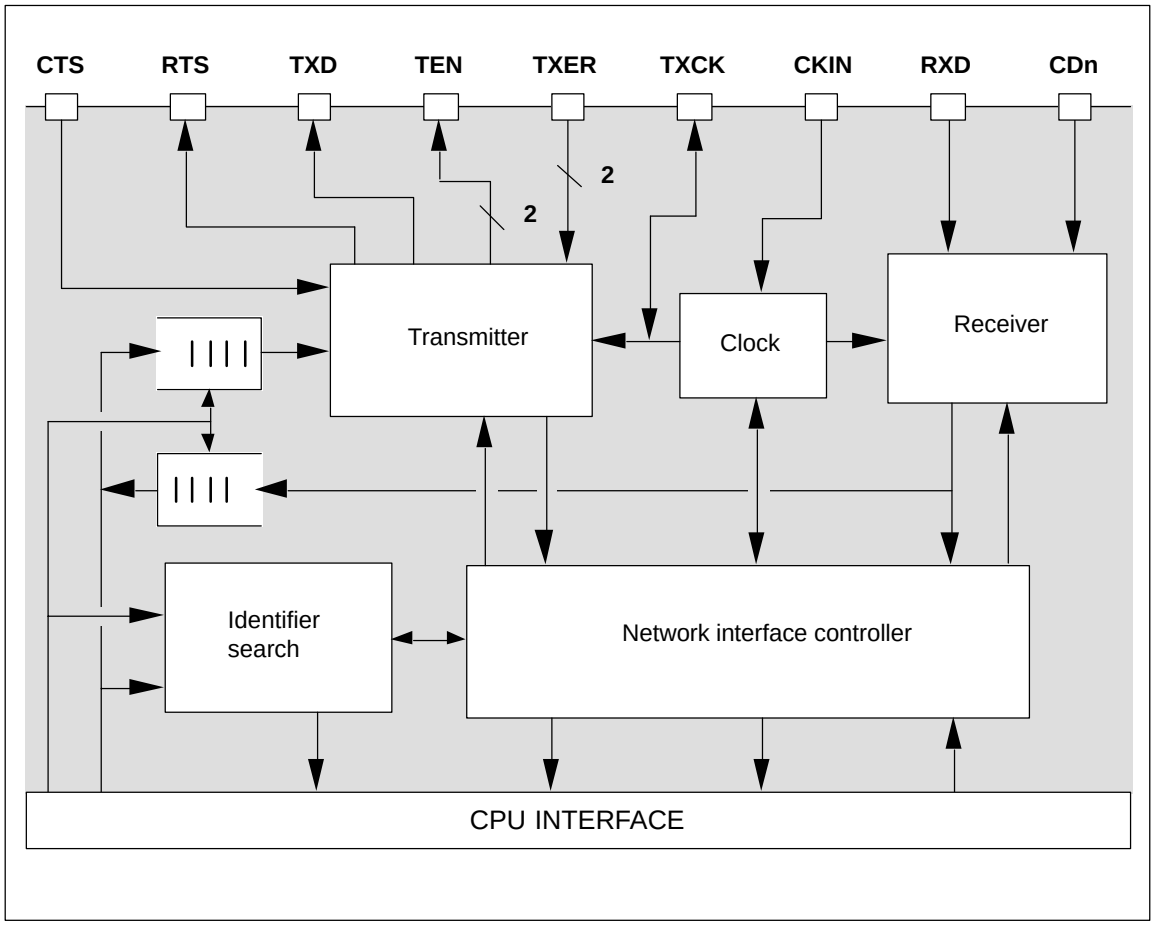


Figure 3.14 – Network interface block diagram

The FULLFIP2 can handle two redundant channels, using an external channel selector such as FIELDUAL.

The transmission is made simultanously on the two channels, and the reception the selected one.

FULLFIP2 manages redundancy management by controlling a channel selector, which is a peripheral on its private bus.

3.2. Signal description

The interface with the line transceiver is composed of the following signals:

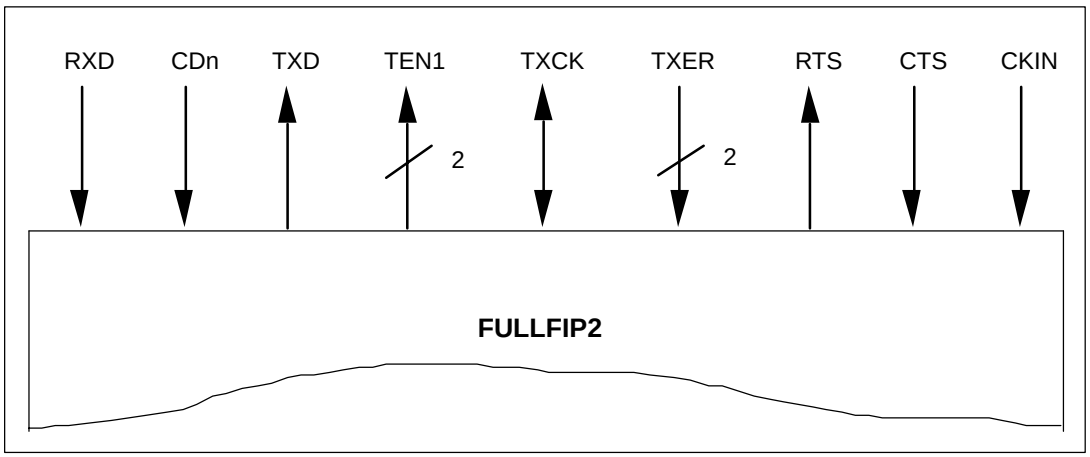


Figure 3.15 – Electrical interface with the line transceiver

3.3. Functional model in transmission

In the transmitter section the signal TEN is designed to validate the bus drivers. This signal is synchronous with the serial Manchester data TXD. The signals RTS and CTS are intended to synchronize the circuit in an external way in specific applications. Within the simplest applications CTS can be connected to VDD and in this case RTS is not connected.

In most applications TXCK is configured by the FULLFIP2 internal microcode as an output that can be used by the line transceiver circuitry such as FIELDRIVE.

For more sophisticated applications the TXCK pin can be programmed as an input or an output which permits to drive the transmitter by means of an external clock.

The signal TXER permits to indicate the errors detected by the line drivers to the circuit. The transmission errors may be due to underloads or overloads on the drivers.

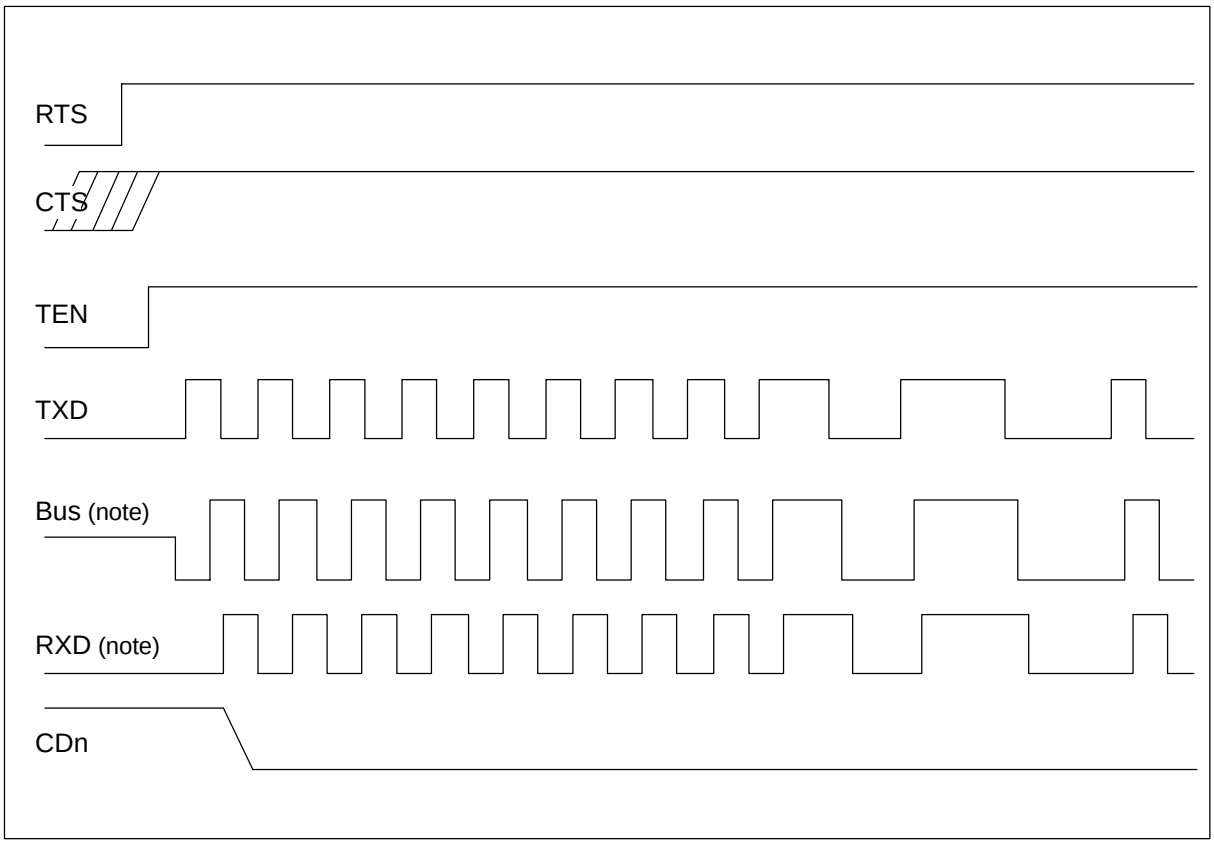


Figure 3.16 – Start of frame (AFNOR/UTE delimiters)

Note: The behavior of the bus signal and the RXD signal depends on the dynamic response of the line transceiver used.

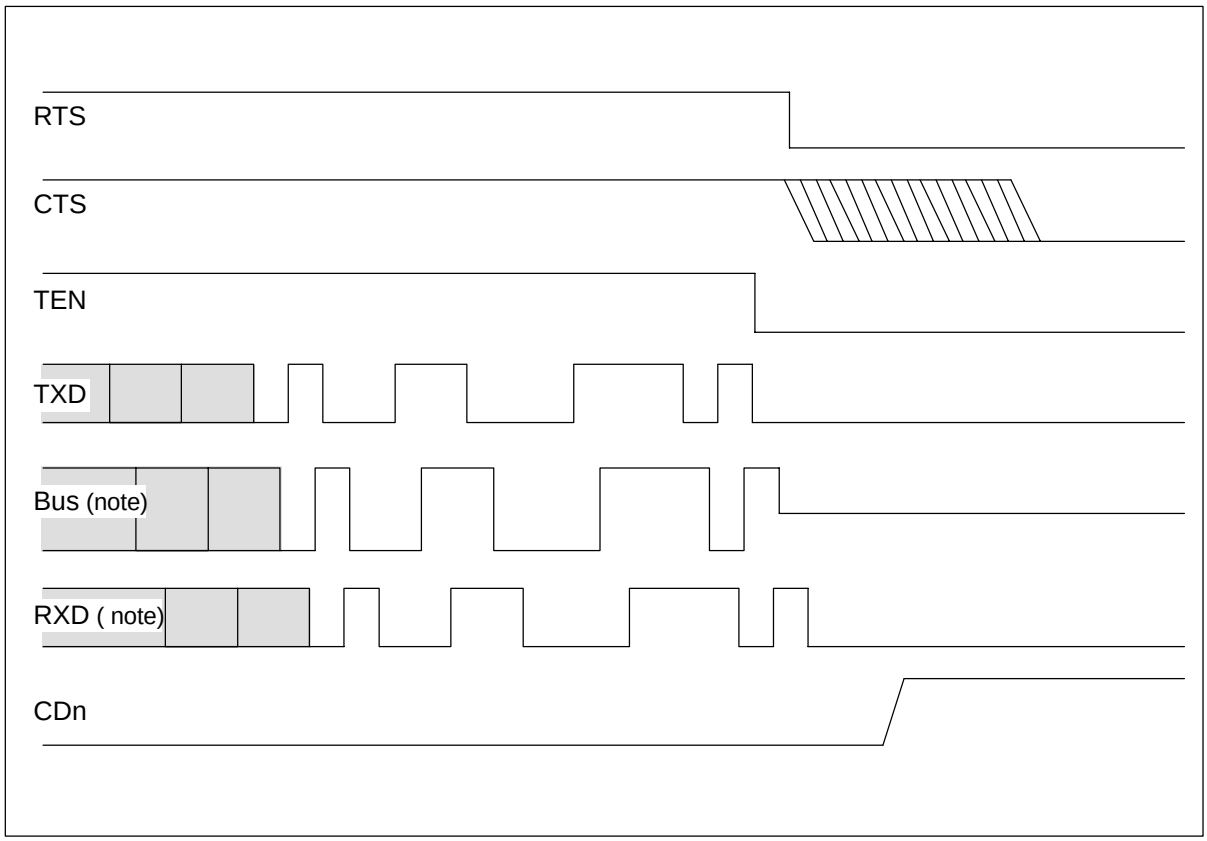
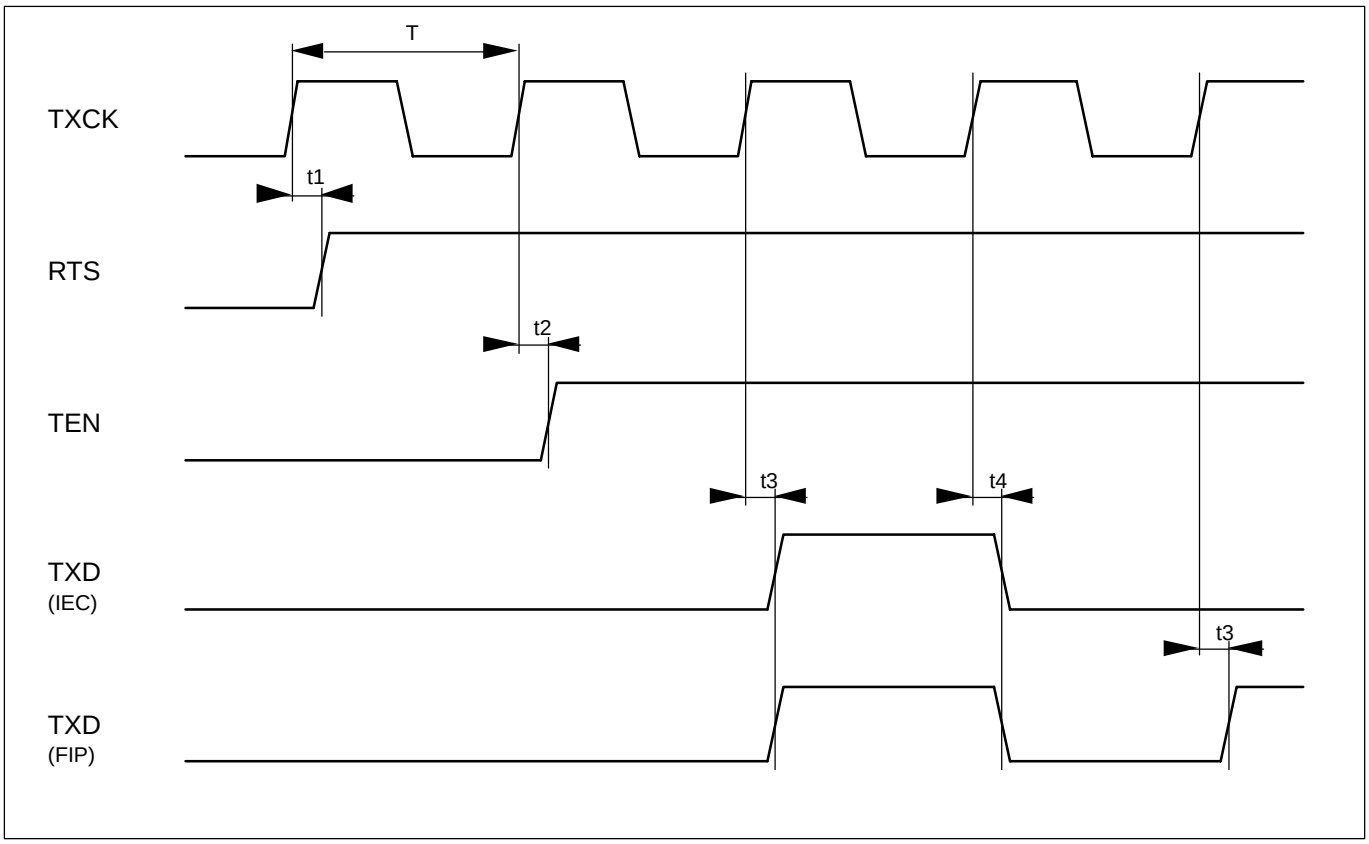


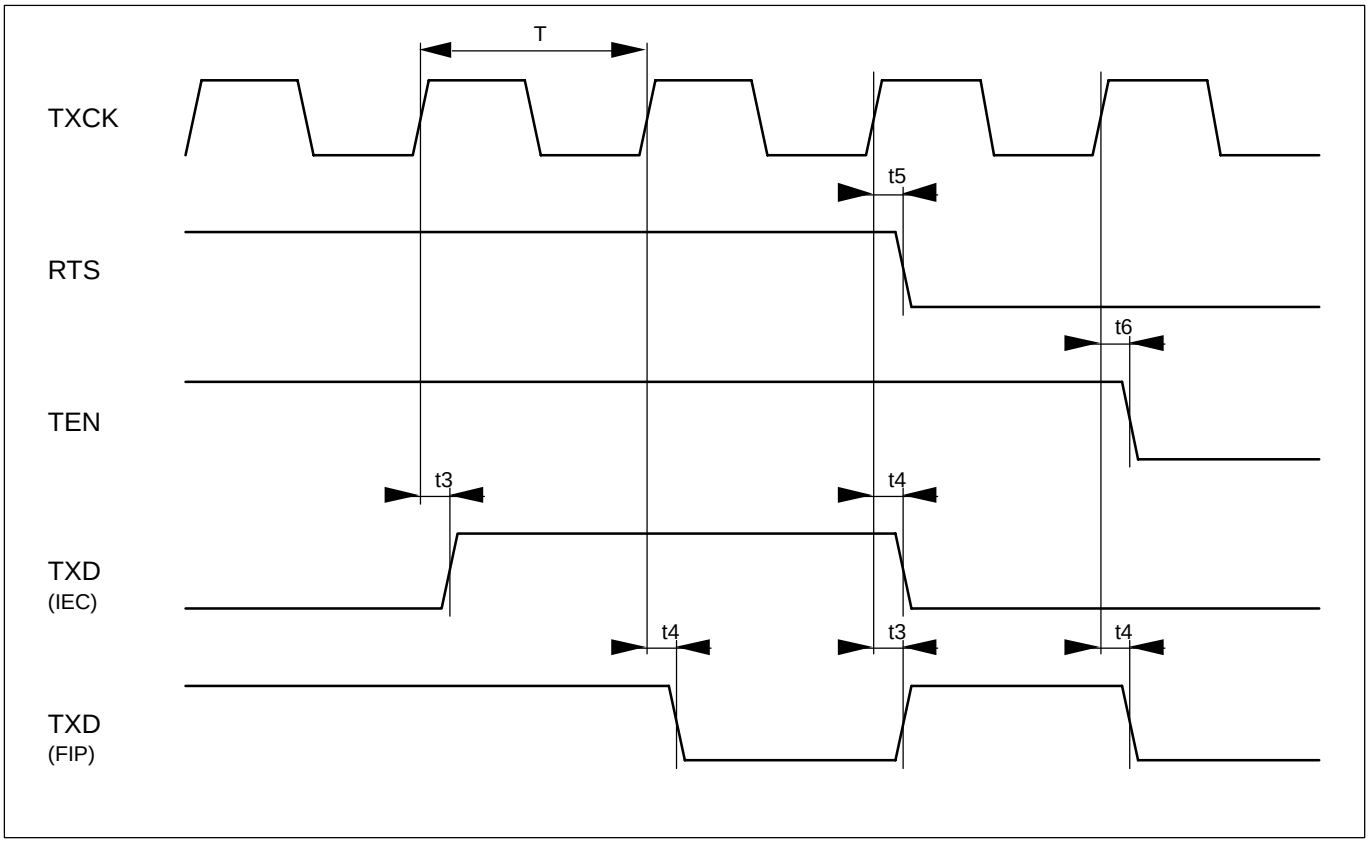
Figure 3.17 – End of frame (AFNOR/UTE delimiters)

Note: The behavior of the bus signal and the RXD signal depends on the dynamic response of the line transceiver used.



Note: T = 16 µs @ Network bitrate = 31.25 Kbit/s
500 ns @ Network bitrate = 1 Mbit/s
200 ns @ Network bitrate = 2.5 Mbit/s
100 ns @ Network bitrate = 5 Mbit/s

Figure 3.18 – Start of Frame – Transmission cycle timing diagram



Note: T = 16 µs @ Network bitrate = 31.25 Kbit/s
500 ns @ Network bitrate = 1 Mbit/s
200 ns @ Network bitrate = 2.5 Mbit/s
100 ns @ Network bitrate = 5 Mbit/s

Figure 3.19 – End of Frame – Transmission cycle timing diagram

Symbol	Description	Min	Max
t1	TXCK high to RTS high	– 10 ns	30 ns
t2	TXCK high to TEN high	– 10 ns	30 ns
t3	TXCK high to TXD high	– 10 ns	30 ns
t4	TXCK high to TXD low	– 10 ns	30 ns
t5	TXCK high to RTS low	– 10 ns	30 ns
t6	TXCK high to TEN low	– 10 ns	30 ns

Note: Output load on RTS, TXD, TEN, TXCK : 50 pF

Table 3.6 – Transmission cycle – Timing values

3.4. Functional model in reception

In the receiver section the input CDn identifies the frame envelope. When CDn is inactive the serial manchester input RXD is ignored. Moreover this carrier detection signal is used for the sequence checking of the frames in order to determine the bus activity.

A received frame is composed of consecutive symbols as represented in the Figure 3.20.

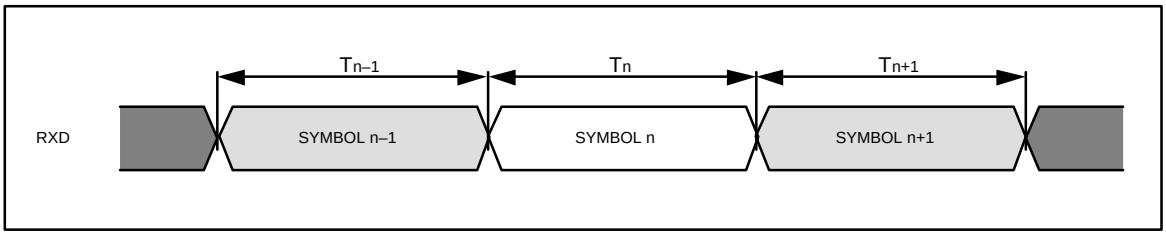


Figure 3.20 – RXD signal timing diagram

Typical duration and shape of a received symbol shall be in accordance with the IEC and AFNOR/UTE communication protocol standards.

Temporal distortion of the symbol ’n’ received at the RXD input is calculated as follows :

$$\textit{Distortion (\%)} = 100 * | T_n - T_{ideal} | / T_{ideal}$$

where T_n : duration of the symbol ’n’ received

T_{ideal} : duration of the ideal symbol

For the FULLFIP2 component, accepted temporal distortion shall not be greater than 15% and accepted jitter on 48 consecutive received bits shall not be greater than 1% whatever the network bitrate.

3.5. Network bitrate, clock signals and timers

The selected network bitrate depends both on the value of the internal programmable 16–bit TIMER_CNT register and the frequency of the basic clock signal driving the FULLFIP2 chip through the CKIN pin as shown in the Table 3.7. The TIMER_CNT register may be configured only by using microcodes.

The maximum frequency of the basic clock signal is limited to 80 MHz in order to guarantee the operation of the entire circuit (worst case condition: VDD = 4.75 V / Tamb = +85 °C). From the basic clock signal, internal clock signals are derived for the central processor unit, the transmitter and receiver circuitry, the line activity timers and the stamping timers.

In transmit mode a clock signal is generated at a frequency double of the bit frequency on the network by the FULLFIP2 circuit when it works in master mode; in this case the TXCK pin is set as output for this signal. When the circuit works in slave mode it receives its transmit clock signal from the outside by the TXCK pin. The operation mode is defined at the system configuration by the microcode.

In receive mode, a clock signal is generated to sample the received signal from the line transceiver.

Internal timers are handled by the transmitter and the receiver circuitry to monitor the line activity and to fix the turn–around time of the station and the network silence time–out.

Internal stamping timers are handled in order to date the events processed by the FULLFIP2 circuit. Internal stamping timers are incremented at every time slot period; the value of the time slot period can be configured only by the FULLFIP2 internal microcode.

Network bitrate	Basic clock frequency (CKIN input)
31.25 Kbit/s	40 MHz
1 Mbit/s	64 MHz
2.5 Mbit/s	80 MHz
5 Mbit/s	80 MHz

Table 3.7 – Basic clock frequency requirement for a selected network bitrate

Chapter 4 Electrical characteristics

Parameter	Comments	Min	Typ	Max	Unit
Absolute supply voltage range		–0.5		6.0	V
Absolute voltage range on input pins		–0.5		VDD + 0.5	V
Storage temperature		–40		+125	°C

Table 4.1 – Absolute maximum ratings (1)

Symbol	Parameter	Comments	Min	Typ	Max	Unit
VDD	Supply voltage range		4.75	5.0	5.25	V
VIH	Input voltage high	Any input except RESETn	2.0		VDD +0.5	V
VIL	Input voltage low	Any input except RESETn	–0.5		0.8	V
VOH	Output voltage high		2.4			V
VOL	Output voltage low				0.4	V
VT–	Schmitt–Trigger negative going threshold	RESETn input	1.2		2.0	V
VT+	Schmitt–Trigger positive going threshold	RESETn input	2.4		3.5	V
CIN, COUT	Input and output pin capacitance	Pad capacitance including package		10		pF
IIN, IOZ	Input and tri–state output leakage current		–10		+10	µA
Base operating frequency (CKIN input)		Network bit rate = 31.25 Kbit/s		40		MHz
		Network bit rate = 1 Mbit/s		64		MHz
		Network bit rate = 2.5 Mbit/s		80		MHz
		Network bit rate = 5 Mbit/s		80		MHz
Normal operating free–air temperature			–40		+85	°C

Table 4.2 – Functional characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Icc	Supply current	CKIN = 40 MHz @ 31.25 Kbit/s		28		mA
		CKIN = 64 MHz @ 1 Mbit/s		43		mA
		CKIN = 80 MHz @ 2.5 Mbit/s		52		mA
		CKIN = 80 MHz @ 5 Mbit/s		52		mA

Table 4.3 – Consumption (2)

1. Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

2. The mean values of the supply current are measured within a typical user application running the FIPCODE microcode.

Chapter 5 Physical dimensions

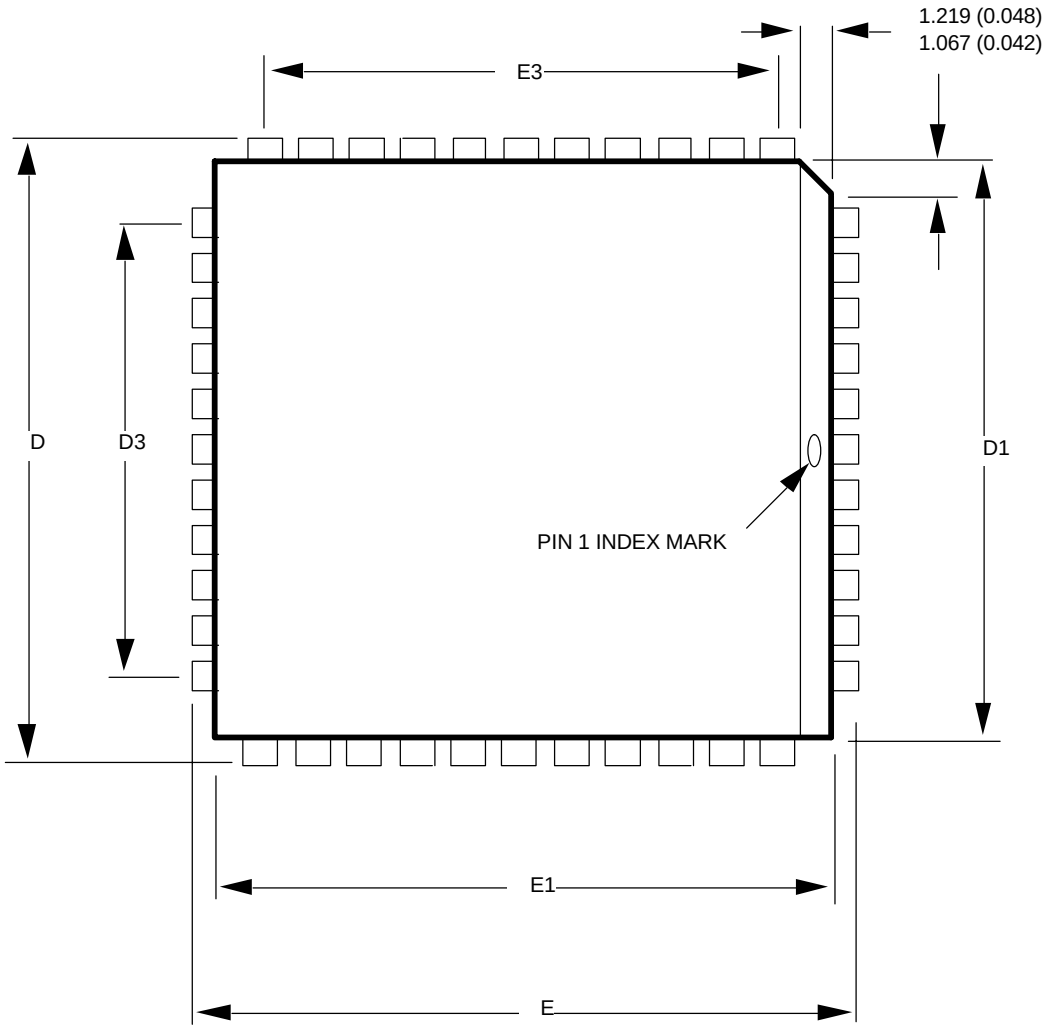


Figure 5.1 – PLCC84 package outlines

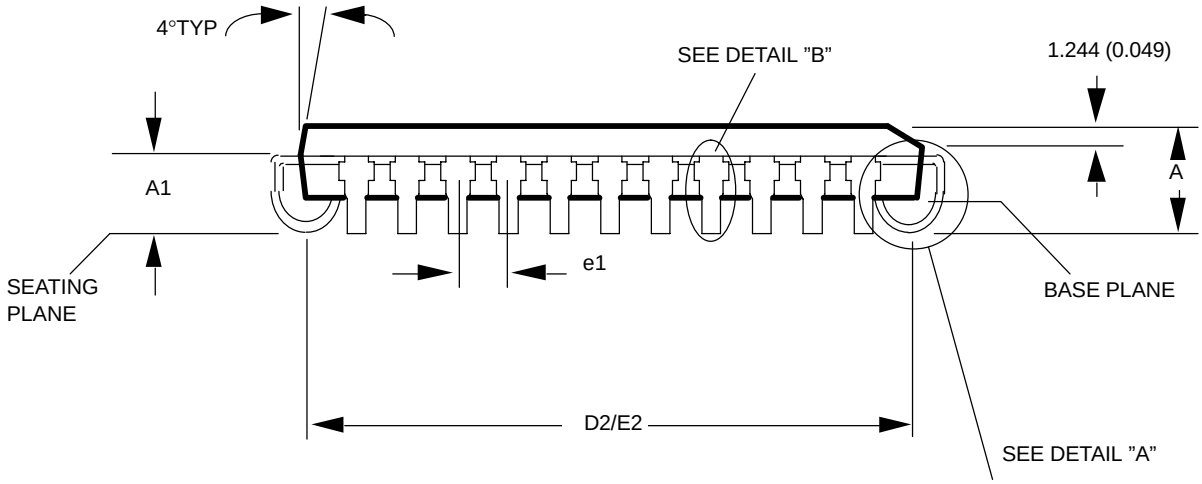


Figure 5.1 – PLCC84 package outlines (continued)

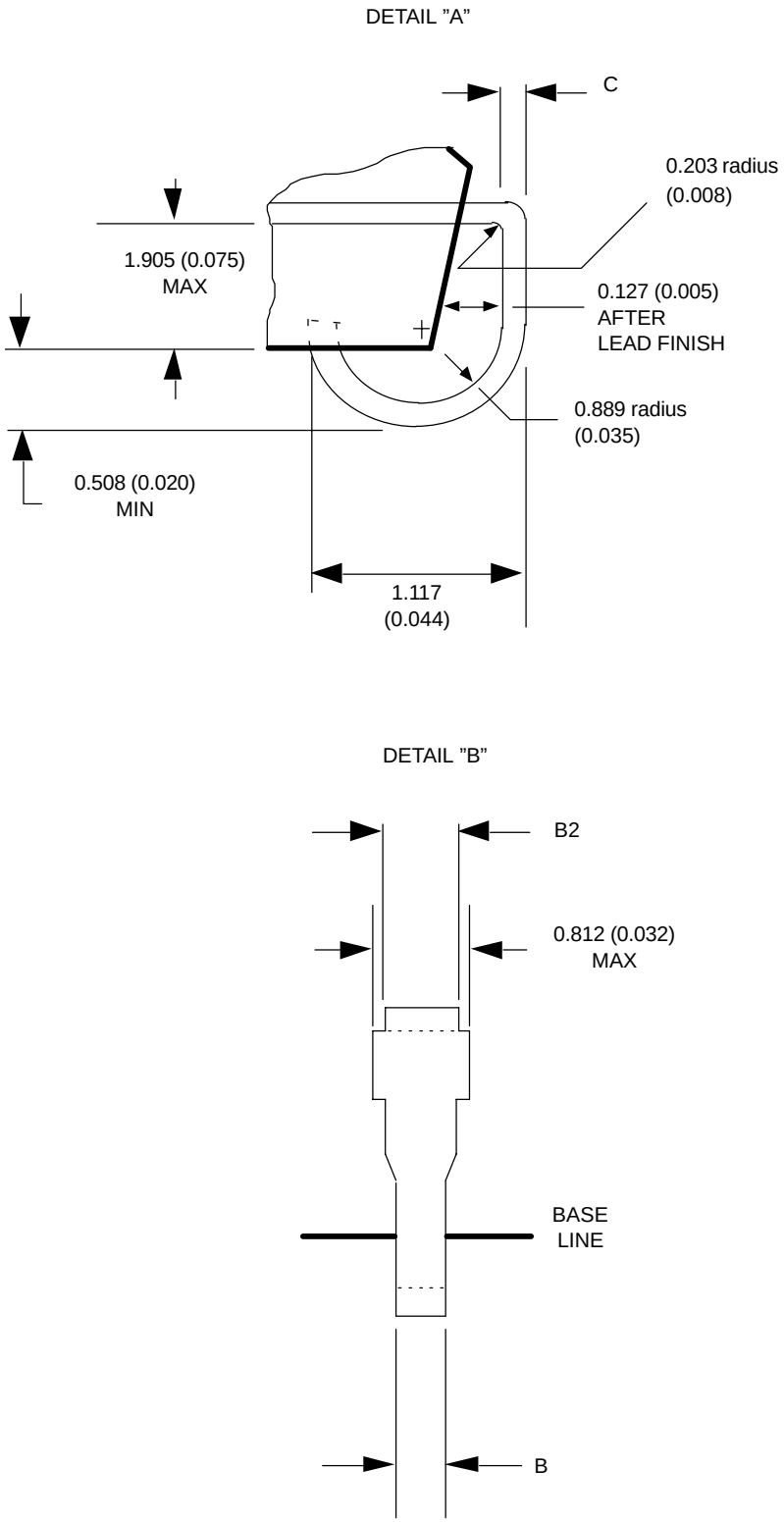


Figure 5.2 – PLCC84 package outlines – Terminal details

SYMBOL	MINIMUM mm (inch)	MAXIMUM mm (inch)
A	4.19 (0.165)	5.08 (0.200)
A1	2.29 (0.090)	3.30 (0.130)
B	0.330 (0.013)	0.533 (0.021)
B2	0.660 (0.026)	0.813 (0.032)
C	0.203 (0.008)	0.254 (0.010)
D	30.10 (1.185)	30.35 (1.195)
D1	29.21 (1.150)	29.41 (1.158)
D2	27.69 (1.090)	28.70 (1.130)
D3	25.40 REF (1.000 REF)	
E	30.10 (1.185)	30.35 (1.195)
E1	29.21 (1.150)	29.41 (1.158)
E2	27.69 (1.090)	28.70 (1.130)
E3	25.40 REF (1.000 REF)	
e1	1.27 TYP (0.050 TYP)	
N	84 pins	
ND	21 pins	
NE	21 pins	

Table 5.1 – PLCC84 package dimensions

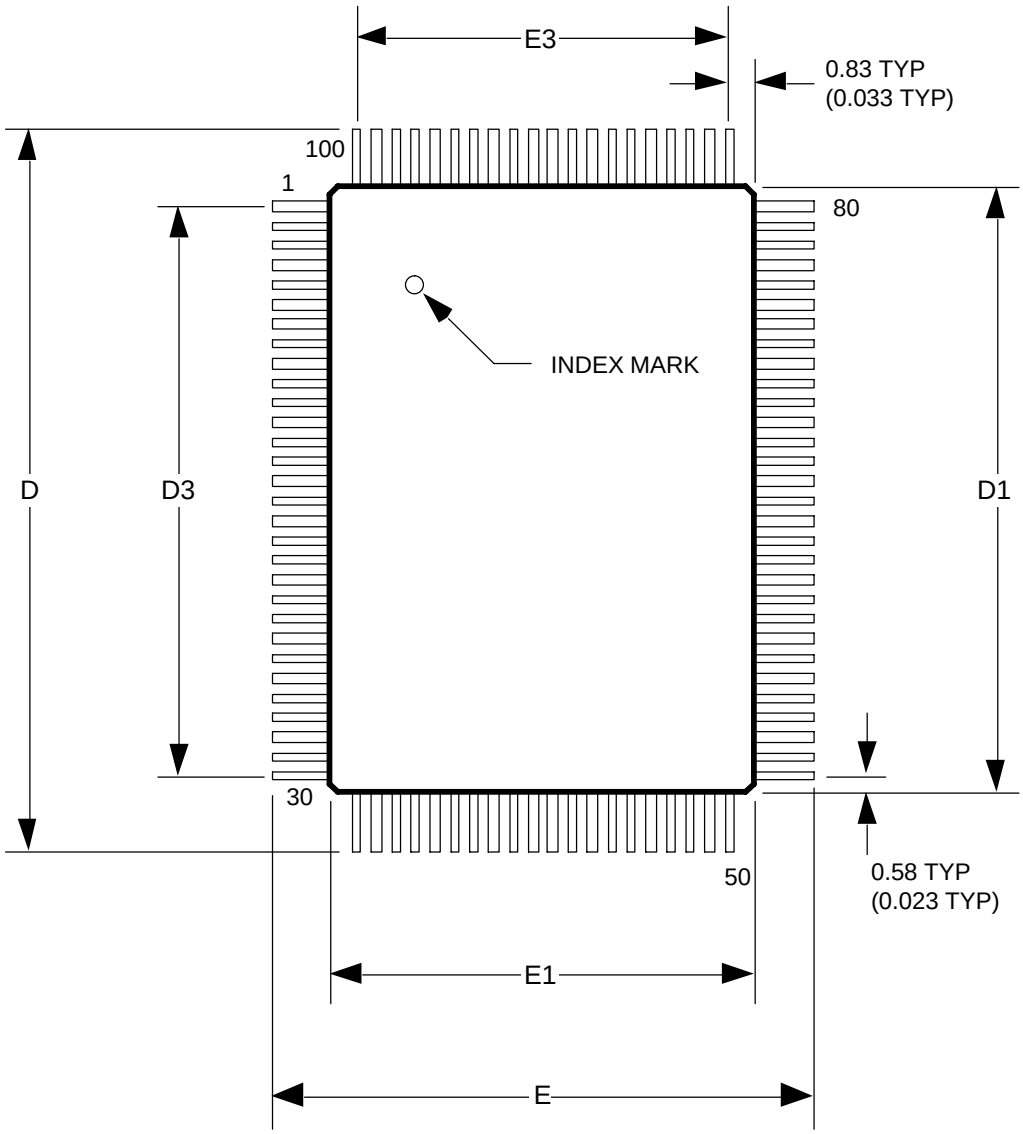


Figure 5.3 – MQFP100 package outlines

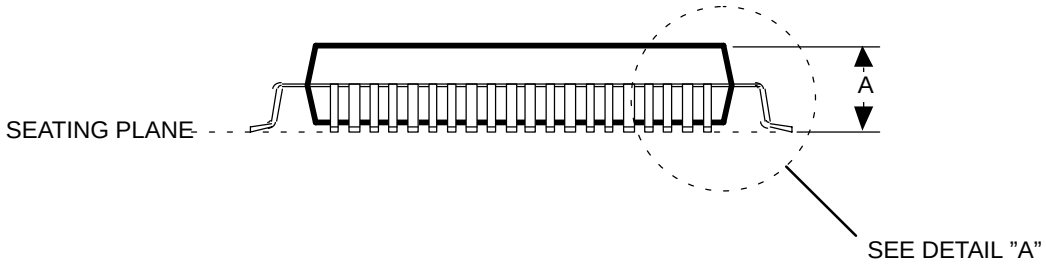


Figure 5.3 – MQFP100 package outlines (continued)

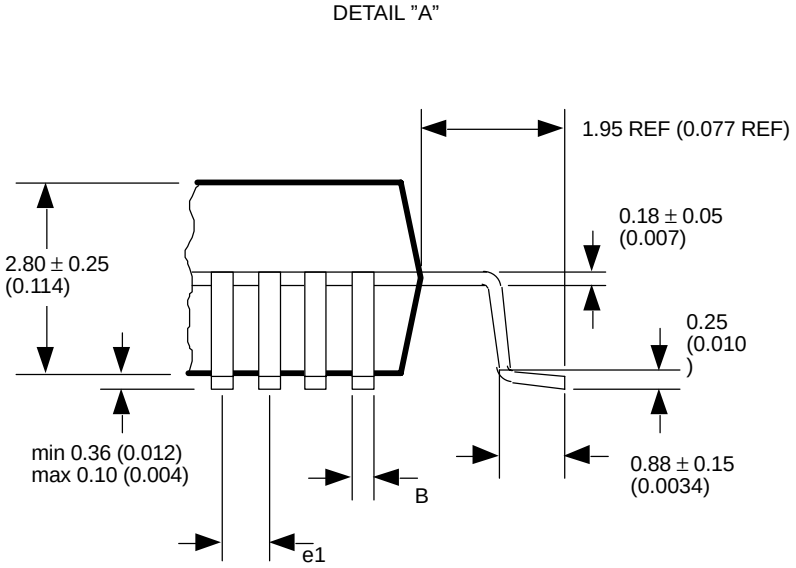


Figure 5.4 – MQFP100 package outlines – Terminal details

SYMBOL	MINIMUM mm (inch)	MAXIMUM mm (inch)
A		3.40 (0.134)
B	0.22 (0.009)	0.38 (0.015)
D	23.65 (0.931)	24.15 (0.951)
D1	19.90 (0.783)	20.10 (0.791)
D3	18.84 REF (0.742 REF)	
E	17.65 (0.695)	18.15 (0.715)
E1	13.90 (0.547)	14.10 (0.555)
E3	12.34 REF (0.486 REF)	
e1	0.65 TYP (0.025 TYP)	
N	100 pins	
ND	30 pins	
NE	20 pins	

Table 5.2 – MQFP100 package dimensions

Chapter 6 Application notes

1. INTERFACING WITH THE MOTOROLA 68000 MICROPROCESSOR

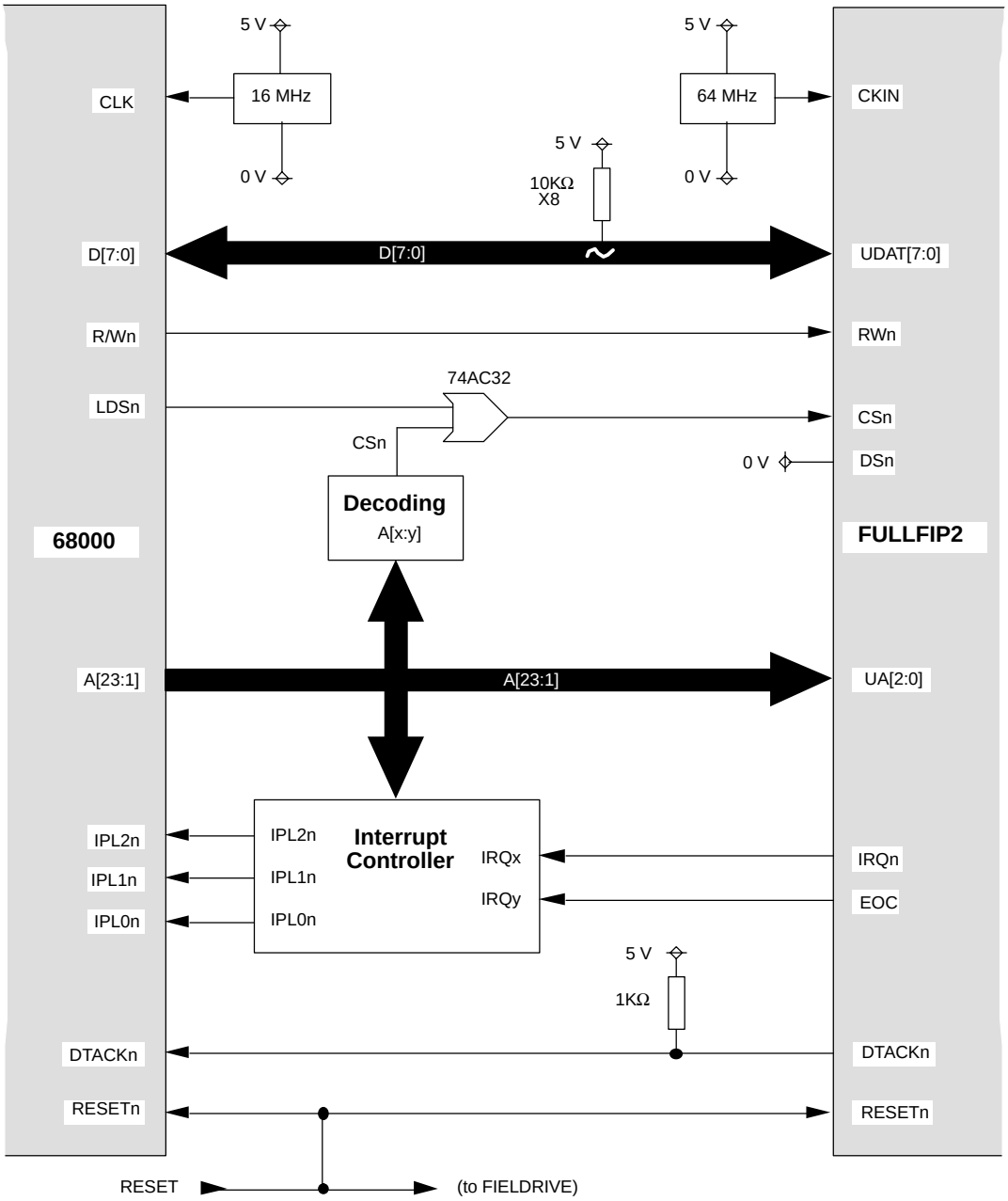


Figure 6.1 – FULLFIP2 interface with a 68000

2. INTERFACING WITH THE INTEL 80C188 MICROPROCESSOR

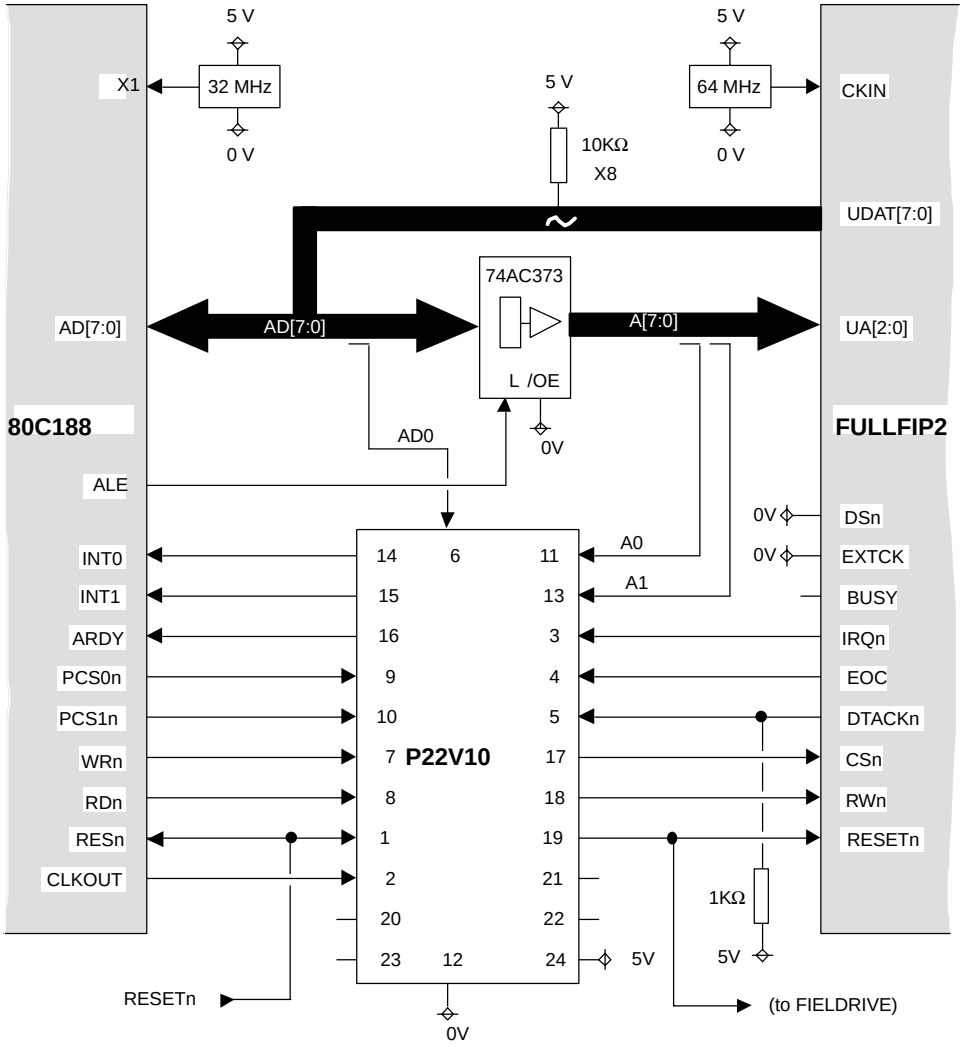


Figure 6.2 – FULLFIP2 interface with a 80C188

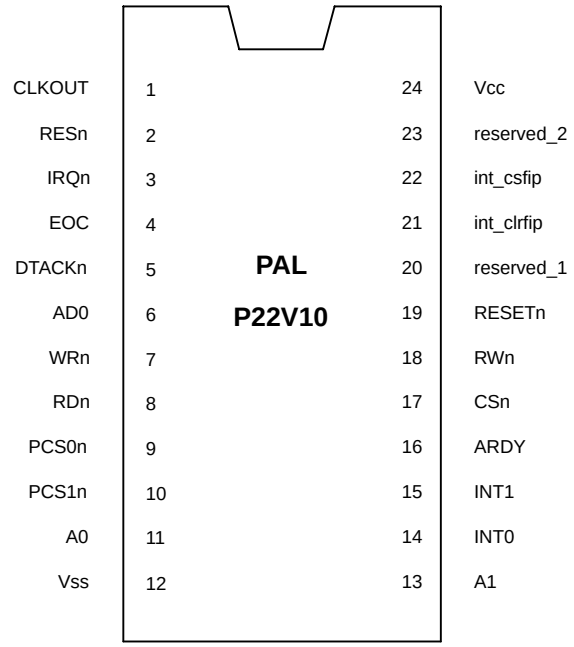


Figure 6.3 – PAL P22V10 component pinout

Reduced equations of the PAL P22V10 component :

```
int_csfip := (!PCS1n & !WRn # !PCS1n & !RDn);

int_clrfip := (WRn & int_clrfip
               # AD0 & int_clrfip
               # A1 & int_clrfip
               # A0 & int_clrfip
               # PCS0n & int_clrfip
               # !A0 & !A1 & AD0 & !PCS0n & !RESn & !WRn);
RESETn = (RESn & !int_clrfip);

RWn = (WRn);

!CSn = (!WRn & int_csfip # !RDn & int_csfip);

!ARDY = (!DTACKn # PCS1n);

!INT1 = (EOC);

!INT0 = (IRQ0n);
```

3. INTERFACING WITH THE EXTERNAL PRIVATE MEMORY

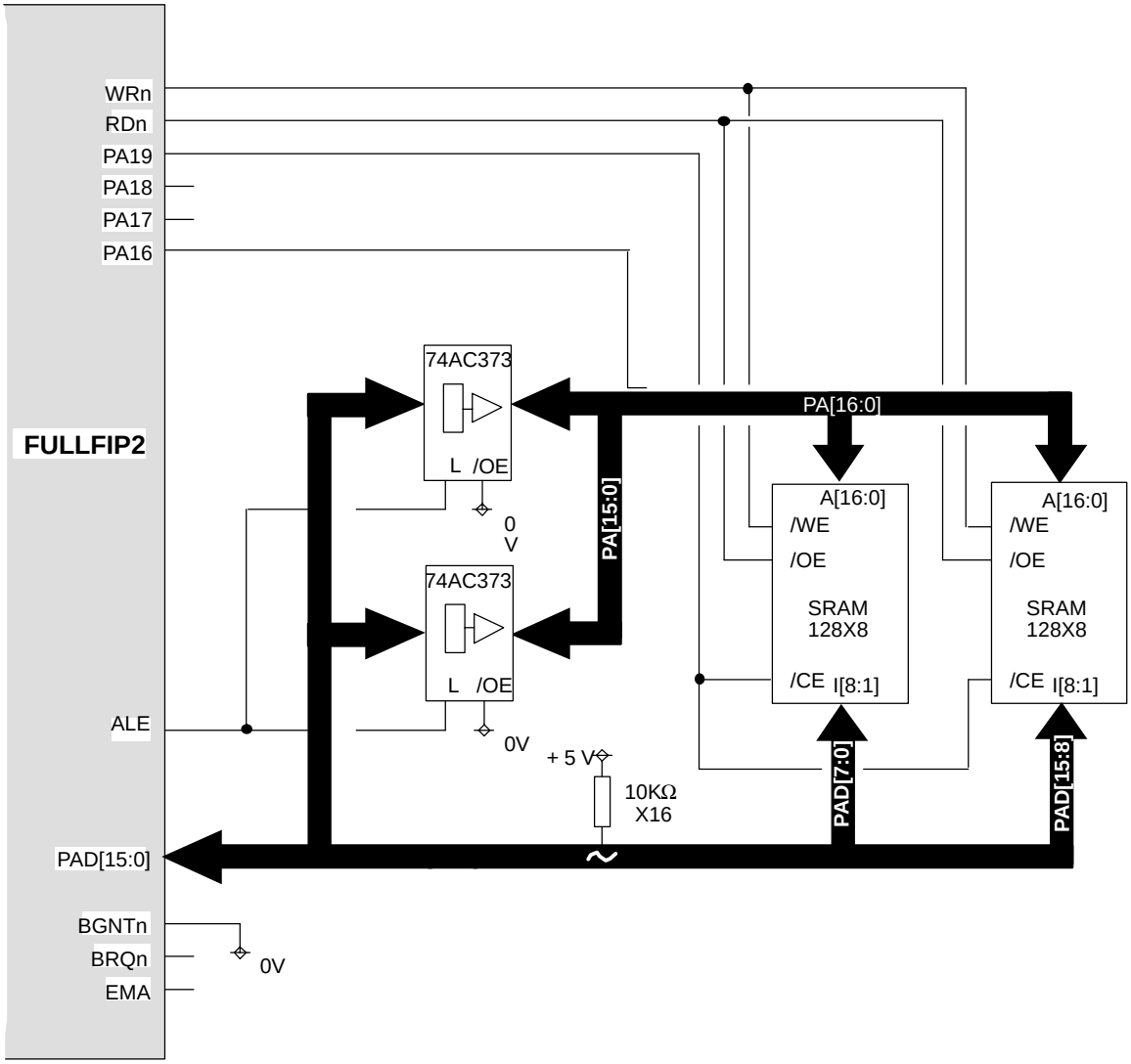


Figure 6.4 – External private memory interface

4. INTERFACING WITH THE LINE TRANSCEIVER

The communication processor FULLFIP2 needs to be connected to the WorldFIP fieldbus through a line driver such as FIELDRIVE which is especially designed to adapt the logical signal of the communication processor inputs/outputs to the signal of the bus.

Moreover, it is recommended to ensure a galvanic isolation between the WorldFIP bus and the line driver with a transformer such as FIELDTR. The insertion of a capacitor between the fieldbus and the FIELDTR line isolating transformer avoids transformer saturation by an eventual continuous current component.

The Figure 6.5 shows a typical example using the FIELDRIVE line driver connected to the FULLFIP2 component.

A protection of the FIELDRIVE line driver input/output against overvoltage generated on the bus outside the –10 V/+10 V range is recommended in every example shown hereafter.

The connection of the subscriber to the bus is made with a 9–pin male connector J9.

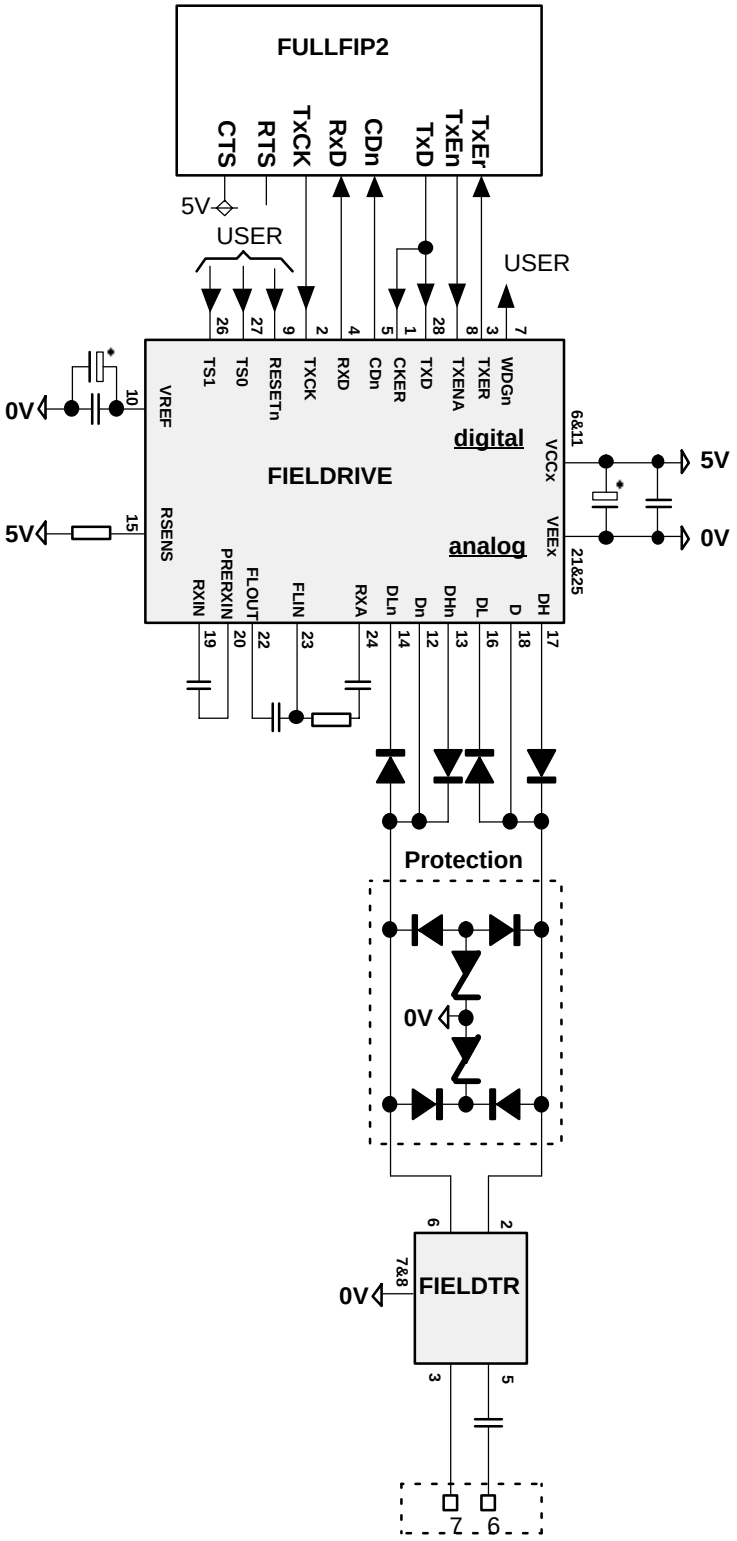


Figure 6.5 – Implementation of a fieldbus connection

Chapter 7 Board design rules

The FULLFIP2 can be used as fully compatible with the first–generation FULLFIP chip. This will allow a direct replacement of the FULLFIP component by the PLCC84–package FULLFIP2 on existing boards, that can be exercised without any change on the software libraries.

However, it is mandatory to verify that the following rules are satisfied on the design :

- **Initialization**

  During the component initialization phase, when the RESETn input pin is kept active, the TXER input signal must be kept not active then forced to the low level.

  This pin is checked by the internal hardware circuitry to force all timings compatible between FULLFIP and FULLFIP2.

- **CSn as unique chip select**

  User access with FULLFIP2 is now driven using the CSn input pin. DSn is no more taken into account. This makes the access simplier (in most designs with FULLFIP CSn and DSn were connected together).

  The end of the user access cycles, DTACKn output signal goes directly from active low state to the tri–stated value. This places the requirement for a 1 kΩ external pullup resistor on the DTACKn pin.

- **External resistors on unconnected input pins**

  Input pins that are not dynamically driven on the design with FULLFIP2 must be pulled up or down externally, even if an internal pulling resistor in the component has been specified.

- **Board testing issue**

  TSTn[2:0] test control input pins must be kept inactive high during FULLFIP2 operation. In addition, if TSTn[1] is connected to VDD through a 1 kΩ resistor, it is possible to force all circuit outputs, except MCK, and all I/Os at the tri–stated level by placing an active low value on TSTn[1]. This feature can be used for board testing purpose.

Signal	Description	Pin	External pulling
TSTCK	External test clock.	1	1 KΩ or direct to VDD
MA[8:0]	Microprogrammed address, tri–stated if EMAn = high.	5 4 3 79 78 77 76 75 74	22 KΩ to VDD 22 KΩ to VDD 22 KΩ to VDD 22 KΩ to VDD 22 KΩ to VDD 22 KΩ to VDD 22 KΩ to VDD 22 KΩ to VDD 22 KΩ to VDD
RTSK	Running task, tri–stated if EMAn = high.	6	22 KΩ to VDD
PA[19:16]	Non multiplexed address bus, tri–stated if BGNTn = high (if BGNTn used).	12 13 14 15	10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD
PAD[15:0]	Multiplexed address bus, tri–stated outside external private memory access cycles.	16 17 18 19 20 21 22 25 30 31 32 33 34 35 36 37	10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD
BGNTn	Bus Grant for memory access.	29	1 KΩ or direct to VSS
CTS	Clear To Send.	42	1 KΩ or direct to VDD
EXTCK	External test clock selection.	53	1 KΩ or direct to VSS
Reserved	(DSn in the first generation)	56	connect to CSn or VDD or VSS
UDAT[7:0]	User data bus, tri–stated outside user access.	64 63 62 61 60 59 58 57	10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD
DTACKn	User access data acknowledge, tri–stated when non active.	71	1KΩ to VDD
TSTn[2:0]	Test control signals. Placing TSTn[1] at low level externally forces all outputs and I/Os tri–stated. This can be used for board testing purposes.	84 81 80	1KΩ or direct to VDD 1KΩ to VDD 1KΩ or direct to VDD
Reserved	(TXER2 in the first generation)	44	Direct to VSS

Table 7.1 – Value of the external pulling resistors – PLCC84 package

Signal	Description	Pin	External pulling
TSTCK	External test clock.	90	1 KΩ or direct to VDD
MA[8:0]	Microprogrammed address, tri–stated if EMAn = high.	94 93 92 84 83 82 81 80 76	22 KΩ to VDD 22 KΩ to VDD 22 KΩ to VDD 22 KΩ to VDD 22 KΩ to VDD 22 KΩ to VDD 22 KΩ to VDD 22 KΩ to VDD 22 KΩ to VDD
RTSK	Running task, tri–stated if EMAn = high.	95	22 KΩ to VDD
PA[19:16]	Non multiplexed address bus, tri–stated if BGNTn = high (if BGNTn used).	5 6 7 8	10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD
PAD[15:0]	Multiplexed address bus, tri–stated outside external private memory access cycles.	9 10 11 12 13 14 15 19 24 25 26 31 32 33 34 35	10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD
BGNTn	Bus Grant for memory access.	23	1 KΩ or direct to VSS
CTS	Clear To Send.	40	1 KΩ or direct to VDD
EXTCK	External test clock selection.	51	1 KΩ or direct to VSS
Reserved	DSn in the first generation	57	connect to CSn or VDD or VSS
UDAT[7:0]	User data bus, tri–stated outside user access.	65 64 63 62 61 60 59 58	10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD 10 KΩ to VDD
DTACKn	User access data acknowledge, tri–stated when non active.	73	1KΩ to VDD
TSTn[2:0]	Test control signals. Placing TSTn[1] at low level externally forces all outputs and I/Os tri–stated. This can be used for board testing purposes.	89 86 85	1KΩ or direct to VDD 1KΩ to VDD 1KΩ or direct to VDD
Reserved	TXER2 in the first generation	42	Direct to VSS

Table 7.2 – Value of the external pulling resistors – MQFP100 package