MHS

DATA SHEET

HM 65664

8 K x 8
ULTIMATE CMOS SRAM

FEATURES

ACCESS TIME
MILITARY/INDUSTRIAL: 45/55ns (max)
COMMERCIAL: 45/55ns (max)
VERY LOW POWER CONSUMPTION
ACTIVE: 175.0 mW (Typ)
STANDBY: 2.0 µW (Typ)
DATA RETENTION: 0.8 µW (Typ)
WIDE TEMPERATURE RANGE: −55 TO +125°C

- **300 AND 600 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **SINGLE 5 VOLT SUPPLY**
- **EQUAL CYCLE AND ACCESS TIME**
- **GATED INPUTS: NO PULL-UP/DOWN RESISTORS ARE REQUIRED**

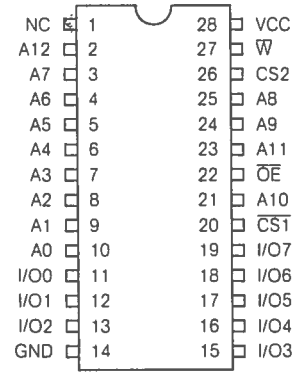
DESCRIPTION

The HM-65664 is a very low power CMOS static RAM organized as 8192 x 8 bits. It is manufactured using the MHS high performance CMOS technology named super CMOS.
With this process, MHS is the first to bring the solution for applications where fast computing is as mandatory as low consumption, such as the aerospace electronics or the portable instruments PC's.
Utilising an array of six transistors (6T) memory cells, the HM-65664 combines an extremely low standby supply current (typical value = 0.1 µA) with a fast access time at 45 ns over the full temperature range.
The high stability of the 6T cell provides excellent protection against soft errors due to noise.
Extra protection against heavy ions is given by the use of an epitaxial layer on a P substrate.
The HM-65664 is processed following the test methods of MIL STD 883C.

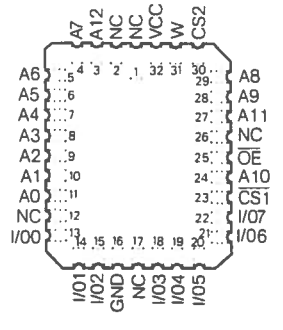
PACKAGES

- Plastic 300 & 600 mils, 28 pins, DIL.
- Ceramic 600 mils, 28 pins, DIL.
- SO 300 mils, 28 pins, DIL.
- LCC, 32 pins.

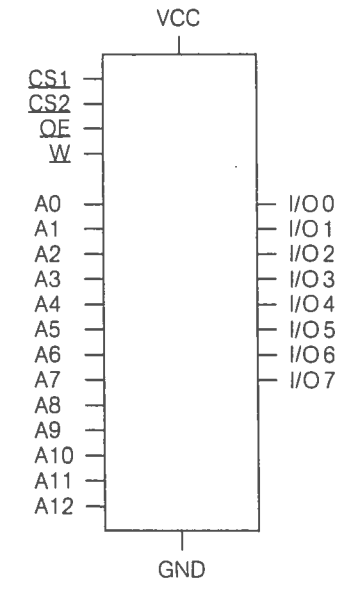
Pinout DIL 28 pins (top view)



Pinout LCC 32 pins (top view)

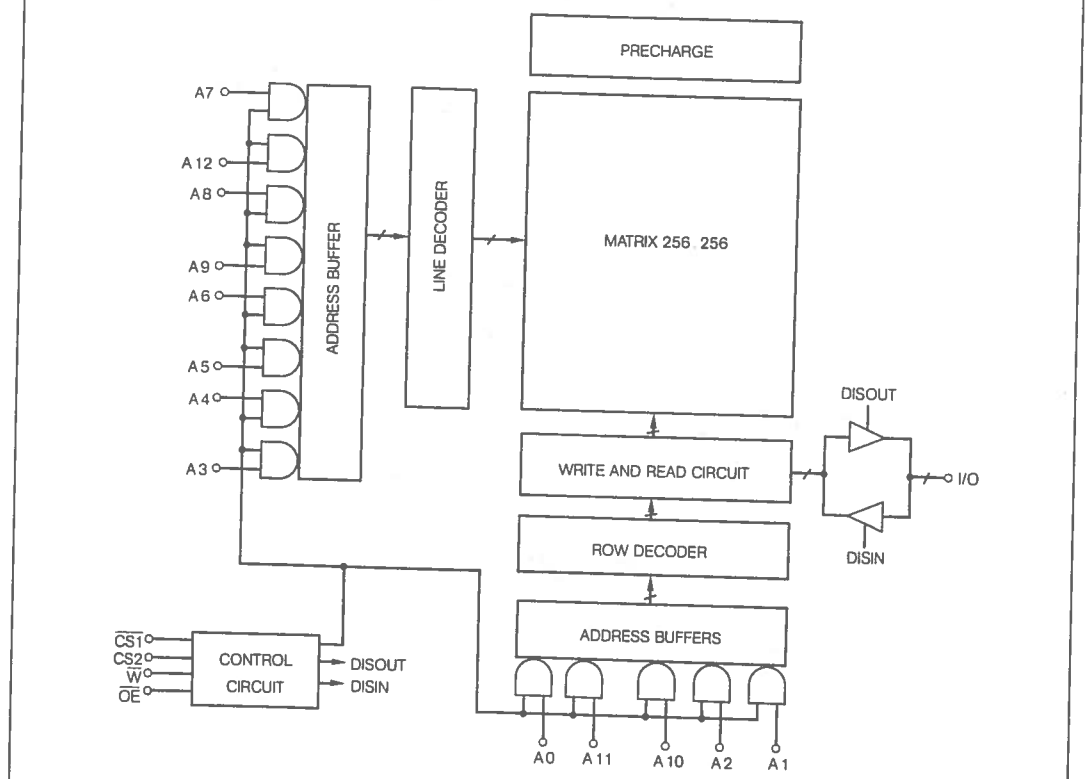


LOGIC SYMBOL



MHS

BLOCK DIAGRAM



PIN NAMES

A0-A12 : Address inputs	$\overline{CS1}$: Chip-Select 1
I/O0-I/O7 : Input/Output	CS2 : Chip-Select 2

Vcc : Power	$\overline{OE}$: Output Enable
Gnd : Ground	$\overline{W}$: Write enable

TRUTH TABLE

$\overline{CS}$ 1	CS 2	$\overline{OE}$	$\overline{W}$	DATA-IN *	DATA-OUT	MODE
H	X	X	X	Z	Z	Deselect
L	H	L	H	Z	Valid	Read
L	H	X	L	Valid	Z	Write
L	H	H	H	Z	Z	Output disable

L=low, H=high, X=H or L, Z=high impedance

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : −0.5V to +7.0V
Input ou Output voltage applied : (Gnd−0.3V) to (Vcc+0.3V)
Storage temperature : −65°C to +150°C

OPERATING RANGE

	OPERATING VOLTAGE	OPERATING TEMPERATURE
Military (−2)	Vcc ± 10%	−55°C to +125°C
Industrial (−9)	Vcc ± 10%	−40°C to + 85°C
Commercial (−5)	Vcc ± 10%	0°C to + 70°C

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL (1)	Input low voltage	−0.3	0.0	0.8	V
VIH	Input high voltage	2.2	–	Vcc+0.3V	V

Note 1 : VIL min=−0.3V or−1.0V pulse width 50 ns

CAPACITANCE

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin (2)	Input capacitance	–	–	8	pF
Cout (2)	Output capacitance	–	–	8	pF

Note 2 : TA=25°C, f=1 MHz, Vcc=5.0V, these parameters are not tested

ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX (3)	Input leakage current	−1.0	–	1.0	µA
IOZ (3)	Output leakage current	−1.0	–	1.0	µA
VOL (4)	Output low voltage	–	–	0.4	V
VOH (4)	Output high voltage	2.4	–	–	V

Note 3 : Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled
Note 4 : Vcc min, IOL = 4.0 mA, IOH = −1.0 mA

CONSUMPTION FOR COMMERCIAL SPECIFICATION (−5) :

SYMBOL	PARAMETER	65664 B–5	65664 S–5	65664 –5	65664 C–5	UNIT	VALUE
ICCSB (5)	Standby supply current	10	15	10	15	mA	max
ICCSB1 (6)	Standby supply current	1.0	100.0	1.0	100.0	µA	max
ICC (7)	Operating supply current	10	15	10	15	mA	max
ICCOP (8)	Operating supply current	50	75	50	75	mA	max

CONSUMPTION FOR INDUSTRIAL SPECIFICATION (−9) :

SYMBOL	PARAMETER	65664 B–9	65664 S–9	65664 –9	65664 C–9	UNIT	VALUE
ICCSB (5)	Standby supply current	15	20	15	20	mA	max
ICCSB1 (6)	Standby supply current	5.0	100.0	5.0	100.0	µA	max
ICC (7)	Operating supply current	15	20	15	20	mA	max
ICCOP (8)	Operating supply current	75	100	75	100	mA	max

CONSUMPTION FOR MILITARY SPECIFICATION (−2) :

SYMBOL	PARAMETER	65664 B–2	65664 S–2	65664 –2	65664 C–2	UNIT	VALUE
ICCSB (5)	Standby supply current	15	20	15	20	mA	max
ICCSB1 (6)	Standby supply current	50.0	500.0	50.0	500.0	µA	max
ICC (7)	Operating supply current	15	20	15	20	mA	max
ICCOP (8)	Operating supply current	75	100	75	100	mA	max

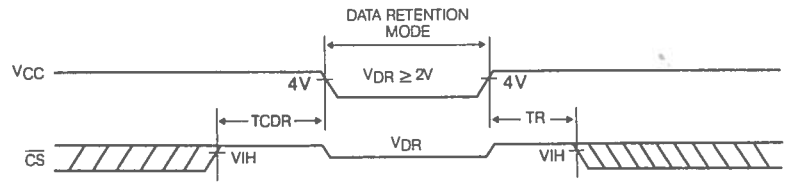
Note 5 : $\overline{CS1}$ >= VIH, CS2 <= VIL
Note 6 : $\overline{CS1}$ >= Vcc − 0.3V, CS2 <= 0.3V, Iout = 0 mA
Note 7 : $\overline{CS1}$ <= VIL, CS2 >= VIH, Iout = 0 mA, Vin = Gna/Vcc
Note 8 : Vcc max, Iout = 0 mA, f = max, Vin = Gnd/Vcc

DATA RETENTION MODE

HS CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1/ Chip select (CS) must be held high during data retention ; within Vcc to Vcc + 0.3V.
2/ Output Enable (OE) should be held high to keep the RAM outputs high impedance, minimizing power dissipation.
3/ CS and OE must be kept between Vcc + 0.3V and 70% of Vcc during the power up and power down transitions.
4/ The RAM can begin operation > 55 NS after Vcc reaches the minimum operating voltage (4.5V).

TIMING



DATA RETENTION CHARACTERISTICS :

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL (9)	MAXIMUM	UNIT
VCCDR	Vcc for data retention	2.0	–		V
TCDR	Chip deselect to data retention time	0.0	–		ns
TR	Operation recovery time	TAVAV (10)	–		
ICCDR1 (11)	Data retention current @ 2.0V : HM-65664 (B)–5	–	0.1	1.0*	µA
	HM-65664 (B)–9	–	0.1	3.0*	µA
	HM-65664 (B)–2	–	0.1	20.0	µA
	HM-65664S/C–5	–	0.1	30.0	µA
	HM-65664S/C–9	–	0.1	30.0	µA
	HM-65664S/C–2	–	0.1	200.0	µA
ICCDR2 (11)	Data retention current @ 3.0V : HM-65664 (B)–5	–	0.3	1.0*	µA
	HM-65664 (B)–9	–	0.3	3.0*	µA
	HM-65664 (B)–2	–	0.3	30.0	µA
	HM-65664S/C–5	–	0.3	50.0	µA
	HM-65664S/C–9	–	0.3	50.0	µA
	HM-65664S/C–2	–	0.3	300.0	µA

Note 9 : TA = 25 °C
Note 10 : TAVAV = Read cycle time
Note 11 : CS = Vcc, Vin = Gnd/Vcc, this parameter is only tested to Vcc = 2V

ELECTRICAL CHARACTERISTICS AC PARAMETERS

AC CONDITIONS :

Input pulse levels	: Gnd to 3.0V
Input rise	: 5 ns
Input timing reference levels	: 1.5V
Output load	: 1 TTL gate + 100 pF

WRITE CYCLE : Commercial specification

SYMBOL	PARAMETER	65664 B–5	65664 S–5	65664 –5	65664 C–5	UNIT	VALUE
TAVAV	Write cycle time	45	45	55	55	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	45	45	55	55	ns	min
TDVWH	Data set-up time	15	15	20	20	ns	min
TEL1WH	$\overline{CS1}$ low to write end	45	45	55	55	ns	min
TEH2WH	CS2 high to write end	45	45	55	55	ns	min
TWLQZ (12)	Write low to high Z	10	10	15	15	ns	max
TWLWH	Write pulse width	40	40	50	50	ns	min
TWHAX	Address hold to end of write	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	0	ns	min
TWHQX (12, 13)	Write high to low Z	0	0	0	0	ns	min

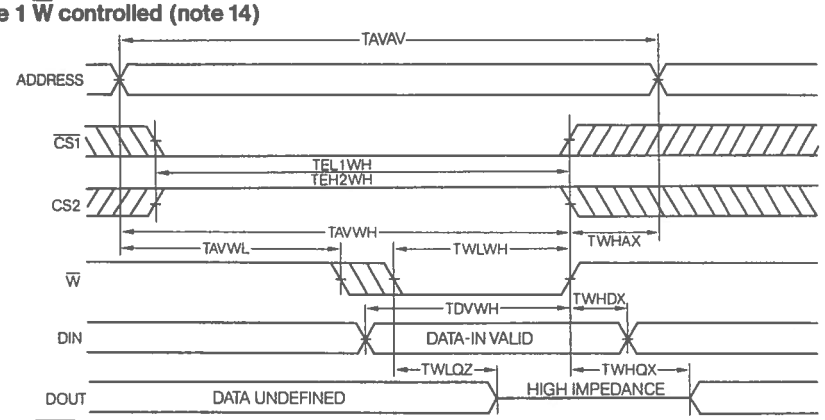
Note 12 : The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Note 13 : At any given temperature and voltage condition, TWHQX is less than TWLQZ for all devices. These parameters are sampled and not 100% tested.

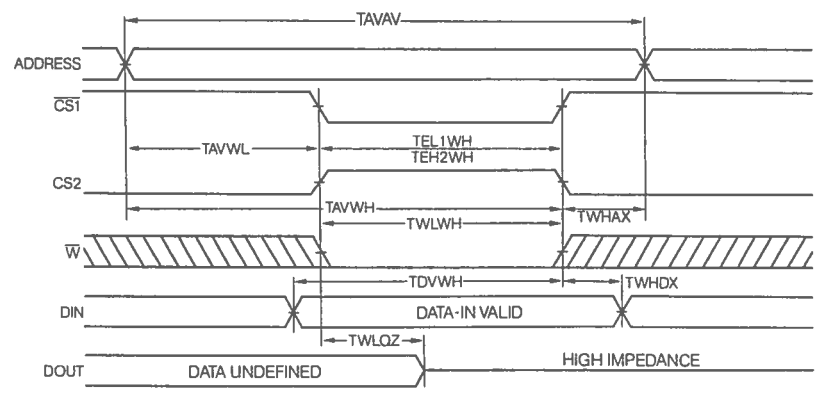
WRITE CYCLE : Industrial and Military specification

SYMBOL	PARAMETER	65664 B–9/2	65664 S–9/2	65664 –9/2	65664 C–9/2	UNIT	VALUE
TAVAV	Write cycle time	45	45	55	55	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	45	45	55	55	ns	min
TDVWH	Data set-up time	15	15	20	20	ns	min
TEL1WH	CS1 low to write end	45	45	55	55	ns	min
TEH2WH	CS2 high to write end	45	45	55	55	ns	min
TWLQZ (12)	Write low to high Z	10	10	15	15	ns	max
TWLWH	Write pulse width	40	40	50	50	ns	min
TWHAX	Address hold to end of write	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	0	ns	min
TWHQX (12, 13)	Write high to low Z	0	0	0	0	ns	min

Write cycle 1 $\overline{W}$ controlled (note 14)



Write cycle 2 $\overline{CS1}$ controlled (note 14)



Note 14 : The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
Data out is high impedance if $\overline{OE}$ = VIH.

READ CYCLE: Commercial specification

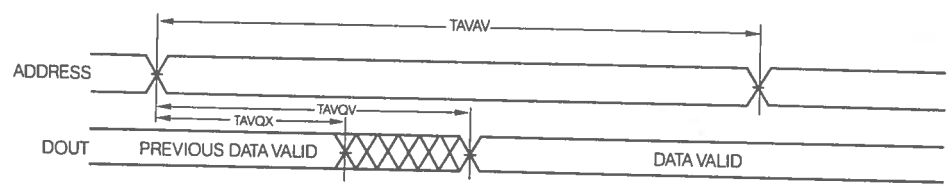
SYMBOL	PARAMETER	65664 B–5	65664 S–5	65664 –5	65664 C–5	UNIT	VALUE
TAVAV	Write cycle time	45	45	55	55	ns	min
TAVQV	Address access time	45	45	55	55	ns	max
TAVQX	Address valid to low Z	5	5	10	10	ns	min
TEL1QV	Chip-select 1 access time	50	50	65	65	ns	max
TEH2QV	Chip-select 2 access time	50	50	65	65	ns	max
TEL1QX	$\overline{CS1}$ low to low Z	5	5	10	10	ns	max
TEH2QX	CS2 to low Z	5	5	10	10	ns	max
TEH1QZ (15)	$\overline{CS1}$ high to high Z	45	45	55	55	ns	max
TEL2QZ (15)	CS2 low to high Z	45	45	55	55	ns	max
TGLQV	Output Enable access time	15	15	20	20	ns	max
TGLQX	$\overline{OE}$ low to low Z	15	15	20	20	ns	min
TGHQZ	$\overline{OE}$ high to high Z	10	10	20	20	ns	max

Note 15 : TEHQZ and TWLQZ are tested with C1 = 5 pF. Transition is measured ± 500 mV from steady state voltage.

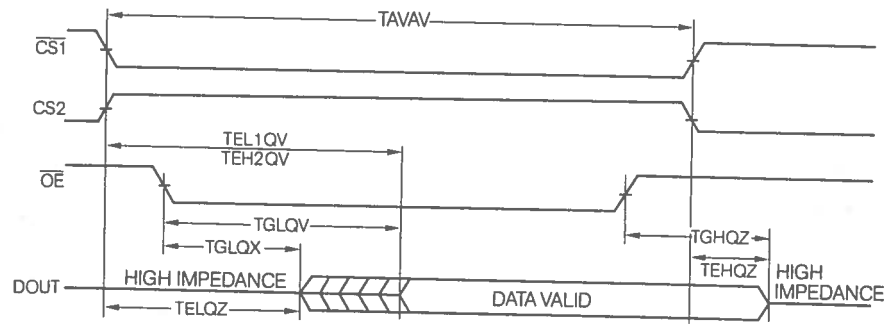
READ CYCLE : Industrial and Military specification

SYMBOL	PARAMETER	65664 B–9/2	65664 S–9/2	65664 –9/2	65664 C–9/2	UNIT	VALUE
TAVAV	Write cycle time	45	45	55	55	ns	min
TAVQV	Address access time	45	45	55	55	ns	max
TAVQX	Address valid to low Z	5	5	10	10	ns	min
TEL1QV	Chip-select 1 access time	50	50	65	65	ns	max
THL2QV	Chip-select 2 access time	50	50	65	65	ns	max
TEL1QX	$\overline{CS1}$ low to low Z	5	5	10	10	ns	max
THL2QX	CS2 high to low Z	5	5	10	10	ns	max
TEH1QZ (15)	$\overline{CS1}$ high to high Z	45	45	55	55	ns	max
TEL2QZ (15)	CS2 low to high Z	45	45	55	55	ns	max
TGLQV	Output Enable access time	15	15	20	20	ns	max
TGLQX	$\overline{OE}$ low to low Z	15	15	20	20	ns	min
TGHQZ	$\overline{OE}$ high to high Z	10	10	20	20	ns	max

Read cycle nb 1 : (notes 16, 17)



Read cycle nb 2 : (notes 16, 18)



Note 16 : $\overline{W}$ is high for read cycle
Note 17 : Device is continuously selected, $\overline{CS1}$ – $\overline{OE}$ = VIL and CS2 = VIH
Note 18 : Address valid prior to or coincident with $\overline{CS}$ transition low.

ORDERING INFORMATION

Package	Device type	Grade	Level
HM1	65664	B	-5
0 - Chip form 1 - Ceramic 28 pins 3 - Plastic 28 pins 300 mils 3E - Plastic 28 pins 600 mils 4 - LCC 32 pins T - SOIC 28 pins	8 kx8 Ultimate CMOS static RAM	B : high speed/low current S : high speed/standard current Blank : standard speed/low current C : standard	-5 : Commercial -7 : Commercial with B.I. -9 : Industrial -2: Military -8: Military with B.I.

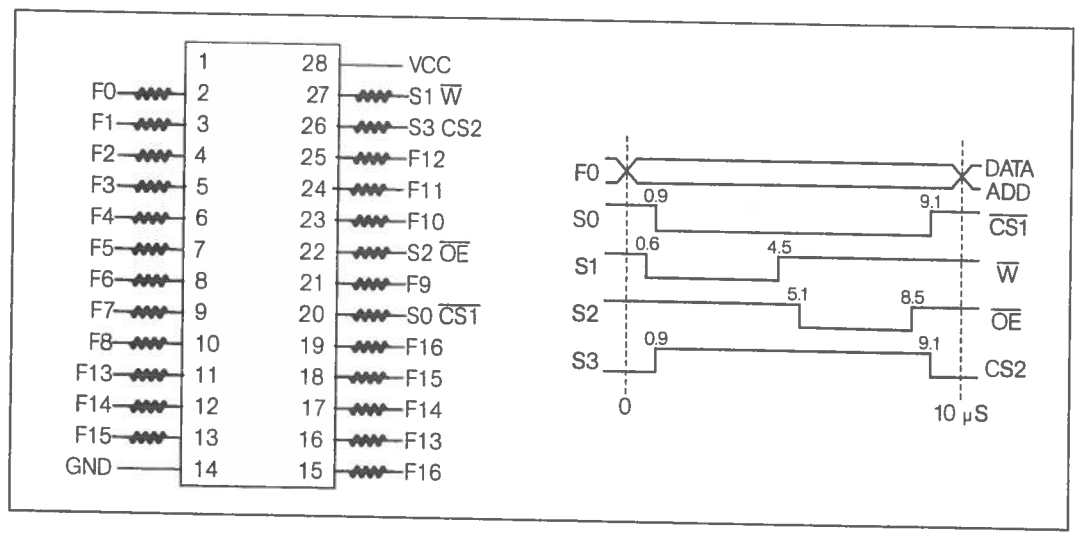
3

PACKAGE OUTLINE

For the packaging information, refer to next page.

Package reference : Plastic DIL, 300 mils, 28 pins : x49
Plastic DIL, 600 mils, 28 pins : x32
Ceramic DIL, 600 mils, 28 pins : C32
SOIC DIL, 300 mils, 28 pins : TBD
LCC rectangular, 32 pins : L19

BURN-IN SCHEMATICS



VCC = 5V (-0,+0.5)
R = 1 Kohm per pin
F0 = 50 KHz ± 20%

Fn = 1/2 Fn - 1
S0 to S3 = programmable signals for write/read cycles.

4

HIGH SPEED CMOS SRAM