3.3V CMOS Static RAM
4 Meg (256K x 16-Bit)

IDT71V416YS
IDT71V416YL

Features

- **256K x 16 advanced high-speed CMOS Static RAM**
- **JEDEC Center Power / GND pinout for reduced noise.**
- **Equal access and cycle times**
  - *Commercial and Industrial: 10/12/15ns*
- **One Chip Select plus one Output Enable pin**
- **Bidirectional data inputs and outputs directly LVTTL-compatible**
- **Low power consumption via chip deselect**
- **Upper and Lower Byte Enable Pins**
- **Single 3.3V power supply**
- **Available in 44-pin, 400 mil plastic SOJ package and a 44-pin, 400 mil TSOP Type II package and a 48 ball grid array, 9mm x 9mm package.**
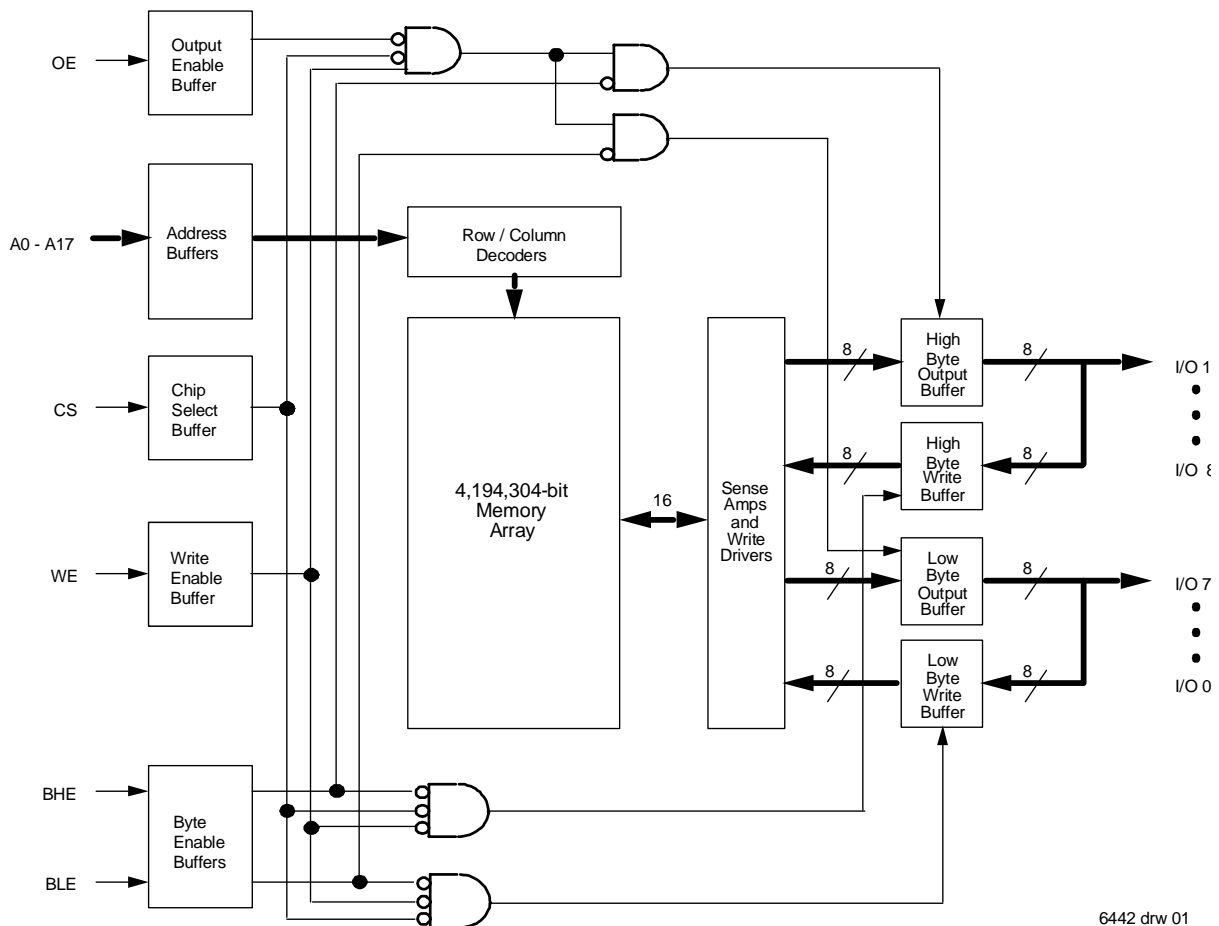
Description

The IDT71V416 is a 4,194,304-bit high-speed Static RAM organized as 256K x 16. It is fabricated using IDT's high-perfomance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

The IDT71V416 has an output enable pin which operates as fast as 5ns, with address access times as fast as 10ns. All bidirectional inputs and outputs of the IDT71V416 are LVTTL-compatible and operation is from a single 3.3V supply. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

The IDT71V416 is packaged in a 44-pin, 400 mil Plastic SOJ and a 44-pin, 400 mil TSOP Type II package and a 48 ball grid array, 9mm x 9mm package.
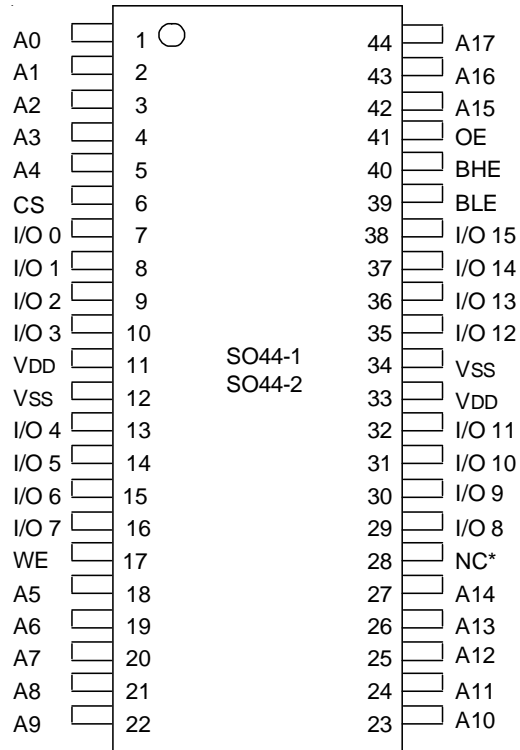
Functional Block Diagram

6442 drw 01

JULY 2004

DSC-6442/01

Pin Configurations - SOJ/TSOP

A0	1	○	44	A17
A1	2		43	A16
A2	3		42	A15
A3	4		41	OE
A4	5		40	BHE
CS	6		39	BLE
I/O 0	7		38	I/O 15
I/O 1	8		37	I/O 14
I/O 2	9		36	I/O 13
I/O 3	10		35	I/O 12
VDD	11	SO44-1	34	VSS
VSS	12	SO44-2	33	VDD
I/O 4	13		32	I/O 11
I/O 5	14		31	I/O 10
I/O 6	15		30	I/O 9
I/O 7	16		29	I/O 8
WE	17		28	NC*
A5	18		27	A14
A6	19		26	A13
A7	20		25	A12
A8	21		24	A11
A9	22		23	A10

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*Pin 28 can either be a NC or connected to Vss

Top View

Pin Configurations - 48 BGA

	1	2	3	4	5	6
A	$\overline{BLE}$	$\overline{OE}$	A_0	A_1	A_2	NC
B	I/O_0	$\overline{BHE}$	A_3	A_4	$\overline{CS}$	I/O_8
C	I/O_1	I/O_2	A_5	A_6	I/O_{10}	I/O_9
D	V_{SS}	I/O_3	A_{17}	A_7	I/O_{11}	V_{DD}
E	V_{DD}	I/O_4	NC	A_{16}	I/O_{12}	V_{SS}
F	I/O_6	I/O_5	A_{14}	A_{15}	I/O_{13}	I/O_{14}
G	I/O_7	NC	A_{12}	A_{13}	$\overline{WE}$	I/O_{15}
H	NC	A_8	A_9	A_{10}	A_{11}	NC

6442 tbl 11

Pin Descriptions

$A_0 - A_{17}$	Address Inputs	Input
$\overline{CS}$	Chip Select	Input
$\overline{WE}$	Write Enable	Input
$\overline{OE}$	Output Enable	Input
$\overline{BHE}$	High Byte Enable	Input
$\overline{BLE}$	Low Byte Enable	Input
$I/O_0 - I/O_{15}$	Data Input/Output	I/O
V_{DD}	3.3V Power	Pwr
V_{SS}	Ground	Gnd

6442 tbl 01

SOJ Capacitance

$(T_A = +25°C, f = 1.0MHz)$

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 3dV$	7	pF
$C_{I/O}$	I/O Capacitance	$V_{OUT} = 3dV$	8	pF

6442 tbl 02

48 BGA Capacitance

$(T_A = +25°C, f = 1.0MHz)$

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 3dV$	6	pF
$C_{I/O}$	I/O Capacitance	$V_{OUT} = 3dV$	7	pF

6442 tbl 02b

NOTE:

1. This parameter is guaranteed by device characterization, but not production tested.

Absolute Maximum Ratings[1]

Symbol	Rating	Value	Unit
V_{DD}	Supply Voltage Relative to V_{SS}	-0.5 to +4.6	V
V_{IN}, V_{OUT}	Terminal Voltage Relative to V_{SS}	-0.5 to V_{DD}+0.5	V
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
P_T	Power Dissipation	1	W
I_{OUT}	DC Output Current	50	mA

6442 tbl 04

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Temperature and Supply Voltage

Grade	Temperature	V_{SS}	V_{DD}
Commercial	0°C to +70°C	0V	See Below
Industrial	–40°C to +85°C	0V	See Below

6442 tbl 05

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	3.0	3.3	3.6	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	V_{DD}+0.3[1]	V
V_{IL}	Input Low Voltage	-0.3[2]	—	0.8	V

6442 tbl 06

NOTES:
1. VIH (max.) = VDD+2V for pulse width less than 5ns, once per cycle.
2. VIL (min.) = –2V for pulse width less than 5ns, once per cycle.

Truth Table[1]

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O0-I/O7	I/O8-I/O15	Function
H	X	X	X	X	High-Z	High-Z	Deselected - Standby
L	L	H	L	H	DATAOUT	High-Z	Low Byte Read
L	L	H	H	L	High-Z	DATAOUT	High Byte Read
L	L	H	L	L	DATAOUT	DATAOUT	Word Read
L	X	L	L	L	DATAIN	DATAIN	Word Write
L	X	L	L	H	DATAIN	High-Z	Low Byte Write
L	X	L	H	L	High-Z	DATAIN	High Byte Write
L	H	H	X	X	High-Z	High-Z	Outputs Disabled
L	X	X	H	H	High-Z	High-Z	Outputs Disabled

6442 tbl 03

NOTE:
1. H = V_{IH}, L = V_{IL}, X = Don't care.

DC Electrical Characteristics

(V$_{DD}$ = Min. to Max., Commercial and Industrial Temperature Ranges)

Symbol	Parameter	Test Conditions	IDT71V416		Unit
			Min.	Max.	
$|I_{LI}|$	Input Leakage Current	V$_{CC}$ = Max., V$_{IN}$ = V$_{SS}$ to V$_{DD}$	—	5	µA
$|I_{LO}|$	Output Leakage Current	V$_{DD}$ = Max., $\overline{CS}$ = V$_{IH}$, V$_{OUT}$ = V$_{SS}$ to V$_{DD}$	—	5	µA
V$_{OL}$	Output Low Voltage	I$_{OL}$ = 8mA, V$_{DD}$ = Min.	—	0.4	V
V$_{OH}$	Output High Voltage	I$_{OH}$ = -4mA, V$_{DD}$ = Min.	2.4	—	V

6442 tbl 07

DC Electrical Characteristics[1, 2, 3]

(V$_{DD}$ = Min. to Max., V$_{LC}$ = 0.2V, V$_{HC}$ = V$_{DD}$ – 0.2V)

Symbol	Parameter		71V416S/L10		71V416S/L12		71V416S/L15		Unit
			Com'l.	Ind.[6]	Com'l.	Ind.	Com'l.	Ind.	
I$_{CC}$	Dynamic Operating Current $\overline{CS} \leq$ V$_{LC}$, Outputs Open, V$_{DD}$ = Max., f = f$_{MAX}$[4]	S	200	200	180	180	170	170	mA
		L	180	—	170	170	160	160	
I$_{SB}$	Dynamic Standby Power Supply Current $\overline{CS} \geq$ V$_{HC}$, Outputs Open, V$_{DD}$ = Max., f = f$_{MAX}$[4]	S	70	70	60	60	50	50	mA
		L	50	—	45	45	40	40	
I$_{SB1}$	Full Standby Power Supply Current (static) $\overline{CS} \geq$ V$_{HC}$, Outputs Open, V$_{DD}$ = Max., f = 0[4]	S	20	20	20	20	20	20	mA
		L	10	—	10	10	10	10	

6442 tbl 08

NOTES:
1. All values are maximum guaranteed values.
2. All inputs switch between 0.2V (Low) and V$_{DD}$ -0.2V (High).
3. Power specifications are preliminary.
4. f$_{MAX}$ = 1/t$_{RC}$ (all address inputs are cycling at f$_{MAX}$); f = 0 means no address input lines are changing.
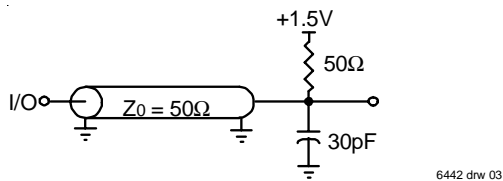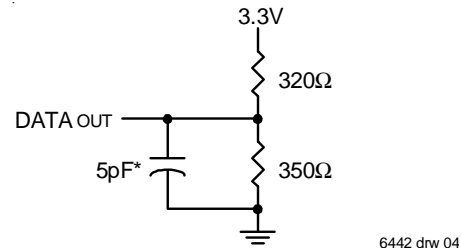5. Standard power 10ns (S10) speed grade only.

AC Test Loads

Figure 1. AC Test Load

*Including jig and scope capacitance.

Figure 2. AC Test Load
(for t$_{CLZ}$, t$_{OLZ}$, t$_{CHZ}$, t$_{OHZ}$, t$_{OW}$, and t$_{WHZ}$)
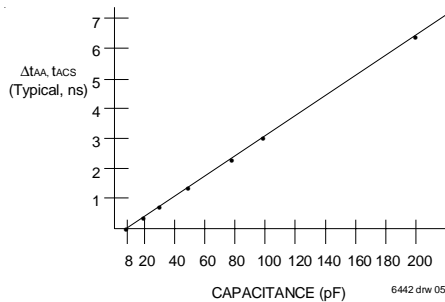
Figure 3. Output Capacitive Derating

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1.5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	Figures 1,2 and 3

6442 tbl 09

AC Electrical Characteristics

(V_{DD} = Min. to Max., Commercial and Industrial Temperature Ranges)

Symbol	Parameter	71V416S/L10[2]		71V416S/L12		71V416S/L15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	10	—	12	—	15	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	ns
t_{ACS}	Chip Select Access Time	—	10	—	12	—	15	ns
t_{CLZ}[1]	Chip Select Low to Output in Low-Z	4	—	4	—	4	—	ns
t_{CHZ}[1]	Chip Select High to Output in High-Z	—	5	—	6	—	7	ns
t_{OE}	Output Enable Low to Output Valid	—	5	—	6	—	7	ns
t_{OLZ}[1]	Output Enable Low to Output in Low-Z	0	—	0	—	0	—	ns
t_{OHZ}[1]	Output Enable High to Output in High-Z	—	5	—	6	—	7	ns
t_{OH}	Output Hold from Address Change	4	—	4	—	4	—	ns
t_{BE}	Byte Enable Low to Output Valid	—	5	—	6	—	7	ns
t_{BLZ}[1]	Byte Enable Low to Output in Low-Z	0	—	0	—	0	—	ns
t_{BHZ}[1]	Byte Enable High to Output in High-Z	—	5	—	6	—	7	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	10	—	12	—	15	—	ns
t_{AW}	Address Valid to End of Write	8	—	8	—	10	—	ns
t_{CW}	Chip Select Low to End of Write	8	—	8	—	10	—	ns
t_{BW}	Byte Enable Low to End of Write	8	—	8	—	10	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WR}	Address Hold from End of Write	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	8	—	8	—	10	—	ns
t_{DW}	Data Valid to End of Write	5	—	6	—	7	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{OW}[1]	Write Enable High to Output in Low-Z	3	—	3	—	3	—	ns
t_{WHZ}[1]	Write Enable Low to Output in High-Z	—	6	—	7	—	7	ns

6442 tbl 10

NOTE:
1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.
2. Low power 10ns (L10) speed 0ºC to +70ºC temperature range only.
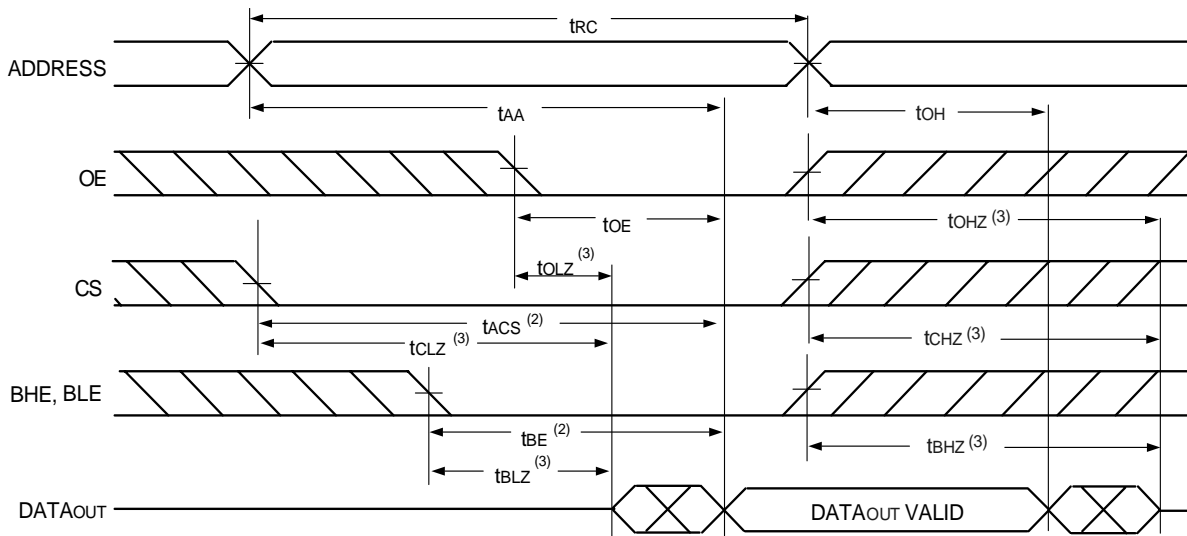
Timing Waveform of Read Cycle No. 1[1,2,3]
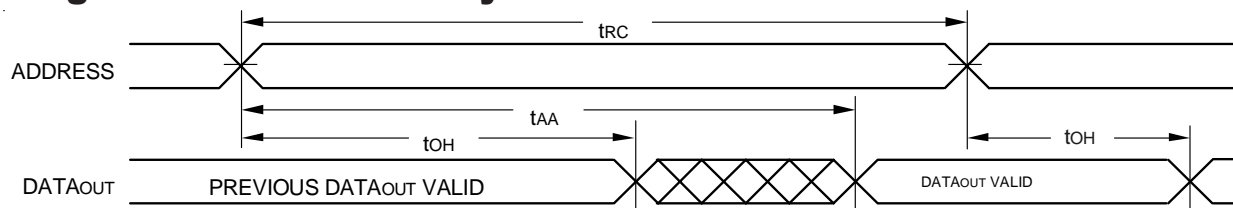
6442d06

NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. $\overline{OE}$, $\overline{BHE}$, and $\overline{BLE}$ are LOW.
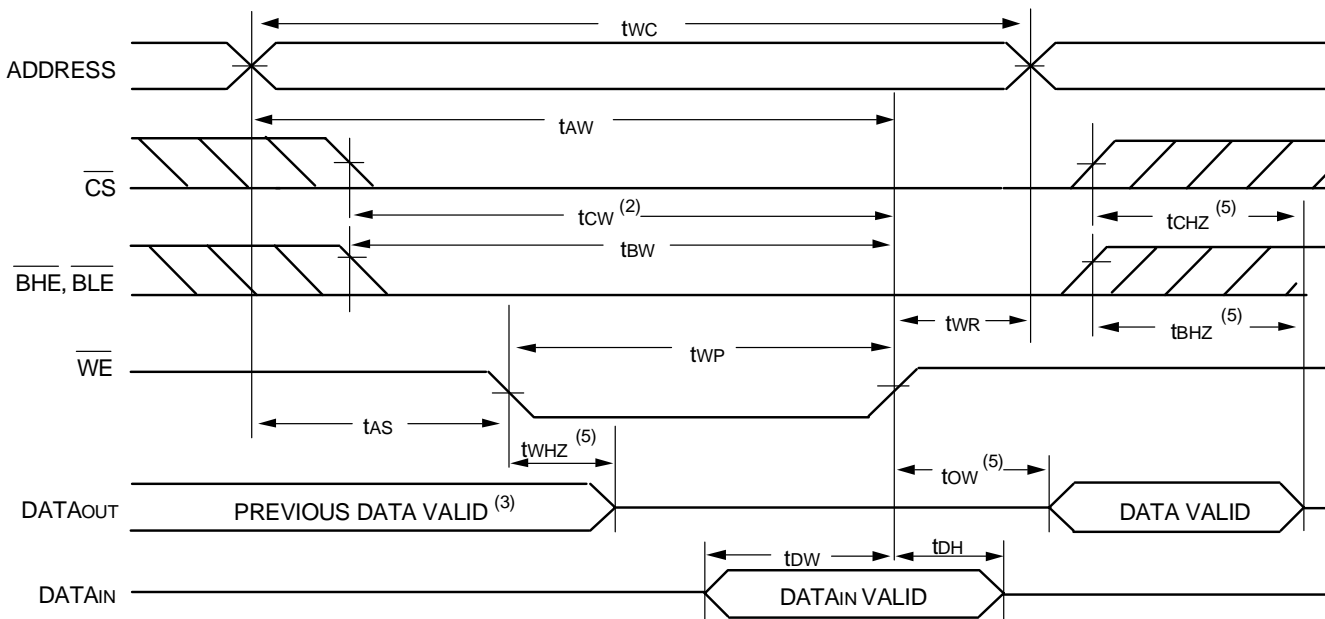
Timing Waveform of Read Cycle No. 2[1]

6442 drw 07

NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Address must be valid prior to or coincident with the later of $\overline{CS}$, $\overline{BHE}$, or $\overline{BLE}$ transition LOW; otherwise t_{AA} is the limiting parameter.
3. Transition is measured ±200mV from steady state.

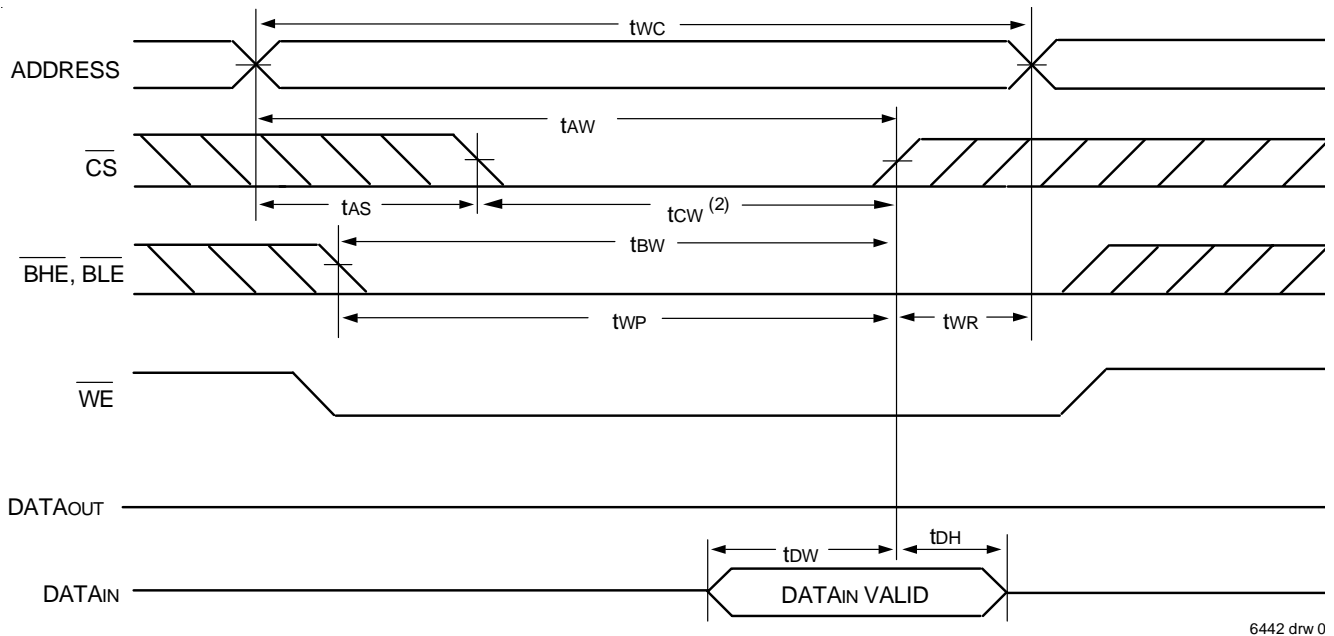## Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled Timing)[1,2,4]

6442 drw 0

NOTES:
1. A write occurs during the overlap of a LOW $\overline{CS}$, LOW $\overline{BHE}$ or $\overline{BLE}$, and a LOW $\overline{WE}$.
2. $\overline{OE}$ is continuously HIGH. If during a $\overline{WE}$ controlled write cycle $\overline{OE}$ is LOW, t_{WP} must be greater than or equal to t_{WHZ} + t_{DW} to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified t_{WP}.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the $\overline{CS}$ LOW or $\overline{BHE}$ and $\overline{BLE}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
5. Transition is measured ±200mV from steady state.

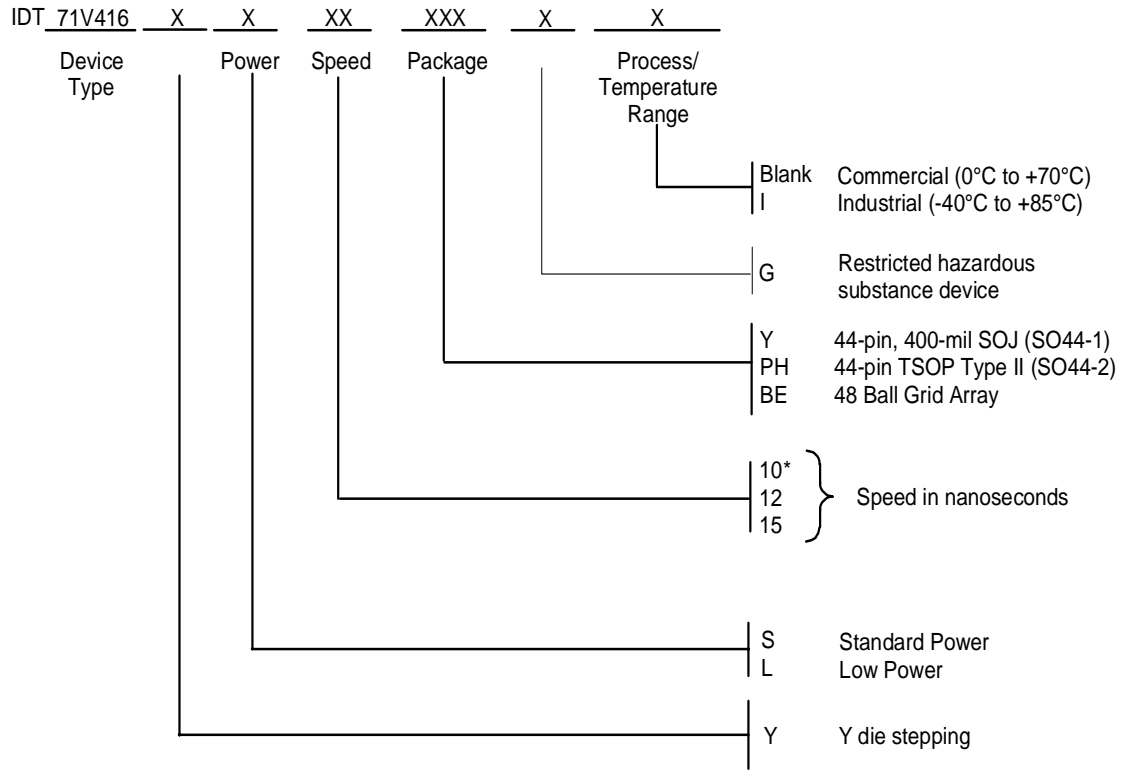## Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled Timing)[1,3]

6442 drw 0

Timing Waveform of Write Cycle No. 3 ($\overline{BHE}$, $\overline{BLE}$ Controlled Timing)[1,3]

6442 drw 1
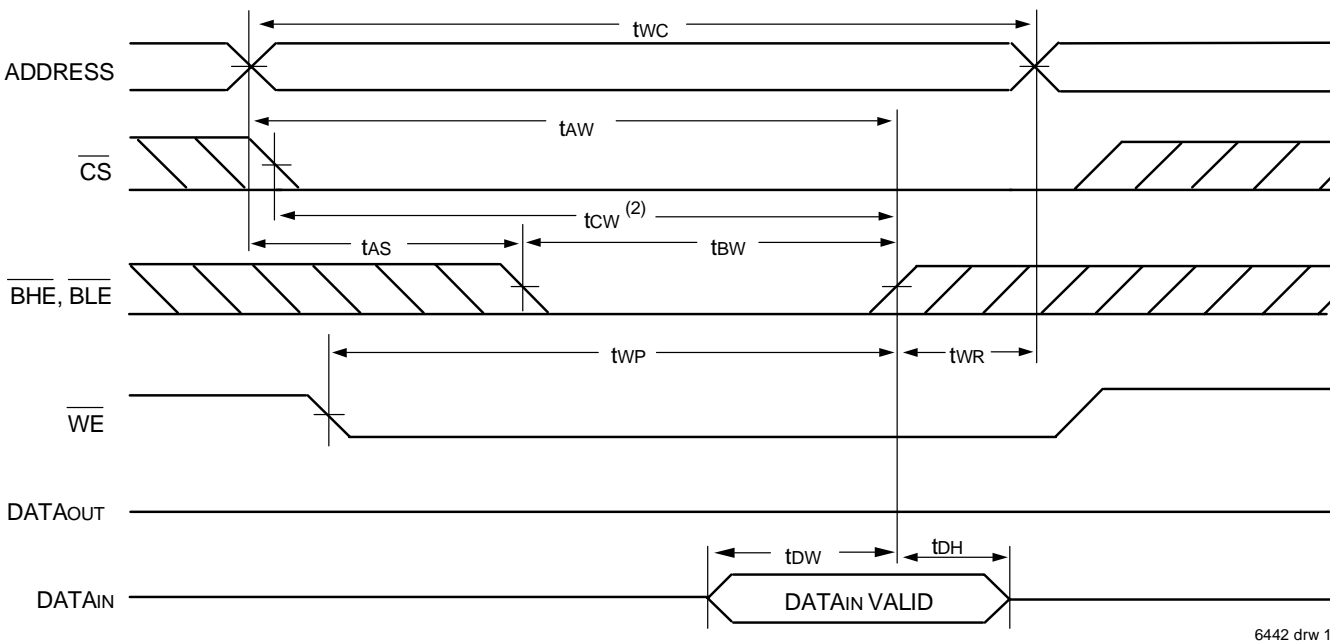
NOTES:
1. A write occurs during the overlap of a LOW $\overline{CS}$, LOW $\overline{BHE}$ or $\overline{BLE}$, and a LOW $\overline{WE}$.
2. During this period, I/O pins are in the output state, and input signals must not be applied.
3. If the $\overline{CS}$ LOW or $\overline{BHE}$ and $\overline{BLE}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.

Ordering Information

```
IDT  71V416    X    X    XX    XXX    X    X
     Device         Power Speed Package  Process/
     Type                              Temperature
                                         Range
```

Blank	Commercial (0°C to +70°C)
I	Industrial (-40°C to +85°C)

G	Restricted hazardous substance device

Y	44-pin, 400-mil SOJ (SO44-1)
PH	44-pin TSOP Type II (SO44-2)
BE	48 Ball Grid Array

10*	
12	} Speed in nanoseconds
15	

S	Standard Power
L	Low Power

Y	Y die stepping

* Commercial only for low power 10ns (L10) speed grade.

6442 drw 11a

Datasheet Document History

10/13/03		Released datasheet
07/30/04	p.8	Added "Restricted hazardous substance device " to ordering information.

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