INTERSIL

IM65X08/IM65X18
1024 Bit (1024 x 1) High Speed CMOS RAM

FEATURES
- **Low Standby Power: 55μW Maximum**
- **Low Operating Power: 10mW/MHz Maximum**
- **High Speed Operation**
- **High Noise Immunity**
- **Data Retention to V_{CC} = 2.0V**
- **TTL Compatible Inputs and Outputs**
- **Three-State Outputs**
- **High Output Drive = 2 TTL Loads**
- **On-Chip Address Registers**
- **Completely Static and Synchronous**
- **Two Chip Selects (IM65X18)**
- **Military and Industrial Temperature Ranges**
- **Operating Voltage Range 4.5V to 10.5V (A Version)**

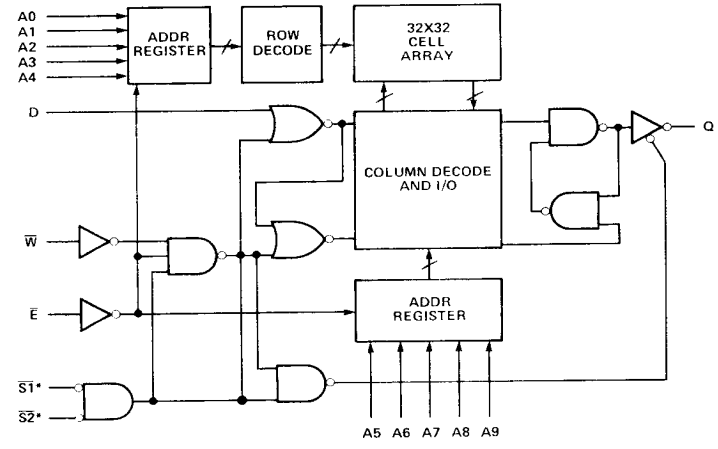
GENERAL DESCRIPTION
The IM65X08 and IM65X18 are high speed, low power CMOS static RAMs organized 1,024 words by 1 bit. Inputs and three-state outputs are TTL compatible and allow for direct interface with common system bus architectures. On-chip address registers and two chip-selects (65X18) simplify system interfacing requirements.

These devices are fully compatible with the industry standard 6508/18 CMOS 1K x 1 RAMs but are fabricated in SELOX C, a CMOS process that uses selective oxidation to achieve higher reliability and performance.

The standard parts operate from 4.5 to 5.5 volts, with access times of 250 ns and standby supply currents of 10 μa guaranteed over operating temperature range. Access times of 180 ns are offered in "-1" versions. High operating voltage range is offered in "A" versions.

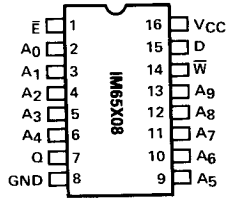
Minimum standby current is drawn when $\overline{E}$ is held at CMOS V_{CC} and all address, data and control lines are held at either CMOS V_{CC} or GND. Data retention is guaranteed to a CMOS V_{CC} of 2.0V.

BLOCK DIAGRAM (IM65X18)

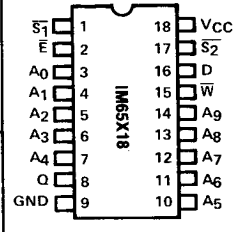


*IM65X08 FUNCTIONS AS IF $\overline{E}$, $\overline{S1}$, $\overline{S2}$, WERE TIED TOGETHER

PIN CONFIGURATION



(outline dwg JE, PE)



TOP VIEW

(outline dwg JN, PN)

Flatpaks (FE, FN) have same pin outs as above

ORDERING INFORMATION

	COMMERCIAL	INDUSTRIAL				MILITARY*			
IM65X08	STD 5V	STD 5V	STD 10V	HI SPEED 5V	HI SPEED 10V	STD 5V	STD 10V	STD 10v	HI SPEED 5v
16 pin Cerdip	CJE	IJE	AIJE	– 1IJE	A-1IJE	MJE	AMJE	A-1MJE	– 1MJE
16 pin Plastic Dip	CPE	IPE	AIPE	– 1IPE	A-1IPE				
16 pin Flatpak						MFE	AMFE	A-1AMFE	– 1MFE
IM65X18									
18 pin Cerdip	CJN	IJN	AIJN	– 1IJN	A-1IJN	MJN	AMJN	A-1MJN	– 1MJN
18 pin Plastic Dip	CPN	IPN	AIPN	– 1IPN	A-1IPN				
18 pin Flatpak						MFN	AMFN	A-1MFN	– 1MFN

* For 883B processing add /883B to order number.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +8.0V
Input or Output Voltage Applied ..... GND −0.3V to V_{CC} +0.3V
Storage Temperature Range ..... −65°C to +150°C
Operating Ranges
  Temperature
    Industrial ..... −40°C to +85°C
    Military ..... −55°C to +125°C
  Voltage
    IM65X08/X18 ..... 4.5V-5.5V

DC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ± 10%, T_A = Operating Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		V_{CC}-2.0			V
Logical "0" Input Voltage	V_{IL}				0.8	
Input Leakage	I_I	GND ≤ V_{IN} ≤ V_{CC}	-1.0		+1.0	μA
Logical "1" Output Voltage	V_{OH}	I_{OH} = 0	V_{CC}-0.01			V
		I_{OH} = −0.4 mA	2.4			
Logical "0" Output Voltage	V_{OL}	I_{OL} = 0			GND +0.01	
		I_{OL} = 3.2 mA			0.4	
Output Leakage	I_O		-1.0		+1.0	μA
IM65X08/X18	I_{CCSB}	V_{IN} = V_{CC}		1.0	10	
	I_{CCSB}	V_{CC} = 3.0V = $\overline{E}$		0.1	10	
Operating Supply Current	I_{CCOP}	f = 1MHz, V_{IN} = V_{CC} or GND, I_O = 0			2	mA
Input Capacitance	C_I			5.0	7.0	pF
Output Capacitance	C_O			6.0	10.0	

AC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ± 10%, C_L = 50pF, T_A = Operating Temperature Range

PARAMETER	SYMBOL	IM65X08/X18 MIN	IM65X08/X18 MAX	UNITS
Access Time From $\overline{E}$	TELQV		250	ns
Output Enable Time	TSLQX		160	
Output Disable Time	TSHQZ		160	
$\overline{E}$ Pulse Width (Pos)	TEHEL	100		
$\overline{E}$ Pulse Width (Neg)	TELEH	250		
$\overline{W}$ Pulse Width (Neg)	TWLWH	130		
Address Setup Time	TAVEL	15		
Address Hold Time	TELAX	50		
Data Setup Time	TDVEH	110		
Data Hold Time	TEHDX	0		

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +8.0V
Input or Output, Voltage Applied ..... GND −0.3V to V_{CC} +.3V
Storage Temperature Range ..... −65°C to +150°C
Operating Ranges
  Temperature
    Industrial ..... −40°C to +85°C
    Military ..... −55°C to +125°C
  Voltage
    IM65X08-1/X18-1 ..... 4.5V to 5.5V

DC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ±10%, T_A = Operating Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		V_{CC} −2.0V			V
Logical "0" Input Voltage	V_{IL}				0.8	
Input Leakage	I_{ILK}	GND ≤ V_{IN} ≤ V_{CC}	−1.0		+1.0	µA
Logical "1" Output Voltage	V_{OH}	I_{OUT} = 0	V_{CC}−0.01			V
	V_{OH}	I_{OUT} = −0.4 mA	2.4			
Logical "0" Output Voltage	V_{OL}	I_{OUT} = 0			GND +0.01	
	V_{OL}	I_{OUT} = 3.2 mA			0.4	
Output Leakage	I_{OLK}	GND ≤ V_O ≤ V_{CC}	−1.0		+1.0	µA
Standby Supply Current IM65X08-1/X18-1	I_{CCSB}	V_{IN} = V_{CC}		1.0	10	
	I_{CCSB}	V_{CC} = 3V = $\overline{E}$		0.01	10	
Operating Supply Current	I_{CCOP}	f = 1MHz, V_{IN} = V_{CC} or GND, I_O = 0			2	mA
Input Capacitance	C_{IN}			5.0	7.0	pF
Output Capacitance	C_O			6.0	10.0	

AC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ±10%, C_L = 50pF, T_A = Operating Temperature Range

PARAMETER	SYMBOL	IM65X08-1/X18-1 MIN	IM65X08-1/X18-1 MAX	UNITS
Access Time From $\overline{E}$	TELQV		180	ns
Output Enable Time	TSLQX		120	
Output Disable Time	TSHQZ		120	
$\overline{E}$ Pulse Width (Pos)	TEHEL	100		
$\overline{E}$ Pulse Width (Neg)	TELEH	180		
$\overline{W}$ Pulse Width (Neg)	TWLWH	100		
Address Setup Time	TAVEL	10		
Address Hold Time	TELAX	40		
Data Setup Time	TDVEH	80		
Data Hold Time	TEHDX	0		

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +12.0V
Input or Output, Voltage Applied ..... GND −0.3V to V_{CC} to .3V
Storage Temperature Range ..... −65°C to +150°C
Operating Ranges
  Temperature
    Industrial ..... −40°C to +85°C
    Military ..... −55°C to +125°C
  Voltage
    IM65X08A/X18A ..... 4.5V to 10.5V
    IM65X08A-1/X18A-1 ..... 4.5V to 10.5V

DC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 4.5V to 10.5V, T_A = Operating Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		70% V_{CC}			V
Logical "0" Input Voltage	V_{IL}				0.8	
Input Leakage	I_{ILK}	$0V \le V_{IN} \le V_{CC}$	−1.0		+1.0	μA
Logical "1" Output Voltage	V_{OH}	$I_{OUT} = 0$	V_{CC}−0.01			V
Logical "0" Output Voltage	V_{OL}	$I_{OUT} = 0$			GND +0.01	
Output Leakage	I_{OLK}	$0V \le V_O \le V_{CC}$	−1.0		+1.0	μA
Standby Supply Current IM65X08A-1/X18A-1	I_{CCSB}	$V_{IN} = V_{CC}$		5.0	500	
	I_{CCSB}	$V_{CC} = 3V = \overline{E}_1$		0.1	50	
IM65X08A/X18A	I_{CCSB}	$V_{IN} = V_{CC}$		5.0	500	
	I_{CCSB}	$V_{CC} = 3V = \overline{E}_1$		0.1	50	
Operating Supply Current	I_{CCOP}	f = 1MHz, $V_{IN} = V_{CC}$ or GND, $I_O = 0$			10	mA
Input Capacitance	C_{IN}			5.0	7.0	pF
Output Capacitance	C_O			6.0	10.0	

AC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 10V ± 5%, C_L = 50pf, T_A = Operating Temperature Range

PARAMETER	SYMBOL	IM65X08A-1/X18A-1		IM65X08A/X18A		UNITS
		MIN	MAX	MIN	MAX	
Access Time From $\overline{E}$	TELQV		125		200	ns
Output Enable Time	TSLQX		75		120	
Output Disable Time	TSHQZ		75		120	
$\overline{E}$ Pulse Width (Pos)	TEHEL	85		125		
$\overline{E}$ Pulse Width (Neg)	TELEH	125		200		
$\overline{W}$ Pulse Width (Neg)	TWLWH	85		125		
Address Setup Time	TAVEL	10		15		
Address Hold Time	TELAX	40		60		
Data Setup Time	TDVEH	85		125		
Data Hold Time	TEHDX	0		0		

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IM65X08C/X18C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 8.0V
Input or Output Voltage Applied ..... GND −0.3V to VCC +0.3V
Storage Temperature Range ..... −65°C to +150°C
Operating Ranges
  Temperature
    Commercial ..... 0°C to 75°C
  Voltage
    IM6508C/18C 4.75V-5.25V

DC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ± 5%, T_A = Operating Temperature Range

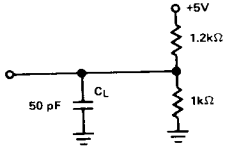
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		V_{CC}−2.0			V
Logical "0" Input Voltage	V_{IL}				0.8	
Input Leakage	I_{ILK}	0V ≤ V_{IN} ≤ V_{CC}	−1.0		+1.0	μA
Logical "1" Output Voltage	V_{OH}	I_{OUT} = 0	V_{CC}−0.01			V
		I_{OH} = −0.2 mA	2.4			
Logical "0" Output Voltage	V_{OL}	I_{OUT} = 0			GND ±0.01	
		I_{OL} = 1.6mA			0.4	
Output Leakage	I_{OLK}	GND ≤ V_O ≤ V_{CC}	−5.0		+5.0	
Standby Supply Current	I_{CCSB}	V_{IN} = V_{CC}		10	100	μA
Operating Supply Current	I_{CCOP}	f = 1MHz, V_{IN} = V_{CC} or GND, I_O = 0			4	mA
Input Capacitance	C_{IN}			5.0	7.0	pF
Output Capacitance	C_O			6.0	10.0	

AC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ± 5%, C_L = 50pF, T_A = Operating Temperature Range

PARAMETER	SYMBOL	IM6508C/18C MIN	IM6508C/18C MAX	UNITS
Access Time From $\overline{E}$	TELQV		300	ns
Output Enable Time	TSLQX		200	
Output Disable Time	TSHQZ		200	
$\overline{E}$ Pulse Width (Pos)	TEHEL	150		
$\overline{E}$ Pulse Width (Neg)	TELEH	300		
$\overline{W}$ Pulse Width (Neg)	TWLWH	160		
Address Setup Time	TAVEL	20		
Address Hold Time	TELAX	70		
Data Setup Time	TDVEH	130		
Data Hold Time	TEHDX	0		

AC TEST CIRCUIT



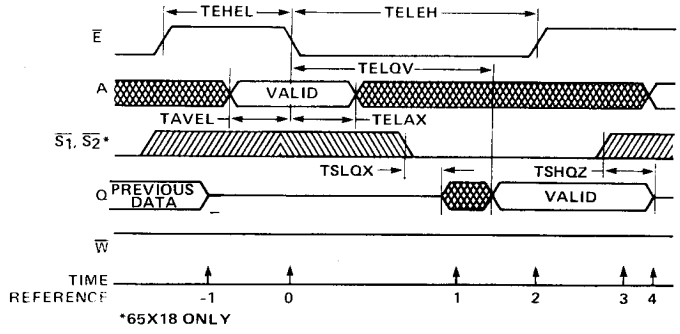
Input Pulse Levels ..... GND to 3.5V
Input Rise and Fall Times ..... $t_r = t_f$ = 10ns
Input and Output Timing
  Reference Level 1.5V

READ MODE OPERATION

In a typical READ operation the address lines are latched by the falling edge of strobe input $\overline{E}$. If the chip has been selected, i.e. $\overline{S}_1$ and $\overline{S}_2$ (65X18 only) are low, data becomes valid an access time (TELQV) after the falling $\overline{E}$ edge. Data out for 65X08 (16 pin) remains valid until $\overline{E}$ returns high. Data out for 65X18 (18 pin) is latched when $\overline{E}$ returns high, and remains valid until a chip select ($\overline{S}_1$ or $\overline{S}_2$) is returned high.

Address information is edge triggered and must be valid a setup time (TAVEL) before and a hold time (TELAX) after the falling $\overline{E}$ edge. $\overline{S}_1$ and $\overline{S}_2$ on the 65X18 are level sensitive and may occur after $\overline{E}$ transition without affecting access time.

READ CYCLE TIMING



FUNCTION TABLE • READ

TIME REF	INPUTS $\overline{E}$	A	$\overline{S}$	$\overline{W}$	OUTPUT Q	NOTES
-1	H	X	H	H	Z	Memory inactive, output high Z
0	↘	V	X	H	Z	Addresses latched, output still high Z
1	L	X	L	H	X	Output enabled and active
2	L	X	L	H	V	Output valid
3	↗	X	L	H	V	Output latched and valid (65X18). Output (65X08).
4	H	X	H	H	Z	Output disabled, high Z. Ready for next cycle.

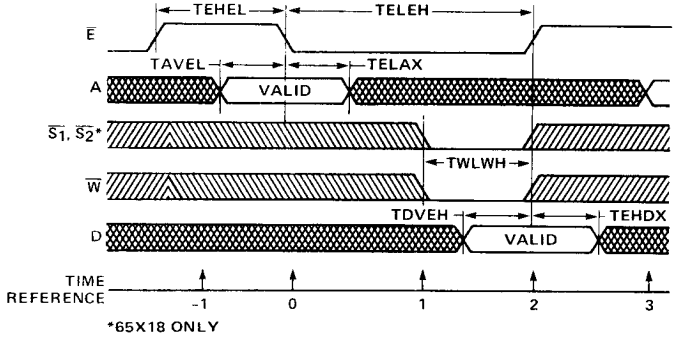
WRITE MODE OPERATION

For a WRITE operation, address lines are latched by $\overline{E}$ as in a READ operation. Writing begins when strobe ($\overline{E}$), chip selects ($\overline{S}_1$, $\overline{S}_2$) and write ($\overline{W}$) are low and ends when one of these lines returns high. Data (D) must be valid a setup time (TDVEH) before and a hold time (TEHDX) after the final rising edge.

Minimum write pulse widths are specified as TWLWH for $\overline{W}$, $\overline{S}_1$ and $\overline{S}_2$. Minimum write pulse width is specified as TELEH for $\overline{E}$.

NOTE: Transitions on strobe line $\overline{E}$ during power down or standby modes may cause change of address or loss of data. When in either mode care must be taken to maintain $\overline{E}$ at CMOS V_{CC} level.

WRITE CYCLE TIMING



FUNCTION TABLE • WRITE

TIME REF	INPUT $\overline{E}$	A	S*	$\overline{W}$	D	OUTPUT Q	NOTES
-1	H	X	H	X	X	Z	Memory inactive, output high Z
0	↘	V	H	X	X	Z	Addresses latched
1	L	X	L	↘	X	Z	Write operation begins
2	L	X	L	↗	V	Z	Write operation ends
3	H	X	H	H	X	Z	Output disabled, high Z. Ready for next cycle.