3.3-V / 5-V HIGH-SPEED DIGITAL ISOLATORS

Check for Samples: ISO721, ISO721M, ISO722, ISO722M

FEATURES

- **4000-$V_{(peak)}$ Isolation, 560-V_{peak} V_{IORM}**
  - **UL 1577, IEC 60747-5-2 (VDE 0884, Rev. 2) IEC 61010-1, IEC 60950-1 and CSA Approved**
  - **50 kV/μs Transient Immunity, Typical**
- **Signaling Rate 0 Mbps to 150 Mbps**
  - **Low Propagation Delay**
  - **Low Pulse Skew (Pulse-Width Distortion)**
- **Low-Power Sleep Mode**
- **High Electromagnetic Immunity**
- **Low Input-Current Requirement**
- **Failsafe Output**
- **Drop-In Replacement for Most Opto and Magnetic Isolators**

APPLICATIONS

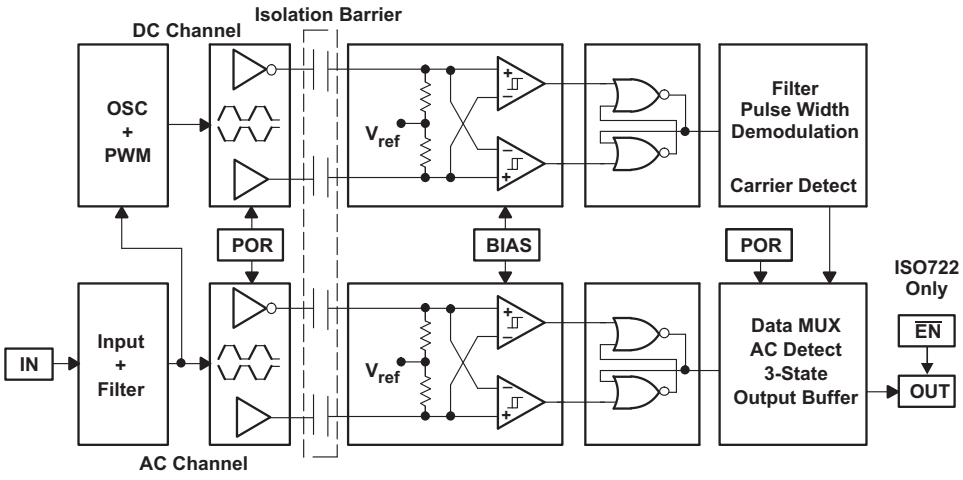
- **Industrial Fieldbus**
  - **Modbus**
  - **Profibus**
  - **DeviceNet™ Data Buses**
  - **Smart Distributed Systems (SDS™)**
- **Computer Peripheral Interface**
- **Servo Control Interface**
- **Data Acquisition**

DESCRIPTION

The ISO721, ISO721M, ISO722, and ISO722M are digital isolators with a logic input and output buffer separated by a silicon dioxide (SiO_2) insulation barrier. This barrier provides galvanic isolation of up to 4000 V. Used in conjunction with isolated power supplies, these devices prevent noise currents on a data bus or other circuits from entering the local ground, and interfering with or damaging sensitive circuitry.

A binary input signal is conditioned, translated to a balanced signal, then differentiated by the capacitive isolation barrier. Across the isolation barrier, a differential comparator receives the logic transition information, then sets or resets a flip-flop and the output circuit accordingly. A periodic update pulse is sent across the barrier to ensure the proper dc level of the output. If this dc-refresh pulse is not received for more than 4 μs, the input is assumed to be unpowered or not being actively driven, and the failsafe circuit drives the output to a logic-high state.

FUNCTION DIAGRAM



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SDS is a trademark of Honeywell.
DeviceNet is a trademark of Open Devicenet Vendors Association, Inc.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

The symmetry of the dielectric and capacitor within the integrated circuitry provides for close capacitive matching, and allows fast transient voltage changes between the input and output grounds without corrupting the output. The small capacitance and resulting time constant provide for fast operation with signaling rates(1) from 0 Mbps (dc) to 100 Mbps for the ISO721/ISO722, and 0 Mbps to 150 Mbps with the ISO721M/ISO722M.

These devices require two supply voltages of 3.3-V, 5-V, or any combination. All inputs are 5-V tolerant when supplied from a 3.3-V supply and all outputs are 4-mA CMOS.

The ISO722 and ISO722M devices include an active-low output enable that when driven to a high logic level, places the output in a high-impedance state and turns off internal bias circuitry to conserve power.

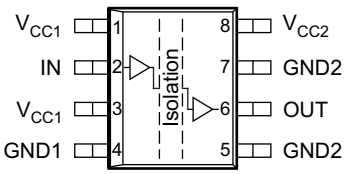
Both the ISO721 and ISO722 have TTL input thresholds and a noise filter at the input that prevent transient pulses of up to 2 ns in duration from being passed to the output of the device.

The ISO721M and ISO722M have CMOS $V_{CC}/2$ input thresholds, but do not have the noise-filter and the additional propagation delay. These features of the ISO721M also provide for reduced-jitter operation.

The ISO721, ISO721M, ISO722, and ISO722M are characterized for operation over the ambient temperature range of –40°C to 125°C.

(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

ISO721, ISO721M
D Package
(Top View)



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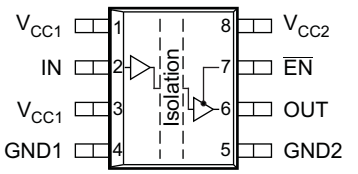
ISO722, ISO722M
D Package
(Top View)



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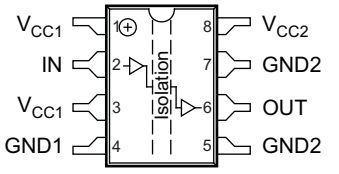
ISO721
DUB Package
(Top View)



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AVAILABLE OPTIONS

PRODUCT	OUTPUT ENABLED	INPUT THRESHOLDS	NOISE FILTER	PACKAGE(1)	MARKED AS	ORDERING NUMBER
ISO721	NO	TTL	YES	D-8	ISO721	ISO721D (rail)
						ISO721DR (reel)
				DUB-8		ISO721DUB (rail)
						ISO721DUBR (reel)
ISO721M	NO	CMOS	NO	D-8	IS721M	ISO721MD (rail)
						ISO721MDR (reel)
ISO722	YES	TTL	YES	D-8	ISO722	ISO722D (rail)
						ISO722DR (reel)
ISO722M	YES	CMOS	NO	D-8	IS722M	ISO722MD (rail)
						ISO722MDR (reel)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

Table 1. REGULATORY INFORMATION

VDE	CSA	UL
Certified according to IEC 60747-5-2	Approved under CSA Component Acceptance notice: CA-5A	Recognized under 1577 Component Recognition Program(1)
File number: 40016131	File number: 1698195	File number: E181974

(1) Production tested ≥ 3000 V_{RMS} for 1 second in accordance with UL 1577.

ABSOLUTE MAXIMUM RATINGS(1)

					UNIT
V_{CC}	Supply voltage(2), V_{CC1}, V_{CC2}				–0.5 V to 6 V
V_I	Voltage at IN, OUT, or $\overline{EN}$ terminal				–0.5 V to 6 V
I_O	Output current				±15 mA
ESD	Electrostatic discharge	Human-body model	JEDEC Standard 22, Test Method A114-C.01	All pins	±2 kV
		Charged-device model	JEDEC Standard 22, Test Method C101		±1 kV
T_J	Maximum junction temperature				170°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values. Vrms values are not listed in this publication.

RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage(1), V_{CC1}, V_{CC2}		3		5.5	V
I_{OH}	Output current				4	mA
I_{OL}			–4			
t_{ui}	Input pulse duration	ISO72x	10			ns
		ISO72xM	6.67			
V_{IH}	High-level input voltage (IN, $\overline{EN}$)	ISO72x	2		V_{CC}	V
V_{IL}	Low-level input voltage (IN, $\overline{EN}$)		0		0.8	
V_{IH}	High-level input voltage (IN, $\overline{EN}$)	IOS72xM	0.7 V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage (IN, $\overline{EN}$)		0		0.3 V_{CC}	
T_J	Junction temperature	See the Thermal Characteristics table			150	°C
H	External magnetic field intensity per IEC 61000-4-8 and IEC 61000-4-9 certification				1000	A/m

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V. For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

INSULATION CHARACTERISTICS(1)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SPECIFICATIONS	UNIT
V_{IORM}	Maximum working insulation voltage		560	Vpeak
V_{PR}	Input to output test voltage	After Input/Output Safety Test Subgroup 2/3 $V_{PR} = V_{IORM} \times 1.2$, t = 10 s, Partial discharge < 5 pC	672	Vpeak
		Method a, $V_{PR} = V_{IORM} \times 1.6$, Type and sample test with t = 10 s, Partial discharge < 5 pC	896	Vpeak
		Method b1, $V_{PR} = V_{IORM} \times 1.875$, 100% production test with t = 1 s, Partial discharge < 5 pC	1050	Vpeak
V_{IOTM}	Transient overvoltage	t = 60 s	4000	Vpeak
V_{ISO}	Isolation voltage per UL	$V_{TEST} = V_{ISO}$, t = 60 s (qualification)	3535 / 2500	Vpeak/Vrms
		$V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)(2)	4242 / 3000	
R_S	Insulation resistance	V_{IO} = 500 V at T_S	$>10^9$	Ω
	Pollution degree		2	

(1) Climatic classification 40/125/21
(2) Based on lifetime curve (see the *High-Voltage Lifetime of the ISO72x Family of Digital Isolators* application report, SLLA197); these devices can withstand 4242 Vpeak / 3000 Vrms for > 10,000 s at 150°C.

ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} 5-V(1) OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC1}	V_{CC1} supply current	Quiescent	V_I = V_{CC} or 0 V, no load			0.5	1	mA
		25 Mbps				2	4	
I_{CC2}	V_{CC2} supply current	ISO722/722M Sleep Mode	V_I = V_{CC} or 0 V, No load	$\overline{EN}$ at V_{CC}			200	µA
		Quiescent		$\overline{EN}$ at 0 V or ISO721/721M		8	12	mA
		25 Mbps	V_I = V_{CC} or 0 V, no load			10	14	
V_{OH}	High-level output voltage		I_{OH} = -4 mA, See Figure 1		V_{CC} – 0.8	4.6		V
			I_{OH} = –20 µA, See Figure 1		V_{CC} – 0.1	5		
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 1			0.2	0.4	V
			I_{OL} = 20 µA, See Figure 1			0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current		$\overline{EN}$, IN at 2 V				10	µA
I_{IL}	Low-level input current		$\overline{EN}$, IN at 0.8 V		–10			
I_{OZ}	High-impedance output current	ISO722, ISO722M	$\overline{EN}$, IN at V_{CC}				1	µA
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)			1		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V, See Figure 5		25	50		kV/µs

(1) For 5-V operation, V_{CC1} and V_{CC2} are specified from 4.5 V to 5.5 V.

SWITCHING CHARACTERISTICS: V_{CC1} and V_{CC2} 5-V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay, low-to-high-level output	ISO72x	$\overline{EN}$ at 0 V, See Figure 1	13	17	24	ns
t_{PHL}	Propagation delay, high-to-low-level output			13	17	24	ns
$t_{sk(p)}$	Pulse skew $\|t_{PHL} – t_{PLH}\|$				0.5	2	ns
t_{PLH}	Propagation delay, low-to-high-level output	ISO72xM		8	10	16	ns
t_{PHL}	Propagation delay, high-to-low-level output			8	10	16	ns
$t_{sk(p)}$	Pulse skew $\|t_{PHL} – t_{PLH}\|$				0.5	1	ns
$t_{sk(pp)}$ (1)	Part-to-part skew				0	3	ns
t_r	Output signal rise time		$\overline{EN}$ at 0 V, See Figure 1		1		ns
t_f	Output signal fall time				1		
t_{pHZ}	Sleep-mode propagation delay, high-level-to-high-mpedance output	ISO722 ISO722M	See Figure 2	6	8	15	ns
t_{pZH}	Sleep-mode propagation delay, high-impedance-to-high-level output			3.5	4	8	µs
t_{pLZ}	Sleep-mode propagation delay, low-level-to-high-impedance output		See Figure 3	5.5	8	15	ns
t_{pZL}	Sleep-mode propagation delay, high-impedance-to-low-level output			4	5	8	µs
t_{fs}	Failsafe output delay time from input power loss		See Figure 4		3		µs
$t_{jit(PP)}$	Peak-to-peak eye-pattern jitter	ISO72x	100-Mbps NRZ data input, See Figure 6		2		ns
			100-Mbps unrestricted bit run length data input, See Figure 6		3		
		ISO72xM	150-Mbps NRZ data input, See Figure 6		1		
			150-Mbps unrestricted bit run length data input, See Figure 6		2		

(1) $t_{sk(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

ELECTRICAL CHARACTERISTICS: V_{CC1} at 5-V, V_{CC2} at 3.3-V[1] OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC1}	V_{CC1} supply current	Quiescent	V_I = V_{CC} or 0 V, no load			0.5	1	mA
		25 Mbps				2	4	
I_{CC2}	V_{CC2} supply current	ISO722/722M Sleep mode	V_I = V_{CC} or 0 V, No load	$\overline{EN}$ at V_{CC}			150	µA
		Quiescent		$\overline{EN}$ at 0 V or ISO721/721M		4	6.5	mA
		25 Mbps	V_I = V_{CC} or 0 V, no load			5	7.5	
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 1		V_{CC} – 0.4	3		V
			I_{OH} = –20 µA, See Figure 1		V_{CC} – 0.1	3.3		
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 1			0.2	0.4	V
			I_{OL} = 20 µA, See Figure 1			0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current		$\overline{EN}$, IN at 2 V				10	µA
I_{IL}	Low-level input current		$\overline{EN}$, IN at 0.8 V		–10			µA
I_{OZ}	High-impedance output current	ISO722, ISO722M	$\overline{EN}$, IN at V_{CC}				1	µA
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)			1		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V, See Figure 5		25	40		kV/µs

(1) For 5-V operation, V_{CC1} is specified from 4.5 V to 5.5 V. For 3.3-V operation, V_{CC2} is specified from 3 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} at 5-V, V_{CC2} at 3.3-V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay, low-to-high-level output	ISO72x	$\overline{EN}$ at 0 V, See Figure 1	15	19	30	ns
t_{PHL}	Propagation delay , high-to-low-level output			15	19	30	ns
$t_{sk(p)}$	Pulse skew $\|t_{PHL} - t_{PLH}\|$				0.5	3	ns
t_{PLH}	Propagation delay, low-to-high-level output	ISO72xM		10	12	20	ns
t_{PHL}	Propagation delay, high-to-low-level output			10	12	20	ns
$t_{sk(p)}$	Pulse skew $\|t_{PHL} - t_{PLH}\|$				0.5	1	ns
$t_{sk(pp)}$ (1)	Part-to-part skew				0	5	ns
t_r	Output signal rise time		$\overline{EN}$ at 0 V, See Figure 1		2		ns
t_f	Output signal fall time				2		ns
t_{pHZ}	Sleep-mode propagation delay, high-level-to-high-mpedance output	ISO722 ISO722M	See Figure 2	7	11	25	ns
t_{pZH}	Sleep-mode propagation delay, high-impedance-to-high-level output			4.5	6	8	µs
t_{pLZ}	Sleep-mode propagation delay, low-level-to-high-impedance output		See Figure 3	7	13	25	ns
t_{pZL}	Sleep-mode propagation delay, high-impedance-to-low-level output			4.5	6	8	µs
t_{fs}	Failsafe output delay time from input power loss		See Figure 4		3		µs
$t_{jit(PP)}$	Peak-to-peak eye-pattern jitter	ISO72x	100-Mbps NRZ data input, See Figure 6		2		ns
			100-Mbps unrestricted bit run length data input, See Figure 6		3		
		ISO72xM	150-Mbps NRZ data input, See Figure 6		1		
			150-Mbps unrestricted bit run length data input, See Figure 6		2		

(1) $t_{sk(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

ELECTRICAL CHARACTERISTICS: V_{CC1} at 3.3-V, V_{CC2} at 5-V(1) OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC1}	V_{CC1} supply current	Quiescent	V_I = V_{CC} or 0 V, no load			0.3	0.5	mA
		25 Mbps				1	2	
I_{CC2}	V_{CC2} supply current	ISO722/722M Sleep mode	V_I = V_{CC} or 0 V, No load	$\overline{EN}$ at V_{CC}			200	μA
		Quiescent		$\overline{EN}$ at 0 V or ISO721/721M		8	12	mA
		25 Mbps	V_I = V_{CC} or 0 V, No load			10	14	
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 1		V_{CC} – 0.8	4.6		V
			I_{OH} = –20 μA, See Figure 1		V_{CC} – 0.1	5		
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 1			0.2	0.4	V
			I_{OL} = 20 μA, See Figure 1			0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current		$\overline{EN}$, IN at 2 V				10	μA
I_{IL}	Low-level input current		$\overline{EN}$, IN at 0.8 V		–10			μA
I_{OZ}	High-impedance output current	ISO722, ISO722M	$\overline{EN}$, IN at V_{CC}				1	μA
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)			1		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V, See Figure 5		25	40		kV/μs

(1) For 5-V operation, V_{CC2} is specified from 4.5 V to 5.5 V. For 3.3-V operation, V_{CC1} is specified from 3 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} at 3.3-V, V_{CC2} at 5-V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay, low-to-high-level output	ISO72x	$\overline{EN}$ at 0 V, See Figure 1	15	17	30	ns
t_{PHL}	Propagation delay , high-to-low-level output			15	17	30	ns
$t_{sk(p)}$	Pulse skew $\|t_{PHL} - t_{PLH}\|$				0.5	2	ns
t_{PLH}	Propagation delay, low-to-high-level output	ISO72xM		10	12	21	ns
t_{PHL}	Propagation delay, high-to-low-level output			10	12	21	ns
$t_{sk(p)}$	Pulse skew $\|t_{PHL} - t_{PLH}\|$				0.5	1	ns
$t_{sk(pp)}$ (1)	Part-to-part skew				0	5	ns
t_r	Output signal rise time		$\overline{EN}$ at 0 V, See Figure 1		1		ns
t_f	Output signal fall time				1		ns
t_{pHZ}	Sleep-mode propagation delay, high-level-to-high-mpedance output	ISO722 ISO722M	See Figure 2	7	9	15	ns
t_{pZH}	Sleep-mode propagation delay, high-impedance-to-high-level output			4.5	5	8	μs
t_{pLZ}	Sleep-mode propagation delay, low-level-to-high-impedance output		See Figure 3	7	9	15	ns
t_{pZL}	Sleep-mode propagation delay, high-impedance-to-low-level output			4.5	5	8	μs
t_{fs}	Failsafe output delay time from input power loss		See Figure 4		3		μs
$t_{jit(PP)}$	Peak-to-peak eye-pattern jitter	ISO72x	100-Mbps NRZ data input, See Figure 6		2		ns
			100-Mbps unrestricted bit run length data input, See Figure 6		3		
		ISO72xM	150-Mbps NRZ data input, See Figure 6		1		
			150-Mbps unrestricted bit run length data input, See Figure 6		2		

(1) $t_{sk(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} at 3.3-V[1] OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC1}	V_{CC1} supply current	Quiescent	V_I = V_{CC} or 0 V, no load			0.3	0.5	mA
		25 Mbps				1	2	
I_{CC2}	V_{CC2} supply current	ISO722/722M Sleep Mode	V_I = V_{CC} or 0 V, No load	$\overline{EN}$ at V_{CC}			150	μA
		Quiescent		$\overline{EN}$ at 0 V or ISO721/721M		4	6.5	mA
		25 Mbps	V_I = V_{CC} or 0 V, no load			5	7.5	
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 1		V_{CC} – 0.4	3		V
			I_{OH} = –20 μA, See Figure 1		V_{CC} – 0.1	3.3		
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 1			0.2	0.4	V
			I_{OL} = 20 μA, See Figure 1			0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current		$\overline{EN}$, IN at 2 V				10	μA
I_{IL}	Low-level input current		$\overline{EN}$, IN at 0.8 V		–10			μA
I_{OZ}	High-impedance output current	ISO722, ISO722M	$\overline{EN}$, IN at V_{CC}				1	μA
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)			1		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V, See Figure 5		25	40		kV/μs

(1) For the 3.3-V operation, V_{CC1} and V_{CC2} are specified from 3 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} and V_{CC2} at 3.3-V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay, low-to-high-level output	ISO72x	$\overline{EN}$ at 0 V, See Figure 1	17	20	34	ns
t_{PHL}	Propagation delay , high-to-low-level output			17	20	34	ns
$t_{sk(p)}$	Pulse skew $\|t_{PHL} - t_{PLH}\|$				0.5	3	ns
t_{PLH}	Propagation delay, low-to-high-level output	ISO72xM		10	12	25	ns
t_{PHL}	Propagation delay, high-to-low-level output			10	12	25	ns
$t_{sk(p)}$	Pulse skew $\|t_{PHL} - t_{PLH}\|$				0.5	1	ns
$t_{sk(pp)}$ (1)	Part-to-part skew				0	5	ns
t_r	Output signal rise time		$\overline{EN}$ at 0 V, See Figure 1		2		ns
t_f	Output signal fall time				2		
t_{pHZ}	Sleep-mode propagation delay, high-level-to-high-mpedance output	ISO722 ISO722M	See Figure 2	7	13	25	ns
t_{pZH}	Sleep-mode propagation delay, high-impedance-to-high-level output			5	6	8	μs
t_{pLZ}	Sleep-mode propagation delay, low-level-to-high-impedance output		See Figure 3	7	13	25	ns
t_{pZL}	Sleep-mode propagation delay, high-impedance-to-low-level output			5	6	8	μs
t_{fs}	Failsafe output delay time from input power loss		See Figure 4		3		μs
$t_{jit(PP)}$	Peak-to-peak eye-pattern jitter	ISO72x	100-Mbps NRZ data input, See Figure 6		2		ns
			100-Mbps unrestricted bit run length data input, See Figure 6		3		
		ISO72xM	150-Mbps NRZ data input, See Figure 6		1		
			150-Mbps unrestricted bit run length data input, See Figure 6		2		

(1) $t_{sk(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION

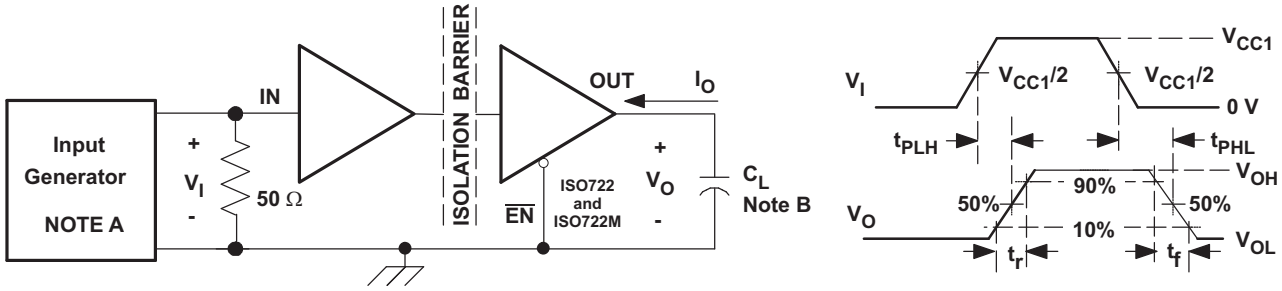


Figure 1. Switching Characteristic Test Circuit and Voltage Waveforms

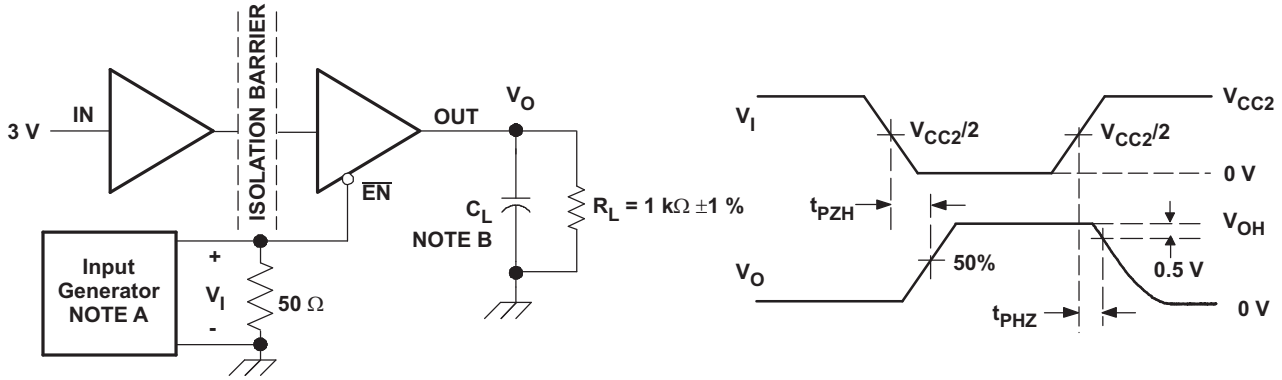


Figure 2. ISO722 Sleep-Mode High-Level Output Test Circuit and Voltage Waveforms

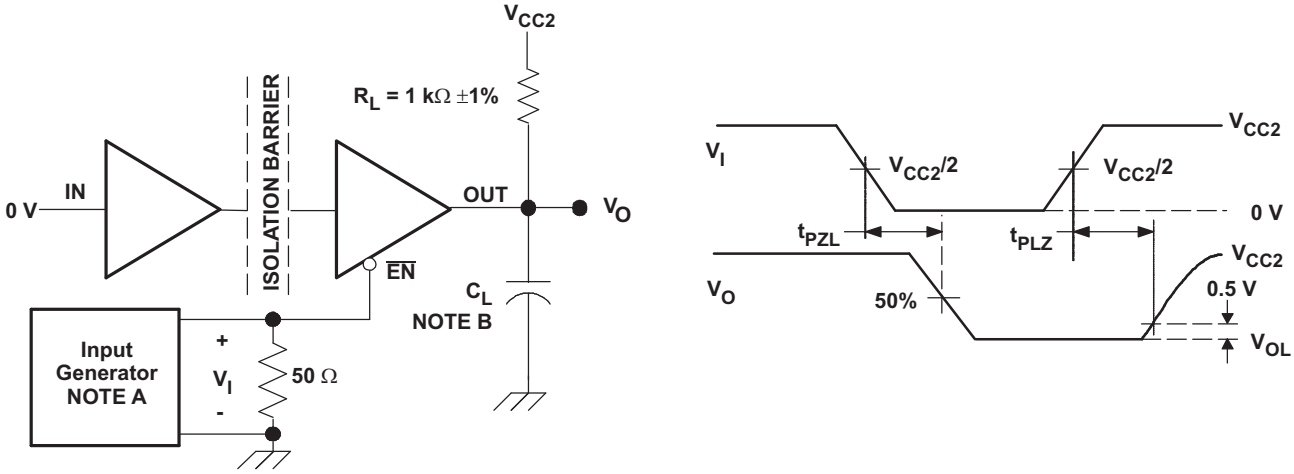


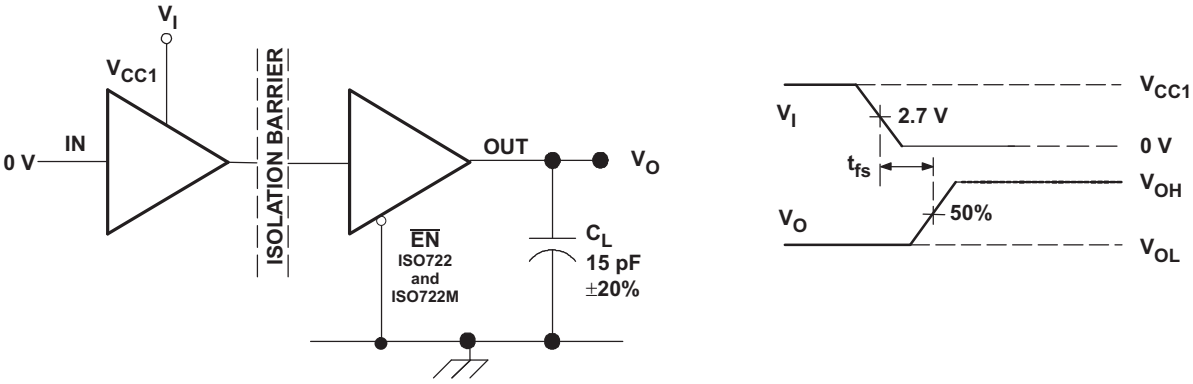
Figure 3. ISO722 Sleep-Mode Low-Level Output Test Circuit and Voltage Waveforms

NOTE

A: The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

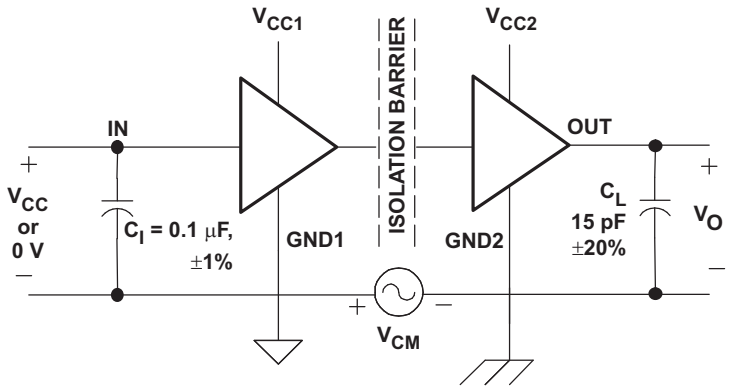
B: C_L = 15 pF ± 20% and includes instrumentation and fixture capacitance.

PARAMETER MEASUREMENT INFORMATION (continued)



NOTE: V_I transition time is 100 ns.

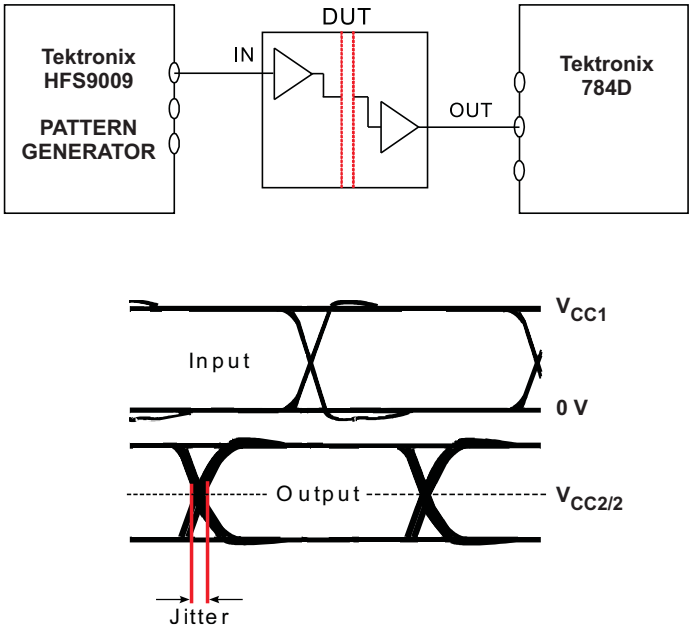
Figure 4. Failsafe Delay Time Test Circuit and Voltage Waveforms



NOTE: Pass/fail criterion is no change in V_O.

Figure 5. Common-Mode Transient-Immunity Test Circuit and Voltage Waveform

PARAMETER MEASUREMENT INFORMATION (continued)



NOTE: Bit pattern run length is 2^{16} – 1. Transition time is 800 ps. NRZ data input has no more than five consecutive 1s or 0s.

Figure 6. Peak-to-Peak Eye-Pattern Jitter Test Circuit and Voltage Waveform

DEVICE INFORMATION

PACKAGE INSULATION CHARACTERISTICS

PARAMETER		DESCRIPTIONS / TEST CONDITIONS		MIN	TYP	MAX	UNIT
L(101)	Minimum air gap (clearance) (1)	Shortest terminal-to-terminal distance through air	D-8	4.8			mm
			DUB-8	6.1			
L(102)	Minimum external tracking (creepage)	Shortest terminal-to-terminal distance across the package surface	D-8	4.3			mm
			DUB-8	6.8			
C_{TI}	Tracking resistance (comparative tracking index)	DIN IEC 60112/VDE 0303 Part 1		≥ 175			V
	Minimum internal gap (internal clearance)	Distance through insulation		0.008			mm
R_{IO}	Isolation resistance	Input to output, V_{IO} = 500 V; all pins on each side of the barrier tied together, creating a two-terminal device; T_A < 100°C			$>10^{12}$		Ω
		Input to output, V_{IO} = 500 V, 100°C ≤ T_A< T_A max.			$>10^{11}$		Ω
C_{IO}	Barrier capacitance Input-to-output	V_I = 0.4 sin (4E6πt)			1		pF
C_I	Input capacitance to ground	V_I = 0.4 sin (4E6πt)			1		pF

(1) Creepage and clearance requirements are applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board do not reduce this distance.

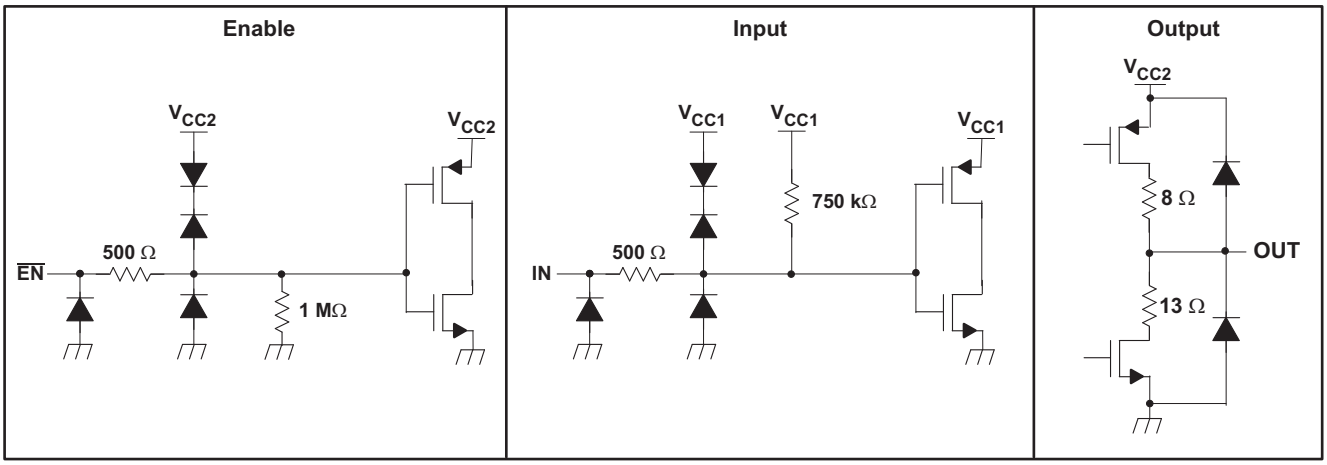
Creepage and clearance on a printed circuit board become equal according to the measurement techniques shown in the *Isolation Glossary*. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

IEC 60664-1 RATINGS TABLE

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	IIIa
Installation classification	Rated mains voltage ≤150 VRMS	I-IV
	Rated mains voltage ≤300 VRMS	I-III

DEVICE I/O SCHEMATIC

Equivalent Input and Output Schematic Diagrams



IEC SAFETY LIMITING VALUES

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply, and without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	θ_{JA} = 263°C/W, V_I = 5.5 V, T_J = 170°C, T_A = 25°C			100	mA
		θ_{JA} = 263°C/W, V_I = 3.6 V, T_J = 170°C, T_A = 25°C			153	
T_S	Maximum case temperature				150	°C

The safety-limiting constraint is the absolute maximum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The junction-to-air thermal resistance in the *Thermal Characteristics* table is that of a device installed in the JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages and is conservative. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

Table 2. THERMAL CHARACTERISTICS for D-8 PACKAGE (over recommended operating conditions unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-air		Low-K thermal resistance(1)		263		°C/W
			High-K thermal resistance(1)		125		°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance				44		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance				75		°C/W
P_D	Device power dissipation	ISO72x	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 100-Mbps 50% duty-cycle square wave			159	mW
		ISO72xM	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 150-Mbps 50% duty-cycle square wave			195	

(1) Tested in accordance with the low-K or high-K thermal metric definition of EIA/JESD51-3 for leaded surface-mount packages.

Table 3. THERMAL CHARACTERISTICS for DUB-8 PACKAGE (over recommended operating conditions unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-air		Low-K thermal resistance(1)		188		°C/W
			High-K thermal resistance(1)		117		°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance				82.1		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance				60		°C/W
P_D	Device power dissipation	ISO721	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 100 Mbps 50% duty cycle square wave			159	mW

(1) Tested in accordance with the low-K or high-K thermal metric definition of EIA/JESD51-3 for leaded surface-mount packages.

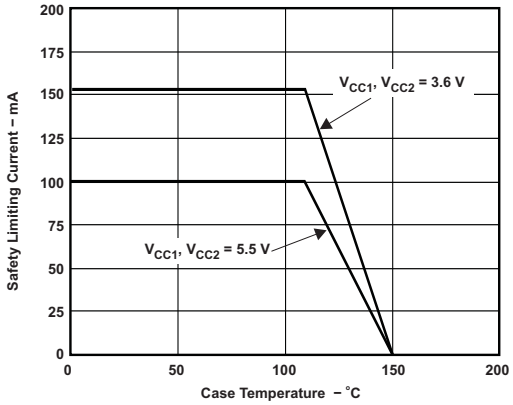


Figure 7. θ_{JC} Thermal Derating Curve per IEC 60747-5-2

FUNCTION TABLE

Table 4. ISO721 (1)

V_{CC1}	V_{CC2}	INPUT (IN)	OUTPUT (OUT)
PU	PU	H	H
		L	L
		Open	H
PD	PU	X	H

(1) PU = Powered up (V_{CC} ≥ 3 V); PD = Powered down (V_{CC} ≤ 2.5 V); X = Irrelevant; H = High level; L = Low level

Table 5. ISO722 (1)

V_{CC1}	V_{CC2}	INPUT (IN)	ISO722/ISO722M OUTPUT ENABLE ($\overline{EN}$)	OUTPUT (OUT)
PU	PU	H	L or open	H
		L	L or open	L
		X	H	Z
		Open	L or open	H
PD	PU	X	L or open	H
PD	PU	X	H	Z

(1) PU = Powered up (V_{CC} ≥ 3 V); PD = Powered down (V_{CC} ≤ 2.5 V); X = Irrelevant; Z = High impedance; H = High level; L = Low level

TYPICAL CHARACTERISTICS

RMS SUPPLY CURRENT vs SIGNALING RATE

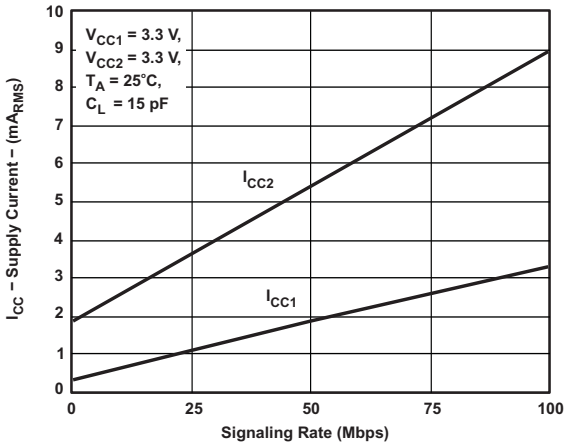


Figure 8.

RMS SUPPLY CURRENT vs SIGNALING RATE

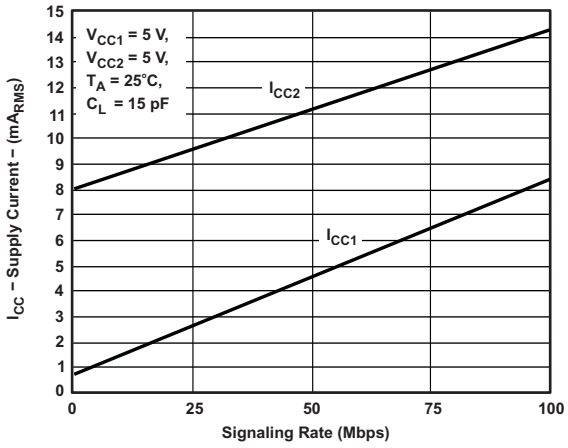


Figure 9.

PROPAGATION DELAY vs FREE-AIR TEMPERATURE

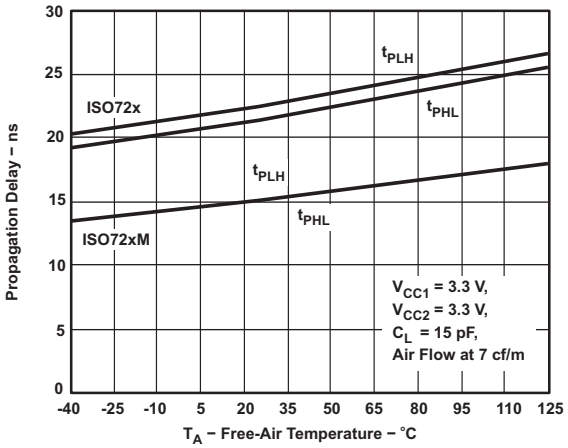


Figure 10.

PROPAGATION DELAY vs FREE-AIR TEMPERATURE

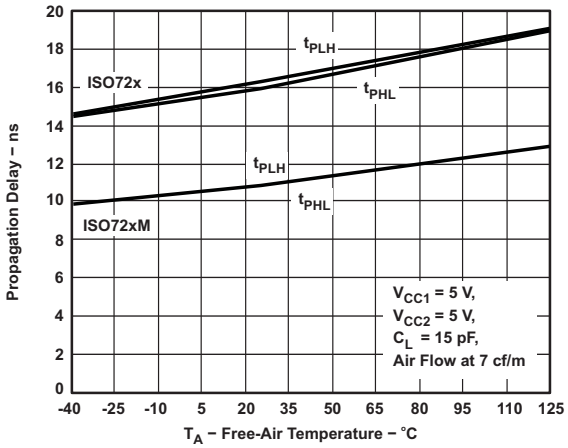


Figure 11.

ISO72x INPUT THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

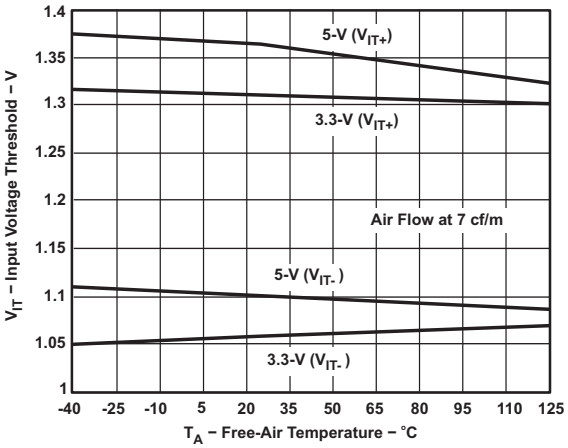


Figure 12.

ISO72xM INPUT THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

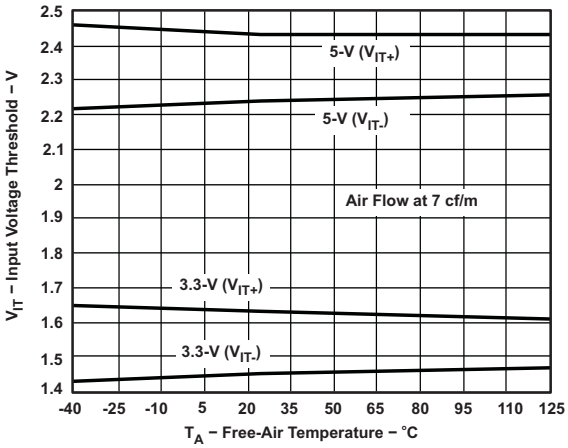


Figure 13.

TYPICAL CHARACTERISTICS (continued)

V_{CC1} FAILSAFE THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

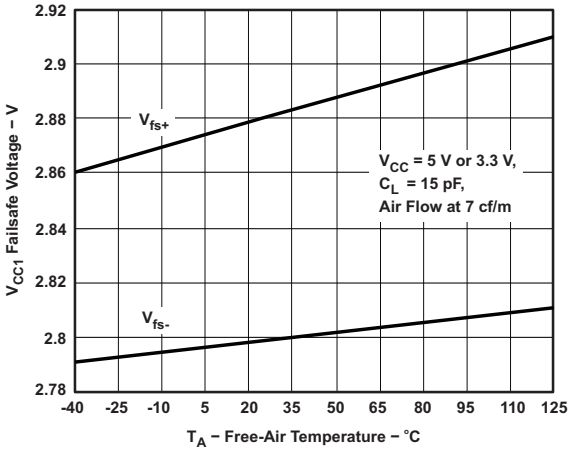


Figure 14.

HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

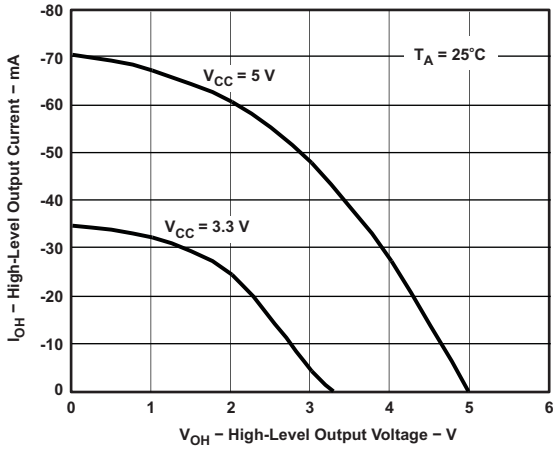


Figure 15.

LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

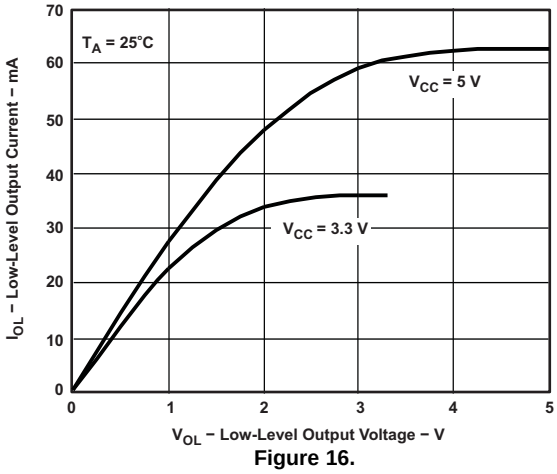


Figure 16.

APPLICATION INFORMATION

MANUFACTURER CROSS-REFERENCE DATA

The ISO72xx isolators have the same functional pinout as those of most other vendors, and they are often pin-for-pin drop-in replacements. The notable differences in the products are propagation delay, signaling rate, power consumption, and transient protection rating. Table 6 is used as a guide for replacing other isolators with the ISO72x family of single channel isolators.

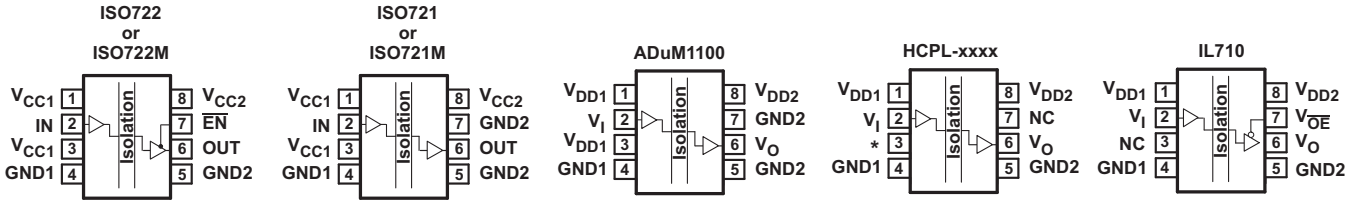


Figure 17. Pin Cross Reference

Table 6. CROSS REFERENCE

ISOLATOR	PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN 6	PIN 7		PIN 8
							ISO721 OR ISO721M	ISO722 OR ISO722M	
ISO721(1) (2)	V_{CC1}	IN	V_{CC1}	GND1	GND2	OUT	GND2	$\overline{EN}$	V_{CC2}
ADuM1100(1) (2)	V_{DD1}	V_I	V_{DD1}	GND1	GND2	V_O	GND2		V_{DD2}
HCPL-xxxx	V_{DD1}	V_I	*Leave Open(3)	GND1	GND2	V_O	NC(4)		V_{DD2}
IL710	V_{DD1}	V_I	NC(5)	GND1	GND2	V_O	$V_{\overline{OE}}$		V_{DD2}

(1) Pin 1 should be used as V_{CC1}. Pin 3 may also be used as V_{CC1} or left open, as long as pin 1 is connected to V_{CC1}.
(2) Pin 5 should be used as GND2. Pin 7 may also be used as GND2 or left open, as long as pin 5 is connected to GND2.
(3) Pin 3 of the HCPL devices must be left open. This is not a problem when substituting an ISO72xx device, because the extra V_{CC1} on pin 3 may be left an open circuit as well.
(4) An HCPL device pin 7 must be left floating (open) or grounded when an ISO722 or ISO722M device is to be used as a drop-in replacement. If pin 7 of the ISO722 or ISO722M device is placed in a high logic state, the output of the device is disabled.
(5) Pin 3 of the IL710 must not be tied to ground on the circuit board because this shorts the ISO72xx's V_{CC1} to ground. The IL710 pin 3 may only be tied to V_{CC} or left open to drop in an ISO72xx.

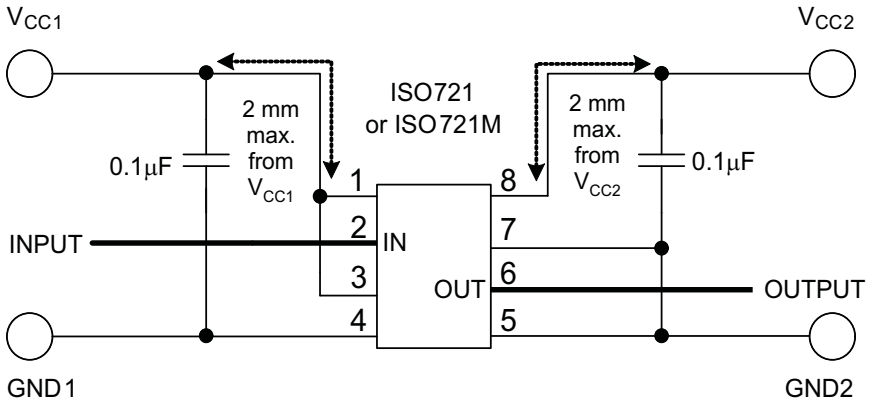
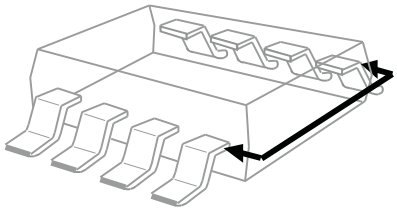


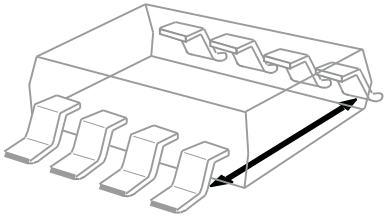
Figure 18. Basic Application Circuit

ISOLATION GLOSSARY

Creepage Distance — The shortest path between two conductive input to output leads measured along the surface of the insulation. The shortest distance path is found around the end of the package body.



Clearance — The shortest distance between two conductive input to output leads measured through air (line of sight).



Input-to Output Barrier Capacitance — The total capacitance between all input terminals connected together, and all output terminals connected together.

Input-to Output Barrier Resistance — The total resistance between all input terminals connected together, and all output terminals connected together.

Primary Circuit — An internal circuit directly connected to an external supply main or other equivalent source which supplies the primary circuit electric power.

Secondary Circuit — A circuit with no direct connection to primary power, which derives its power from a separate isolated source.

Comparative Tracking Index (CTI) — CTI is an index used for electrical insulating materials that is defined as the numerical value of the voltage which causes failure by tracking during standard testing. Tracking is the process that produces a partially conducting path of localized deterioration on or through the surface of an insulating material as a result of the action of electric discharges on or close to an insulation surface -- the higher the CTI value of the insulating material, the smaller the minimum creepage distance.

Generally, insulation breakdown occurs either through the material, over its surface, or both. Surface failure may arise from flashover or from the progressive degradation of the insulation surface by small localized sparks. Such sparks are the result of the breaking of a surface film of conducting contaminant on the insulation. The resulting break in the leakage current produces an overvoltage at the site of the discontinuity, and an electric spark is generated. These sparks often cause carbonization on insulation material and lead to a carbon track between points of different potential. This process is known as *tracking*.

Insulation:

Operational insulation — Insulation needed for the correct operation of the equipment.

Basic insulation — Insulation to provide basic protection against electric shock.

Supplementary insulation — Independent insulation applied in addition to basic insulation in order to ensure protection against electric shock in the event of a failure of the basic insulation.

Double insulation — Insulation comprising both basic and supplementary insulation.

Reinforced insulation — A single insulation system which provides a degree of protection against electric shock equivalent to double insulation.

Pollution Degree:

Pollution Degree 1 — No pollution, or only dry, nonconductive pollution occurs. The pollution has no influence.

Pollution Degree 2 — Normally, only nonconductive pollution occurs. However, a temporary conductivity caused by condensation must be expected.

Pollution Degree 3 — Conductive pollution occurs or dry nonconductive pollution occurs which becomes conductive due to condensation which is to be expected.

Pollution Degree 4 – Continuous conductivity occurs due to conductive dust, rain, or other wet conditions.

Installation Category:

Overvoltage Category — This section is directed at insulation co-ordination by identifying the transient overvoltages which may occur, and by assigning four different levels as indicated in IEC 60664.

I: Signal level — Special equipment or parts of equipment.

II: Local level — Portable equipment, etc.

III: Distribution level — Fixed installation

IV: Primary supply level — Overhead lines, cable systems

Each category should be subject to smaller transients than the category above.

REVISION HISTORY

Changes from Revision I (February 2010) to Revision J — **Page**

- Changed V to Vpeak in UNIT column of IEC Insulation Characteristics table 4
- Added row for V_{ISO} to IEC Insulation Characteristics table 4
- Changed note from " 5
- Removed V_{CC2} from 5-V operation, changed 3-V operation to 3.3-V operation, and removed V_{CC1} from 3.3-V operation in note. 6
- Removed V_{CC1} from 5-V operation, changed 3-V operation to 3.3-V operation, and removed V_{CC2} from 3.3-V operation in note. 7
- Removed 5-V operation, changed 3-V operation to 3.3-V operation, and changed " 8
- Added "INSULATION" to the title of "PACKAGE CHARACTERISTICS" table 12
- Added "Descriptions" to header of PACKAGE INSULATION CHARACTERISTICS table 12

Changes from Revision H (June 2009) to Revision I — **Page**

- Changed 50 kV/s to 50 kV/µs 1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
ISO721D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
ISO721DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
ISO721DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
ISO721DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
ISO721DUB	ACTIVE	SOP	DUB	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	Purchase Samples
ISO721DUBR	ACTIVE	SOP	DUB	8	350	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	Request Free Samples
ISO721MD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
ISO721MDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
ISO721MDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
ISO721MDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
ISO722D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
ISO722DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
ISO722DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
ISO722DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
ISO722MD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
ISO722MDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
ISO722MDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
ISO722MDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

OTHER QUALIFIED VERSIONS OF ISO721, ISO721M :

- Automotive: ISO721-Q1
- Enhanced Product: ISO721M-EP

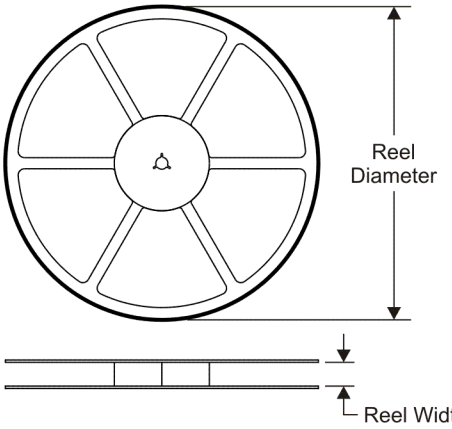
NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

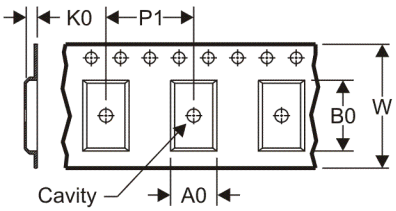
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

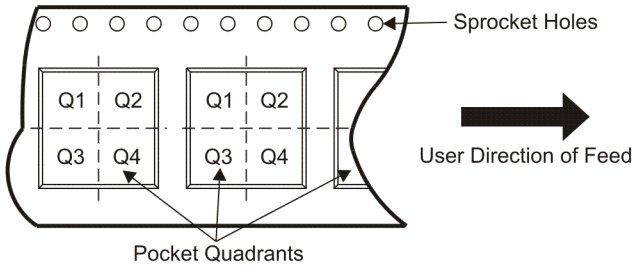


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

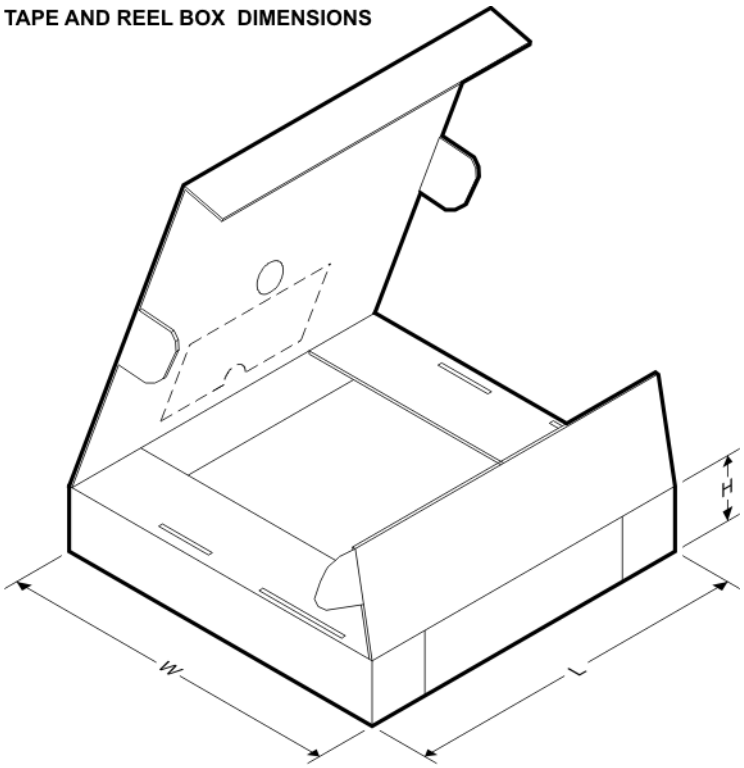
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO721DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO721DUBR	SOP	DUB	8	350	330.0	24.4	10.9	10.01	5.85	16.0	24.0	Q1
ISO721MDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO722DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO722MDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

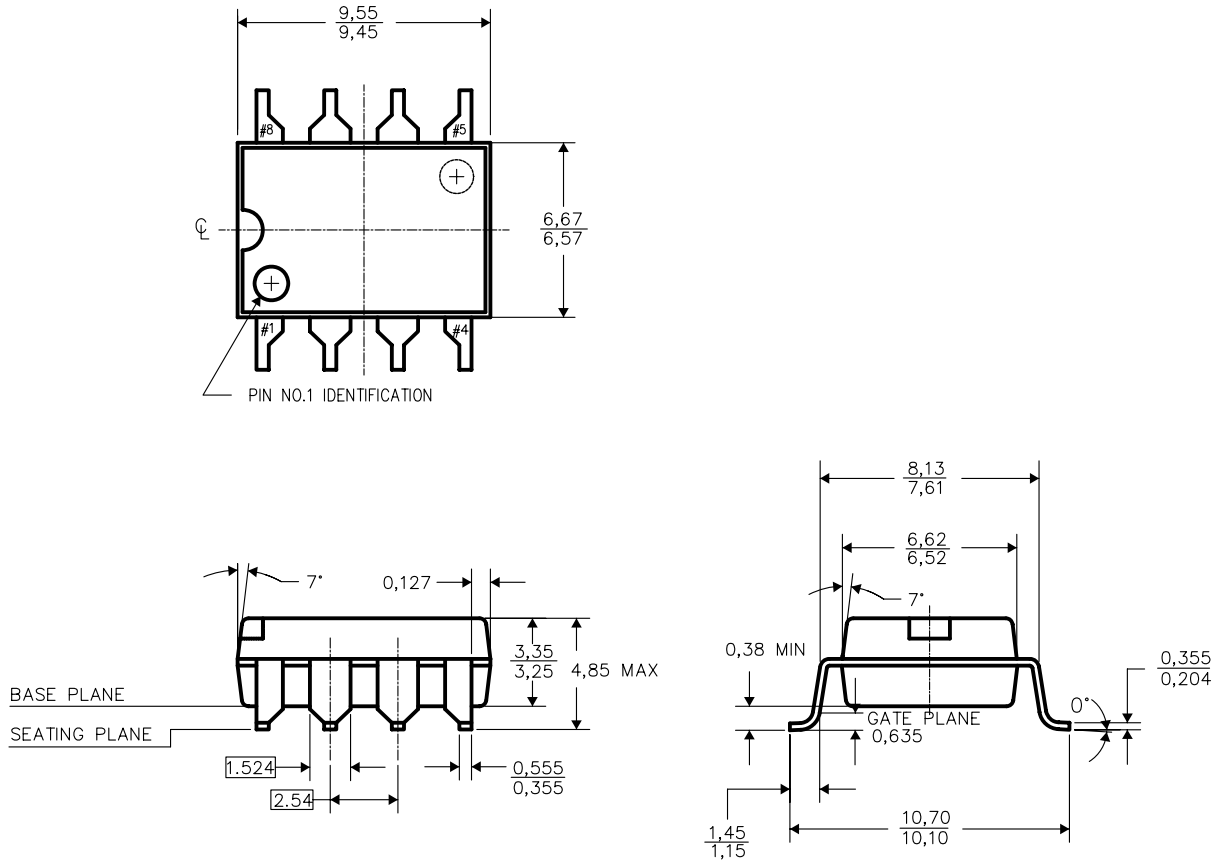
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

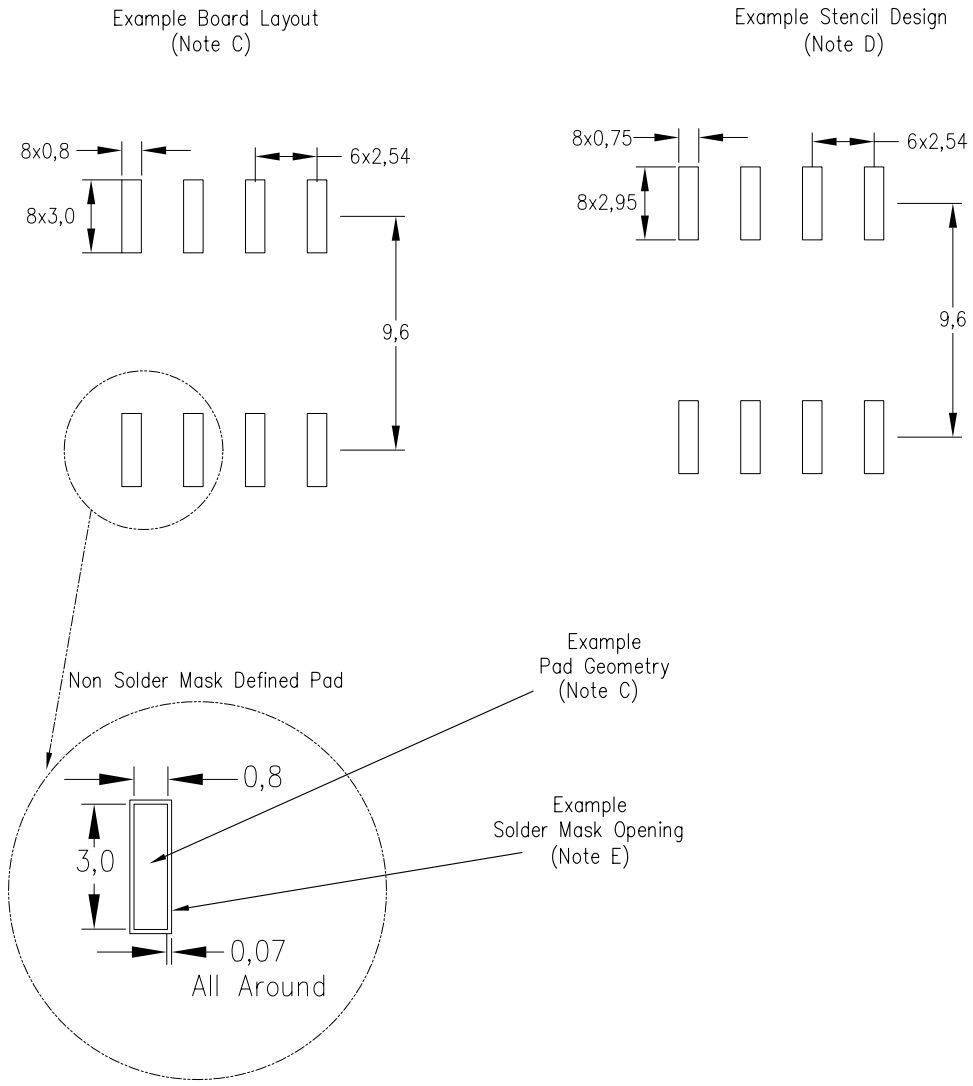
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO721DR	SOIC	D	8	2500	358.0	335.0	35.0
ISO721DUBR	SOP	DUB	8	350	358.0	335.0	35.0
ISO721MDR	SOIC	D	8	2500	358.0	335.0	35.0
ISO722DR	SOIC	D	8	2500	358.0	335.0	35.0
ISO722MDR	SOIC	D	8	2500	358.0	335.0	35.0

DUB (R–PDSO–G8) PLASTIC SMALL–OUTLINE



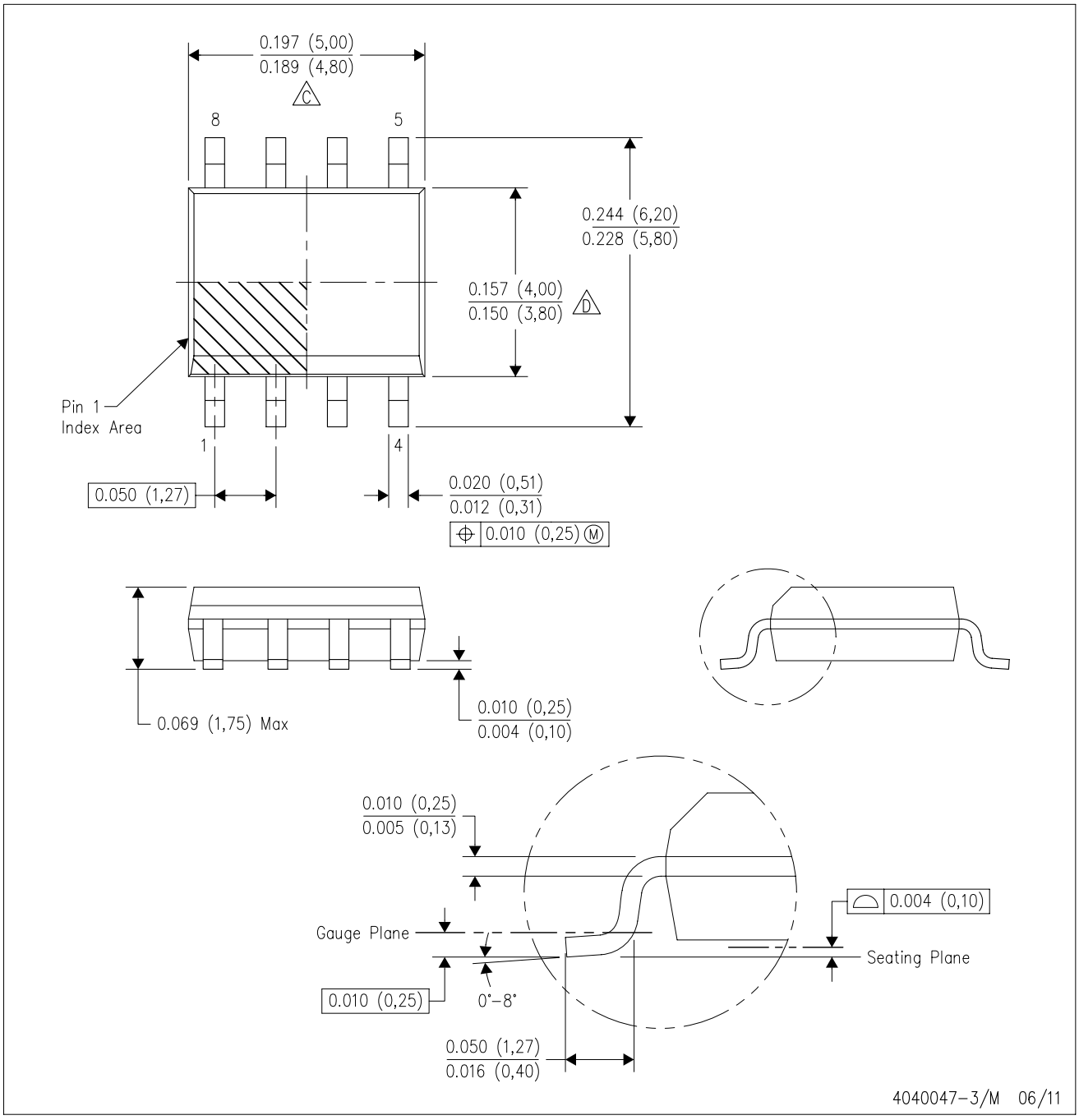
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ANSI Y14.5 M–1982.
B. This drawing is subject to change without notice.
C. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.254mm.

DUB (R–PDSO–G8) PLASTIC SMALL OUTLINE



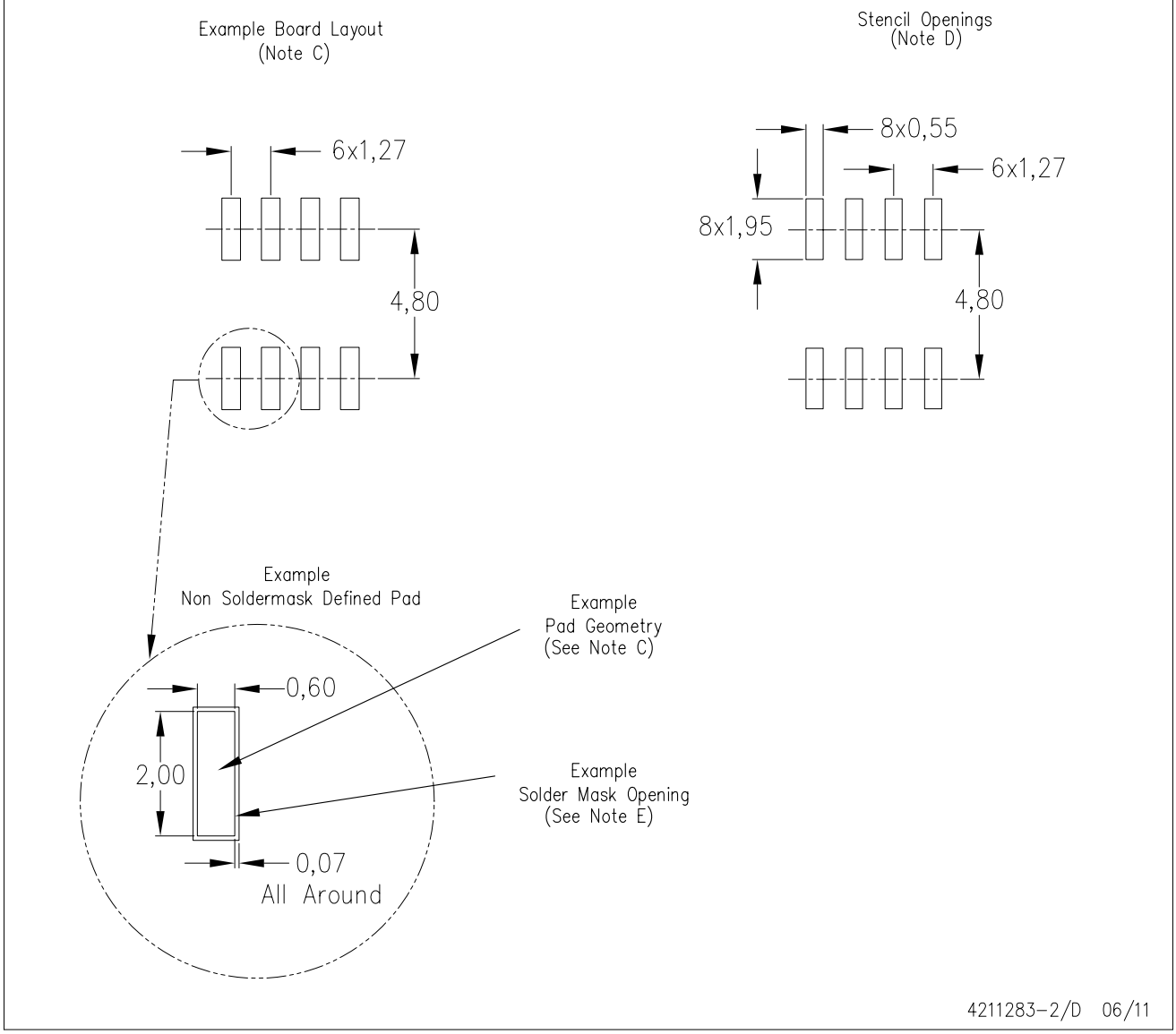
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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