REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device types 03 and 04. – rrp	99-11-15	R. Monnin
B	Changes made to V_{RLOAD}, ΔI_{ADJ}(line), V_{RLINE}, V_{OUT}, and $\Delta V_{IN}/\Delta V_{OUT}$ tests in table I. – rrp	00-07-17	R. Monnin
C	Add case outline Z. Make change to 1.2.4, 1.3, and figure 2. - ro	00-10-03	R. Monnin
D	Add footnote to 1.5. Change made to 3.2.3. Remove radiation test circuits. -rrp	00-12-22	R. Monnin
E	Drawing updated to reflect current requirements. – gt	02-05-10	R. Monnin
F	Make change to the radiation hardened V_{OUT} test maximum limits for device types 03 and 04 as specified under table I. - ro	02-08-01	R. Monnin
G	Make change to V_{OUT} (Recovery) test as specified in table I for device types 03 and 04. - ro	02-09-05	R. Monnin
H	Add device type 05 tested at Low Dose Rate. Make changes to 1.2.2, 1.3, 1.4, 1.5, table I, figure 2, table IIB, and 4.4.4.1. Drawing updated to reflect current requirements. -rrp	06-07-18	R. Monnin
J	Add appendix A, die requirements. Change 1.3, ELDRS dose rate from 12 mrad(Si)/s to 10 mrad(Si)/s. - drw	08-09-25	Robert M. Heber
K	Add device types 06 and 07. - drw	11-11-14	Charles F. Saffle
L	Add device type 08. - ro	12-06-27	Charles F. Saffle
M	Make correction to the Output voltage recovery after output short circuit current test by adding the post irradiation limit for device type 08 as specified under Table I. Delete references to device class M requirements. - ro	15-03-12	Charles F. Saffle

REV																				
SHEET																				
REV	M	M	M	M	M	M	M	M	M	M										
SHEET	15	16	17	18	19	20	21	22	23	24										
REV STATUS				REV			M	M	M	M	M	M	M	M	M	M	M	M	M	M
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Rajesh Pithadia

APPROVED BY
Raymond Monnin

DRAWING APPROVAL DATE
99-05-13

REVISION LEVEL
M

MICROCIRCUIT, LINEAR, RADIATION HARDENED, ADJUSTABLE, VOLTAGE REGULATOR, MONOLITHIC SILICON

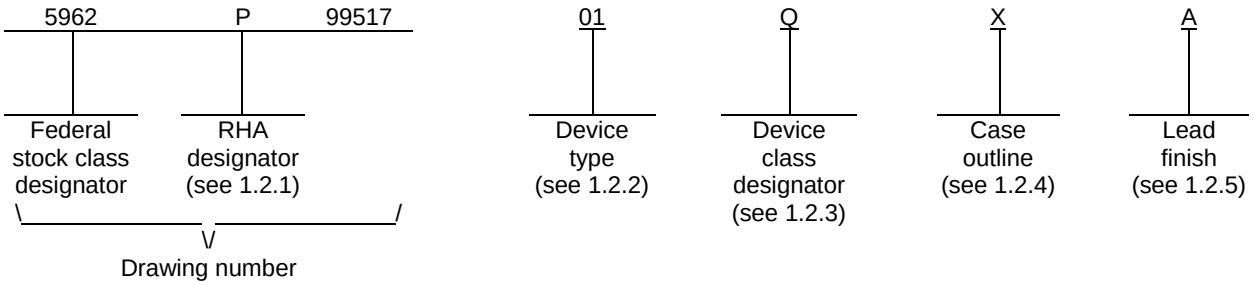
SIZE	CAGE CODE	
A	**67268**	**5962-99517**

SHEET 1 OF 24

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	LM137H, WG	Adjustable, negative, voltage regulator
02	LM137K	Adjustable, negative, voltage regulator
03 1/	LM117H, WG	Adjustable, positive, voltage regulator
04	LM117K	Adjustable, positive, voltage regulator
05 1/	LM117H, WG	Adjustable, positive, voltage regulator
06 1/	LM117GW	Adjustable, positive, voltage regulator
07 1/	LM117GW	Adjustable, positive, voltage regulator
08	LM137H	Adjustable, negative, voltage regulator

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	3	TO-39 can
Y	MBFM1-P2	2	Flange mount
Z 1/	GDFP1-G16	16	Flat pack with gullwing leads

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1/ For case outline Z, package material for device types 03 and 05 are aluminum nitride and package material for device types 06 and 07 are aluminum oxide.

1.3 Absolute maximum ratings. 2/

Minimum input voltage (V_{IN}):	
Device types 01, 02, and 08	-41.25 V
Maximum input voltage (V_{IN}):	
Device types 03, 04, 05, 06 and 07	41.25 V
Input-output voltage differential	40 V
Power dissipation:	Internally limited 3/
Maximum power dissipation at T_A = 25°C:	
Device types 01 and 08	2.5 W
Device type 02	28 W
Device types 03, 05, 06 and 07	2 W
Device type 04	20 W
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	300°C
Maximum junction temperature (T_J)	150°C 3/
Operating junction temperature	-55°C to +150°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case X at 1.0 W (device types 01 and 08)	15°C/W
Case Y (device type 02)	4°C/W
Case X (device types 03 and 05)	21°C/W
Case Y (device type 04)	1.9°C/W
Case Z (device type 01)	2.7°C/W
Case Z (device types 03 and 05)	3.4°C/W 1/
Case Z (device types 06 and 07)	7°C/W 1/
Thermal resistance, junction-to-ambient (θ_{JA}):	
Case X (device types 01 and 08)	140°C/W still air at 0.5 W 64°C/W 500 LFPM air flow at 0.5 W
Case Y (device type 02)	40°C/W still air 14°C/W 500 LFPM air flow
Case X (device types 03 and 05)	186°C/W still air 64°C/W 500 LFPM air flow
Case Y (device type 04)	39°C/W still air 14°C/W 500 LFPM air flow
Case Z (device type 01)	108°C/W still air at 0.5 W 65°C/W 500 LFPM air flow at 0.5 W
Case Z (device types 03 and 05)	115°C/W still air at 0.5 W 1/ 66°C/W 500 LFPM air flow at 0.5 W 1/
Case Z (device types 06 and 07)	130°C/W still air 1/ 80°C/W 500 LFPM air flow 1/

1.4 Recommended operating conditions.

Input voltage range:	
Device types 01 02, and 08	-4.25 V to -41.25 V
Device types 03, 04, 05, 06 and 07	4.25 V to 41.25 V
Ambient operating temperature range (T_A)	-55°C to +125°C

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3/ The maximum power dissipation must be derated at elevated temperatures and is dictated by T_J, θ_{JA}, and T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the absolute maximum ratings, whichever is lower.

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s):
Device classes Q and V (device types 01, 02, and 08) ..... 30 krads(Si) 4/
Device classes Q and V (device types 03, 04 and 06) ..... 100 krads(Si) 4/
Maximum total dose available (dose rate = 10 mrads(Si)/s):
Device classes Q and V (device types 05 and 07) ..... 100 krads(Si) 5/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

4/ For device types 01, 02, 03, 04, 06, and 08, these parts may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883, method 1019, condition A.

5/ For device types 05 and 07, these parts have been tested lot acceptance testing at low dose rate (10 mrads(Si)/s) and do not demonstrate low dose rate sensitivity. Radiation end point limits for the noted parameters are guaranteed for the conditions specified in MIL-STD-883, test method 1019, condition D. Lot acceptance testing at low dose rate will continue to be performed on each wafer or wafer lot until characterization testing has been performed in accordance with Method 1019 of MIL-STD-883.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output voltage	V_{OUT}	V_{IN} = -4.25 V, I_L = 5 mA	1	01, 02, 08	-1.275	-1.225	V
			2, 3		-1.3	-1.2	
		V_{IN} = -4.25 V, I_L = 500 mA	1	01, 08	-1.275	-1.225	
			2, 3		-1.3	-1.2	
		V_{IN} = -4.25 V, I_L = 1.5 A	1	02	-1.275	-1.225	
			2, 3		-1.3	-1.2	
		V_{IN} = -41.25 V, I_L = 5 mA	1	01, 02,	-1.275	-1.225	
			2, 3	08	-1.3	-1.2	
		M, D, P	1	08	-1.30	-1.225	
		V_{IN} = -41.25 V, I_L = 50 mA	1	01, 08	-1.275	-1.225	
			2, 3		-1.3	-1.2	
		M, D, P	1	08	-1.30	-1.225	
		V_{IN} = -41.25 V, I_L = 200 mA	1	02	-1.275	-1.225	
			2, 3		-1.3	-1.2	
Line regulation	V_{RLINE}	V_{IN} = -41.25 V to -4.25 V, I_L = 5 mA	1	01, 02, 08	-9	9	mV
			2, 3		-23	23	
		M, D, P	1	08	-9.0	+50	
Load regulation	V_{RLOAD}	V_{IN} = -6.25 V, I_L = 5 mA to 500 mA	1	01, 08	-12	12	mV
			2, 3		-24	24	
		V_{IN} = -41.25 V, I_L = 5 mA to 50 mA	1		-6	6	
			2, 3		-12	12	
		V_{IN} = -6.25 V, I_L = 5 mA to 200 mA	1		-6	6	
			2, 3		-12	12	
		V_{IN} = -6.25 V, I_L = 5 mA to 1.5 A	1	02	-6	6	
			2, 3		-12	12	
		M, D, P	1		-7.5	7.5	
		V_{IN} = -41.25 V, I_L = 5 mA to 200 mA	1		-6	6	
			2, 3		-12	12	
Thermal regulation	V_{rth}	V_{IN} = -14.6 V, I_L = 500 mA	1	01, 08	-5	5	mV
		V_{IN} = -14.6 V, I_L = 1.5 A	1	02	-5	5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Adjust pin current	I_{adj}	V_{IN} = -4.25 V, I_L = 5 mA	1, 2, 3	01, 02,	25	100	µA
		V_{IN} = -41.25 V, I_L = 5 mA		08	25	100	
		M, D, P	1	08	25	140	
Adjust pin current change vs. line voltage	ΔI_{adj} (line)	V_{IN} = -41.25 V to –4.25 V, I_L = 5 mA	1, 2, 3	01, 02, 08	-5	+5	µA
		M, D, P	1	01	-20	+20	
		M, D, P		08	-70	+20	
Adjust pin current change vs. load current	ΔI_{adj} (load)	V_{IN} = -6.25 V, I_L = 5 mA to 500 mA	1, 2, 3	01, 08	-5	5	µA
		V_{IN} = -6.25 V, I_L = 5 mA to 1.5 A		02	-5	5	
Output short circuit current	I_{OS}	V_{IN} = -4.25 V	1, 2, 3	01, 08	0.5	1.8	A
		V_{IN} = -40 V			0.05	0.5	
		V_{IN} = -4.25 V		02	1.5	3.5	
		V_{IN} = -40 V			0.2	1	
Output voltage recovery after output short circuit current	V_{OUT} (Recovery)	V_{IN} = -4.25 V	1	01, 02,	-1.275	-1.225	V
			2, 3	08	-1.3	-1.2	
		V_{IN} = -40 V	1	01, 02,	-1.275	-1.225	
			2, 3	08	-1.3	-1.2	
		M, D, P	1	08	-1.30	-1.225	
Minimum load current	I_q	V_{IN} = -4.25 V	1, 2, 3	01, 02,	0.2	3	mA
		V_{IN} = -14.25 V		08	0.2	3	
		V_{IN} = -41.25 V			1	5	
Voltage start-up	V_{start}	V_{IN} = -4.25 V, I_L = 500 mA	1	01, 08	-1.275	-1.225	V
			2, 3		-1.3	-1.2	
		V_{IN} = -4.25 V, I_L = 1.5 A	1	02	-1.275	-1.225	
			2, 3		-1.3	-1.2	
Output voltage 3/	V_{OUT}	V_{IN} = -6.25 V, I_L = 5 mA	2	01, 02, 08	-1.3	-1.2	V
Ripple rejection	ΔV_{IN} / ΔV_{OUT}	V_{IN} = -6.25 V, I_L = 125 mA, ei = 1 Vrms at 2400 Hz	4	01, 08	48		dB
		V_{IN} = -6.25 V, I_L = 500 mA, ei = 1 Vrms at 2400 Hz		02	50		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output noise voltage	V_{no}	V_{IN} = -6.25 V, I_L = 50 mA	7	01, 08		120	µVrms
		V_{IN} = -6.25 V, I_L = 100 mA		02		120	
Line transient response	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = -6.25 V, V_{PULSE} = -1 V, I_L = 50 mA	7	01, 08		80	mV/V
		V_{IN} = -6.25 V, V_{PULSE} = -1 V, I_L = 100 mA		02		80	
Load transient response	$\Delta V_{OUT}/\Delta I_L$	V_{IN} = -6.25 V, I_L = 50 mA, ΔI_L = 200 mA	7	01, 08		60 4/	mV
		V_{IN} = -6.25 V, I_L = 100 mA, ΔI_L = 400 mA		02		60 5/	
Output voltage	V_{OUT}	V_{IN} = 4.25 V, I_L = -5 mA	1,2,3	03, 04, 05, 06,	1.2	1.3	V
		M,D,P,L,R	1	07	1.2	1.350	
		V_{IN} = 4.25 V, I_L = -500 mA	1,2,3	03, 05,	1.2	1.3	
		M,D,P,L,R	1	06, 07	1.2	1.350	
		V_{IN} = 4.25 V, I_L = -1.5 A	1,2,3	04	1.2	1.3	
		M,D,P,L,R	1		1.2	1.350	
		V_{IN} = 41.25 V, I_L = -5 mA	1,2,3	03, 04,	1.2	1.3	
		M,D,P,L,R	1	05, 06, 07	1.2	1.350	
		V_{IN} = 41.25 V, I_L = -50 mA	1,2,3	03, 05,	1.2	1.3	
		M,D,P,L,R	1	06, 07	1.2	1.350	
		V_{IN} = 41.25 V, I_L = -200 mA	1,2,3	04	1.2	1.3	
		M,D,P,L,R	1		1.2	1.350	
Line regulation	V_{RLINE}	V_{IN} = 4.25 V to 41.25 V, I_L = -5 mA	1	03, 04, 05, 06,	-9	9	mV
			2, 3		-23	23	
		M,D,P,L,R	1	07	-25	25	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Load regulation	V_{RLOAD}	V_{IN} = 6.25 V, I_L = -500 mA to -5 mA	1,2,3	03, 05, 06, 07	-12	12	mV
		V_{IN} = 41.25 V, I_L = -50 mA to -5 mA	1,2,3		-12	12	
		V_{IN} = 6.25 V, I_L = -1.5 A to -5 mA	1	04	-3.5	3.5	
			2, 3		-12	12	
		M,D,P,L,R	1		-7.0	7.0	
		V_{IN} = 41.25 V, I_L = -200 mA to -5 mA	1		-3.5	3.5	
			2, 3		-12	12	
		M,D,P,L,R	1		-7.0	7.0	
Thermal regulation	V_{rth}	V_{IN} = 14.6 V, I_L = -500 mA	1	03, 05, 06, 07	-12	12	mV
		V_{IN} = 14.6 V, I_L = -1.5 A	1	04	-12	12	
Adjust pin current	I_{adj}	V_{IN} = 4.25 V, I_L = -5 mA	1, 2, 3	03, 04, 05, 06, 07	-100	-15	µA
		V_{IN} = 41.25 V, I_L = -5 mA			-100	-15	
Adjust pin current change vs. line voltage	ΔI_{adj} (line)	V_{IN} = 4.25 V to 41.25 V, I_L = -5 mA	1, 2, 3	03, 04, 05, 06, 07	-5	5	µA
Adjust pin current change vs. load current	ΔIadj (load)	V_{IN} = 6.25 V, I_L = -500 mA to -5 mA	1, 2, 3	03, 05, 06, 07	-5	5	µA
		V_{IN} = 6.25 V, I_L = -1.5 A to --5 mA		04	-5	5	
Output short circuit current	I_{OS}	V_{IN} = 4.25 V	1, 2, 3	03, 05, 06, 07	-1.8	-0.5	A
		V_{IN} = 40 V			-0.5	-0.05	
		V_{IN} = 4.25 V		04	-3.5	-1.5	
		V_{IN} = 40 V			-1	-0.18	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output voltage recovery after output short circuit current	V_{OUT} (Recovery)	V_{IN} = 4.25 V, R_L = 2.5 Ω, C_L = 20 μF	1, 2, 3	03, 05, 06, 07	1.2	1.3	V
		M,D,P,L,R	1		1.2	1.350	
		V_{IN} = 4.25 V, R_L = 0.833Ω, C_L = 20 μF	1, 2, 3	04	1.2	1.3	
		M,D,P,L,R	1		1.2	1.350	
		V_{IN} = 40 V, R_L = 250Ω	1, 2, 3	03, 04,	1.2	1.3	
		M,D,P,L,R	1	05, 06, 07	1.2	1.350	
Minimum load current	I_q	V_{IN} = 4.25 V, forced V_{OUT} = 1.4 V	1, 2, 3	03, 05, 06, 07	-3	-0.5	mA
		V_{IN} = 14.25 V, forced V_{OUT} = 1.4 V			-3	-0.5	
		V_{IN} = 41.25 V, forced V_{OUT} = 1.4 V			-5	-1	
		V_{IN} = 4.25 V, forced V_{OUT} = 1.4 V		04	-3	-0.2	mA
		V_{IN} = 14.25 V, forced V_{OUT} = 1.4 V			-3	-0.2	
		V_{IN} = 41.25 V, forced V_{OUT} = 1.4 V			-5	-0.2	
Voltage start-up	V_{start}	V_{IN} = 4.25 V, I_L = -500 mA, R_L = 2.5 Ω, C_L = 20 μF	1, 2, 3	03, 05, 06, 07	1.2	1.3	V
		V_{IN} = 4.25 V, I_L = -1.5 A, R_L = 0.833 Ω, C_L = 20 μF	1, 2, 3	04	1.2	1.3	
Output voltage 3/	V_{OUT}	V_{IN} = 6.25 V, I_L = -5 mA	2	03, 04, 05, 06, 07	1.2	1.3	V
Ripple rejection	ΔV_{IN} / ΔV_{OUT}	V_{IN} = 6.25 V, I_L = -125 mA, ei = 1 Vrms at 2400 Hz	4	03, 05, 06, 07	65		dB
		M,D,P,L,R			60		
		V_{IN} = 6.25 V, I_L = -500 mA, ei = 1 Vrms at 2400 Hz		04	65		
		M,D,P,L,R			60		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output noise voltage	V_{no}	V_{IN} = 6.25 V, I_L = -50 mA	7	03, 05, 06, 07		120	µVrms
		V_{IN} = 6.25 V, I_L = -100 mA		04		120	
Line transient response	ΔV_{OUT} / ΔV_{IN}	V_{IN} = 6.25 V, ΔV_{IN} = 3 V, I_L = -10 mA	7	03, 05, 06, 07		6	mV/V
				04		18 6/	mV
Load transient response	ΔV_{OUT} / ΔI_L	V_{IN} = 6.25 V, ΔI_L = -200 mA, I_L = -50 mA	7	03, 05, 06, 07		0.6	mV/mA
		V_{IN} = 6.25 V, ΔI_L = -400 mA, I_L = -100 mA		04		120 7/	mV

1/ Device types 01, 02, and 08 have been characterized through all levels M, D, P of irradiation. However, these devices are only tested at the "P" level. Device types 03, 04, 05, 06 and 07 have been characterized through all levels M, D, P, L, R of irradiation. However, these devices are only tested at the "R" level. Pre and Post irradiation values are identical unless otherwise specified in table I.

2/ For device types 01, 02, 03, 04, 06, and 08, these parts may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883, method 1019, condition A. For device types 05 and 07, these parts have been tested and do not demonstrate low dose rate sensitivity. Radiation end point limits for the noted parameters are guaranteed for the conditions specified in MIL-STD-883, test method 1019, condition D.

3/ Tested at T_A = +125°C, correlated to T_A = +150°C.

4/ Limit is equivalent to a limit of 0.3 mV/mA.

5/ Limit is equivalent to a limit of 0.15 mV/mA.

6/ Limit of 6 mV/V is equivalent to 18 mV.

7/ Limit of 0.3 mV/V is equivalent to 120 mV.

Case X

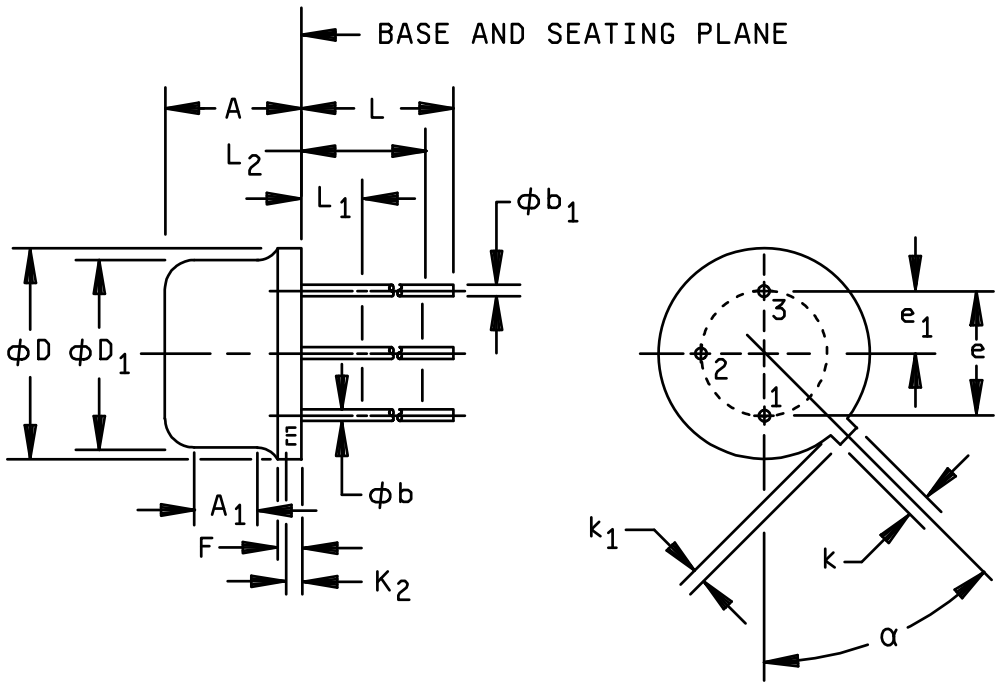


FIGURE 1. Case outline.

Case X

Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	.165	.195	4.19	4.95	
A_1	.100	---	2.54	---	7
ϕb	.016	.019	0.41	0.48	3
ϕb_1	.016	.021	0.41	0.53	3
ϕD	.335	.370	8.51	9.40	
ϕD_1	.305	.335	7.75	8.51	
e	.200 BSC		5.08 BSC		5
e_1	.100 BSC		2.54 BSC		5
F	---	.050	---	1.27	
k	.028	.034	0.71	0.86	
k_1	.029	.045	0.74	1.14	4
k_2	.009	.041	0.23	1.04	
L	.500	----	12.70	----	
L_1	---	.050	---	1.27	
L_2	.250	---	6.35	---	
α	45° T.P.		45° T.P.		5

NOTES:

1. The US government preferred system of measurement is the metric SI system. However, this item was originally designed using inch-pound units of measurement. In the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
2. ϕb applies between L_1 and beyond .500 inch (12.70 mm) from the seating plane (two leads). Diameter is uncontrolled in L_1 and beyond .500 inch (12.70 mm) from the seating plane.
3. Two leads.
4. Two holes.
5. Two holes located at true position within diameter .010 inch (0.25 mm).
6. Leads having a maximum diameter of .043 inch (1.09 mm) measured in gauging plane .054 inch (1.37 mm) $\pm$ .001 inch (0.03 mm) .000 inch (0.00 mm) below the seating plane shall be located at true position within diameter .014 inch (0.36 mm).
7. The mounting surface of the header shall be flat to convex within .003 inch (0.08 mm) inside a .930 inch (23.62 mm) diameter circle on the center of the header and flat to convex within .006 inch (0.15 mm) overall.

FIGURE 1. Case outline – Continued.

Device types	01, 08	02	03 and 05	04
Case outlines	X	Y 1/	X	Y 2/
Terminal number	Terminal symbol			
1	ADJUSTMENT	ADJUSTMENT	INPUT	ADJUSTMENT
2	OUTPUT	OUTPUT	ADJUSTMENT	INPUT
3	INPUT	---	OUTPUT	---

Device types	01	03, 05, 06 and 07
Case outline	Z 3/	
Terminal number	Terminal symbol 4/	
1	NC	NC
2	NC	NC
3	ADJUSTMENT	ADJUSTMENT
4	INPUT	NC
5	NC	INPUT
6	NC	NC
7	NC	NC
8	NC	NC
9	NC	NC
10	NC	NC
11	OUTPUT SENSE	NC
12	OUTPUT	OUTPUT
13	NC	OUTPUT SENSE
14	NC	NC
15	NC	NC
16	NC	NC

1/ For case outline Y, case is input.
2/ For case outline Y, case is output.
3/ For case Z to function properly, the “OUTPUT” and “OUTPUT SENSE” pins must be connected on the users printed circuit board.
4/ NC = No connection

FIGURE 2. Terminal connections.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. .

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5, 6, 8, 9, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical Parameters (see 4.2)	1	1
Final electrical Parameters (see 4.2)	1, 2, 3, 4 1/	1, 2, 3, 4 1/
Group A test Requirements (see 4.4)	1, 2, 3, 4, 7	1, 2, 3, 4, 7
Group C end-point electrical parameters (see 4.4)	1, 2,3	1, 2, 3 2/
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1	1

1/ PDA applies to subgroup 1.
2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be computed with reference to the previous endpoint electrical parameters.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A for device types 01, 02, 03, 04, 06 and 08; condition D for device type 05 and 07 and as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

Table IIB. Group C end-point electrical parameters. T_A = 25°C

Parameter	Device type	Conditions	Delta limit	
			Min	Max
V_{OUT}	01, 02, 08	V_{IN} = -4.25 V, I_L = 5 mA	-0.01 V	0.01 V
	01, 08	V_{IN} = -4.25 V, I_L = 500 mA	-0.01 V	0.01 V
	02	V_{IN} = -4.25 V, I_L = 1.5 A	-0.01 V	0.01 V
	01,02, 08	V_{IN} = -41.25 V, I_L = 5 mA	-0.01 V	0.01 V
	01, 08	V_{IN} = -41.25 V, I_L = 50 mA	-0.01 V	0.01 V
	02	V_{IN} = -41.25 V, I_L = 200 mA	-0.01 V	0.01 V
	03,04,05,06,07	V_{IN} = 4.25 V, I_L = -5 mA	-0.01 V	0.01 V
	03,05,06,07	V_{IN} = 4.25 V, I_L = -500 mA	-0.01 V	0.01 V
	04	V_{IN} = 4.25 V, I_L = -1.5 A	-0.01 V	0.01 V
	03,04,05,06,07	V_{IN} = 41.25 V, I_L = -5 mA	-0.01 V	0.01 V
	03,05,06,07	V_{IN} = 41.25 V, I_L = -50 mA	-0.01 V	0.01 V
	04	V_{IN} = 41.25 V, I_L = -200 mA	-0.01 V	0.01 V
V_{rline}	01,02, 08	V_{IN} = -41.25 V to -4.25 V, I_L = 5 mA	-4 mV	4 mV
	03,04, 05,06,07	V_{IN} = 4.25 V to 41.25 V, I_L = -5 mA	-4 mV	4 mV
I_{adj}	01, 02, 08	V_{IN} = -4.25 V, I_L = 5 mA	-10 μA	10 μA
		V_{IN} = -41.25 V, I_L = 5 mA	-10 μA	10 μA
	03,04, 05,06,07	V_{IN} = 4.25 V, I_L = -5 mA	-10 μA	10 μA
		V_{IN} = 41.25 V, I_L = -5 mA	-10 μA	10 μA
V_{OUT} (Recovery)	03,05,06,07	V_{IN} = 4.25 V, R_L = 2.5Ω, C_L = 20 μF	-0.01 V	0.01 V
		V_{IN} = 40 V, R_L = 250Ω	-0.01 V	0.01 V

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

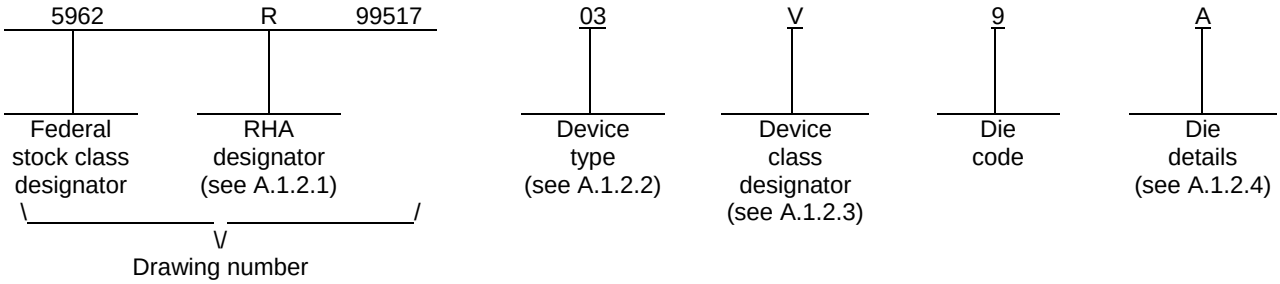
6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-99517

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
03	LM117H	Adjustable, positive, voltage regulator
05	LM117H	Adjustable, positive, voltage regulator

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
03, 05	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
03, 05	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
03, 05	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
03, 05	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.3 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, and 4.4.4.1.1 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

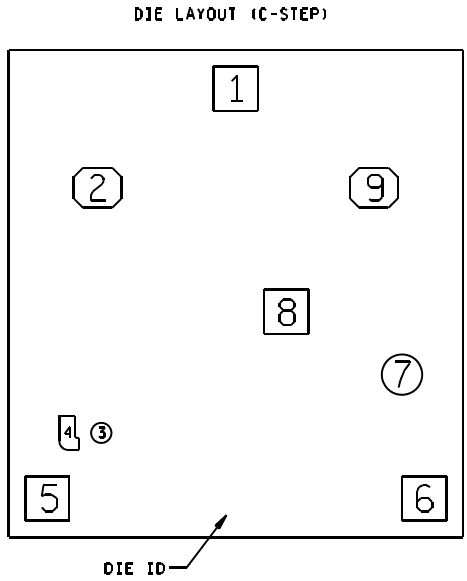
A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0540.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.



Die bonding pad locations and electrical functions

Die physical dimensions.
Die size: 2184.40 µm x 2362.20 µm
86.0 mils x 93.0 mils
Die thickness: 254 µm
Minimum pitch: 1827.53 µm

Interface materials.
Top metallization: AL 0.5% CU
Backside metallization: Gold

Glassivation.
Type: Vapox over metal only (VOM only)
Thickness: 8 kÅ to 12 kÅ

Substrate: Silicon

Assembly related information.
Substrate potential: Output
Special assembly instructions: None

FIGURE A-1. Die bonding pad locations and electrical functions.

Die Bond Pad Coordinate Locations (C-Step) (Referenced to die center, coordinates in µm) NC = No connection						
Signal Name	Pad Number	X/Y Coordinates		Pad Size		
		X	Y	X		Y
Input	1	10	986	213	X	210
Output	2	-655	515	228	X	187
NC	3	-680	-673	91	X	91
NC	4	-826	-689	88	X	170
Output	5	-914	-1000	193	X	198
Adj	6	913	-996	195	X	205
NC	7	800	-391	208	X	208
Input	8	254	-91	193	X	233
Output	9	603	514	226	X	185

FIGURE A-1. Die bonding pad locations and electrical functions - continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 15-03-12

Approved sources of supply for SMD 5962-99517 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9951701VZA	3/	LM137WG-QMLV
5962P9951701QXA	3/	LM137HPQML
5962P9951701QZA	3/	LM137WGPQML
5962P9951701VXA	3/	LM137HPQMLV
5962P9951701VZA	3/	LM137WGPQMLV
5962P9951702QYA	3/	LM137KPQML
5962P9951702VYA	3/	LM137KPQMLV
5962-9951703VZA	3/	LM117WG-QMLV
5962R9951703QXA	3/	LM117HRQML
5962R9951703QZA	3/	LM117WGRQML
5962R9951703V9A	3/	LM117H MDR
5962R9951703VXA	3/	LM117HRQMLV
5962R9951703VZA	3/	LM117WGRQMLV
5962R9951704QYA	3/	LM117KRQML
5962R9951704VYA	3/	LM117KRQMLV
5962R9951705V9A	3/	LM117H MDE
5962R9951705VXA	3/	LM117HRLQMLV
5962R9951705VZA	3/	LM117WGRLQMLV

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9951706QZA	3/	LM117GW-QML
5962R9951706VZA	3/	LM117GWRQMLV
5962R9951707VZA	3/	LM117GWRLQMLV
5962P9951708VXA	27014	LM137H1PQMLV

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
27014	National Semiconductor 2900 Semiconductor Drive P.O. Box 58090 Santa Clara, CA 95052-8090