Intel® LXT971A Single-Port 10/100 Mbps PHY Transceiver

Datasheet

The Intel® LXT971A Single-Port 10/100 Mbps PHY Transceiver (called hereafter the LXT971A Transceiver) directly supports both 100BASE-TX and 10BASE-T applications. It provides a Media Independent Interface (MII) for easy attachment to 10/100 Media Access Controllers (MACs). The LXT971A Transceiver is IEEE compliant, and provides a Low Voltage Positive Emitter Coupled Logic (LVPECL) interface for use with 100BASE-FX fiber networks. (This document also supports the Intel® LXT971 Transceiver.) The LXT971A Transceiver supports full-duplex operation at 10 Mbps and 100 Mbps. Operating conditions for the LXT971A Transceiver can be set using auto-negotiation, parallel detection, or manual control. The LXT971A Transceiver is fabricated with an advanced CMOS process and requires only a single 2.53.3 V power supply.

Applications

- Combination 10BASE-T/100BASE-TX or 100BASE-FX Network Interface Cards (NICs)
- Network printers
- 10/100 Personal Computer Memory Card International Association (PCMCIA) cards
- Cable Modems and Set-Top Boxes

Product Features

- 3.3 V Operation
- Low power consumption (300 mW typical)
- Low-power “Sleep” mode
- 10BASE-T and 100BASE-TX using a single RJ-45 connection
- IEEE 802.3-compliant 10BASE-T or 100BASE-TX ports with integrated filters
- Auto-negotiation and parallel detection
- MII interface with extended register capability
- Robust baseline wander correction
- Carrier Sense Multiple Access / Collision Detection (CSMA/CD) or full-duplex operation
- JTAG boundary scan
- MDIO serial port or hardware pin configurable
- 100BASE-FX fiber-optic capable
- Integrated, programmable LED drivers
  - —64-ball Plastic Ball Grid Array (PBGA) or 64-pin Quad Flat Package (LQFP)
  - —LXT971ABC - Commercial (0° to 70 °C ambient).
  - —LXT971ABE - Extended (-40° to 85 °C ambient).
  - —LXT971ALC - Commercial (0° to 70 °C ambient).
  - —LXT971ALE - Extended (-40° to 85 °C ambient).

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Revision Date: 25-Oct-2005

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Revision History

Intel® LXT971A Transceiver Revision 003 Revision Date: 25-Oct-2005	
Page	**Description**
1	Front page text changed.
51	Changed "PECL Interface" to "LVPECL Interface" in Figure 21 “Protocol Sublayers”.
54	Replaced text under Section 5.7.3.4, “Fiber PMD Sublayer”.
65	Modified first paragraph under Section 6.3, “The Fiber Interface”.
65	Modified text and added a new bullet in first and second set of bullets under Section 6.3, “The Fiber Interface”.
66	Replaced Figure 27 “Recommended LXT971A-to-3.3 V Fiber Transceiver Interface Circuitry”.
67	Replaced Figure 28 “Recommended LXT971A-to-5 V Fiber Transceiver Interface Circuitry”.
107	Added Section 10.1, “Top Label Markings”.
109	Modified Section 11.0, “Product Ordering Information”: added RoHS information to Table 63 “Product Ordering Information” and changed Figure 49 “Order Matrix for Intel® LXT971A Transceiver - Sample”.

Intel® LXT971A Transceiver Revision 002 (Sheet 1 of 2) Revision Date: August 6, 2002	
Page	**Description**
	Globally replaced “pseudo-PECL” with Low-Voltage PECL”, except when identified with 5 V.
1	Front Page: Changed “pseudo-ECL (PECL)” to “Low Voltage PECL (LVPECL). Added “JTAG Boundary Scan” to Product Features on front page.
12	Modified Figure 2 “LXT971A 64-Ball PBGA Assignments” (replaced TEST1 and TEST0 with GND).
13	Modified Figure 3 “LXT971A 64-Pin LQFP Assignments” (replaced TEST1 and TEST0 with GND).
14	Modified Table 1 “LQFP Numeric Pin List” (replaced TEST1 and TEST0 with GND).
16	Added note under Section 2.0, “Signal Descriptions”: “Intel recommends that all inputs and multi-function pins be tied to the inactive states and all outputs be left floating, if unused.”
17	Modified SD/$\overline{\text{TP}}$ description in Table 3 “LXT971A Network Interface Signal Descriptions”. Added Table note 2.
18	Modified Table 4 “LXT971A Miscellaneous Signal Descriptions”.
19	Modified Table 5 “LXT971A Power Supply Signal Descriptions”.
20	Added Table 8 “LXT971A Pin Types and Modes”.
22	Replaced second paragraph under Section 3.2.1.2, “Fiber Interface”.
23	Added Section 3.2.2.1, “Increased MII Drive Strength”.
23	Changed “Far-End Fault” title to ‘100BASE-FX Far-End Fault”. Modified first sentence under this heading.
30	Modified Figure 8 “Hardware Configuration Settings”.
35	Added paragraph after bullets under Section 3.6.7.2, “Test Loopback”.
43	Modified text under Section 3.7.3.4, “Fiber PMD Sublayer”.
47	Modified Table 13 “Supported JTAG Instructions”.

Intel® LXT971A Transceiver Revision 002 (Sheet 2 of 2) Revision Date: August 6, 2002	
Page	**Description**
47	Modified Table 14 “Device ID Register”.
52	Added a new Section 4.3, “The Fiber Interface”.
53	Replaced Figure 25 “Recommended LXT971A-to-3.3 V Fiber Transceiver Interface Circuitry”.
54	Added Figure 26 “Recommended LXT971A-to-5 V Fiber Transceiver Interface Circuitry”.
55	Added Figure 27 “ON Semiconductor Triple PECL-to-LVPECL Logic Translator”.
56	Modified Table 17 “Absolute Maximum Ratings”.
56	Modified Table 18 “Operating Conditions”: Added Typ values to Vcc current.
57	Modified Table 20 “Digital I/O Characteristics - MII Pins”.
58	Modified Table 22 “I/O Characteristics - LED/CFG Pins”.
58	Added Table 23 “I/O Characteristics – SD/TP Pin”.
60	Added Table 28 “LXT971A Thermal Characteristics”.
65	Modified Table 33 “10BASE-T Receive Timing Parameters”
72	Modified Table 42 “Register Bit Map”. (Added Table 26 information).
86	Added Table 57 “Digital Configuration Register (Address 26)”.
87	Modified Table 58 “Transmit Control Register (Address 30)”.
90	Added Section 8.0, “Product Ordering Information”.

Intel® LXT971A Transceiver Revision 001 Revision Date: January 2001	
Page	**Description**
N/A	Clock Requirements: Modified language under Clock Requirements heading.
	Table 21 I/O Characteristics REFCLK: Changed values for Input Clock Duty Cycle under Min from 40 to 35 and under Max from 60 to 65.

1.0 Introduction to This Document

This document includes information on the Intel® LXT971A Single-Port 10/100 Mbps PHY Transceiver (called hereafter the LXT971A Transceiver).

1.1 Document Overview

This document includes the following subjects:

- Chapter 2.0, “Block Diagram for Intel® LXT971A Transceiver”
- Chapter 3.0, “Ball and Pin Assignments for Intel® LXT971A Transceiver”
- Chapter 4.0, “Signal Descriptions for Intel® LXT971A Transceiver”
- Chapter 5.0, “Functional Description”
- Chapter 6.0, “Application Information”
- Chapter 7.0, “Electrical Specifications”
- Chapter 8.0, “Register Definitions - IEEE Base Registers”
- Chapter 9.0, “Register Definitions - Product-Specific Registers”
- Chapter 10.0, “Intel® LXT971A Transceiver Package Specifications”
- Chapter 11.0, “Product Ordering Information”

1.2 Related Documents

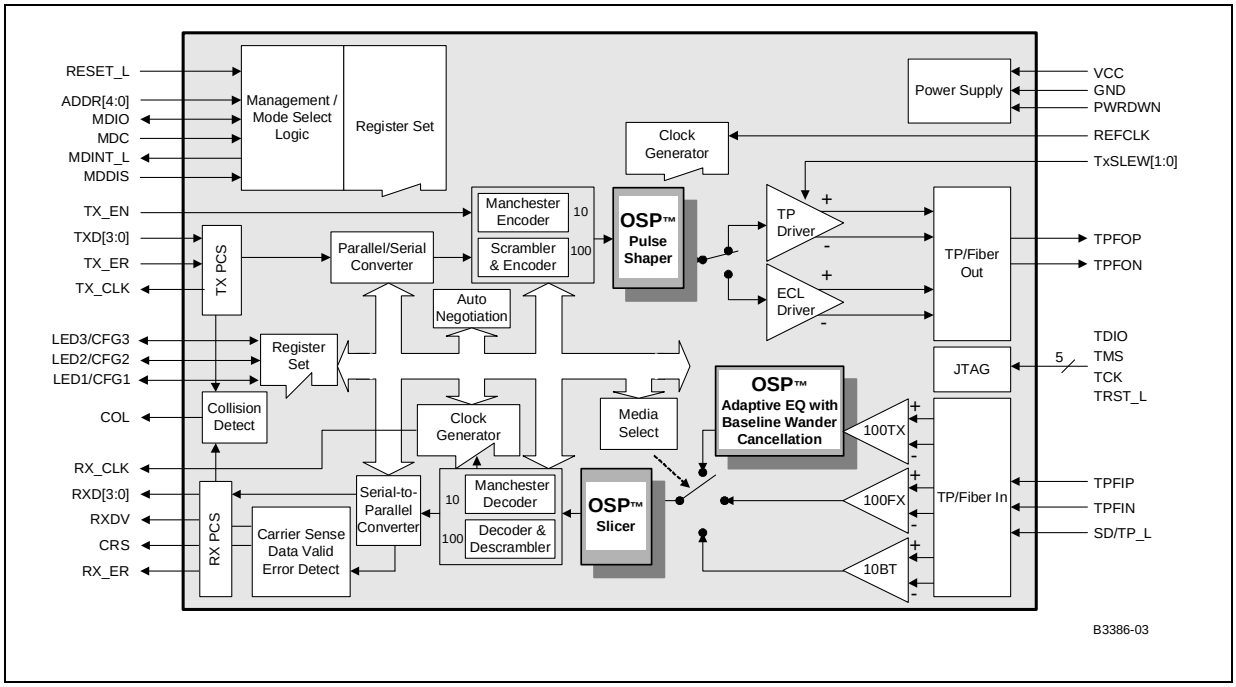
Table 1. Related Documents from Intel

Document Title	Document Number
Fiber Optic Transceivers Connecting a PECL Interface Application Note	249015
Intel® 100BASE-FX Fiber Optic Transceivers - Connecting a PECL/ LVPECL Interface Application Note	250781
Intel® LXT971A , LXT972A , LXT972M Single-Port 10/100 Mbps PHY Transceivers Specification Update	249354
Intel® LXT971A, LXT972A, and LXT972M 3.3V PHY Transceivers Design and Layout Guide - Application Note	249016
Magnetic Manufacturers for Networking Product Applications - Application Note	248991

2.0 Block Diagram for Intel® LXT971A Transceiver

Figure 1 is a block diagram of the LXT971A Transceiver.

Figure 1. Intel® LXT971A Transceiver Block Diagram



3.0 Ball and Pin Assignments for Intel® LXT971A Transceiver

Figure 2 shows the ball assignments for the LXT971A Transceiver 64-ball PBGA package.

Figure 2. Ball Assignments for Intel® LXT971A Transceiver 64-Ball PBGA

	1	2	3	4	5	6	7	8	
A	MDINT_L	CRS	TXD3	TXD0	RX_ER	VCCD	RX_DV	RXD0	A
B	REF CLK/XI	COL	TXD2	TX_EN	TX_ER	RX_ CLK	NC	RXD1	B
C	XO	RESET_L	GND	TXD1	TX_ CLK	GND	NC	RXD2	C
D	Tx SLEW0	Tx SLEW1	MDDIS	GND	VCCIO	RXD3	NC	MDIO	D
E	ADDR0	ADDR1	GND	GND	VCCIO	LED/ CFG1	MDC	PWR DWN	E
F	ADDR3	ADDR2	GND	GND	TDI	TMS	LED/ CFG2	LED/ CFG3	F
G	ADDR4	SD/ TP_L	VCCA	VCCA	TDO	TCK	GND	GND	G
H	RBIAS	TPFOP	TPFON	TPFIP	TPFIN	TRST_ L	SLEEP	PAUSE	H
	1	2	3	4	5	6	7	8	

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Figure 3 shows the pin assignments for the LXT971A Transceiver LQFP package.

Figure 3. Pins for Intel® LXT971A Transceiver 64-Pin LQFP Package

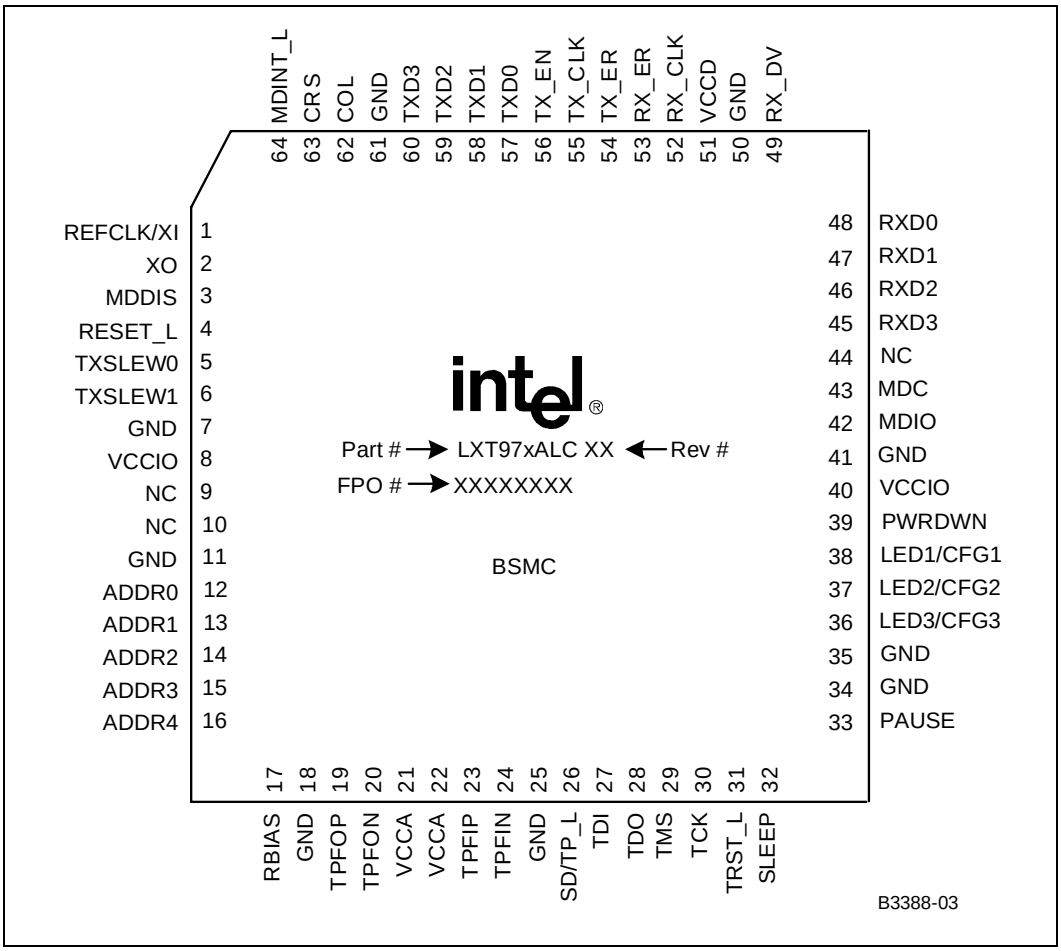


Table 2 lists LXT971A Transceiver LQFP pin numbers, symbols, and pin types.

Table 2. Intel® LXT971A Transceiver LQFP Numeric Pin List (Sheet 1 of 2)

Pin	Symbol	Type
1	REFCLK/XI	I
2	XO	O
3	MDDIS	I
4	RESET_L	I
5	TxSLEW0	I
6	TxSLEW1	I
7	GND	–
8	VCCIO	–
9	NC	–
10	NC	–
11	GND	–
12	ADDR0	I
13	ADDR1	I
14	ADDR2	I
15	ADDR3	I
16	ADDR4	I
17	RBIAS	AI
18	GND	–
19	TPFOP	O
20	TPFON	O
21	VCCA	–
22	VCCA	–
23	TPFIP	I
24	TPFIN	I
25	GND	–
26	SD/TP_L	I
27	TDI	I
28	TDO	O
29	TMS	I
30	TCK	I
31	TRST_L	I
32	SLEEP	I
33	PAUSE	I
34	GND	–
35	GND	–
36	LED/CFG3	I/O

Table 2. Intel® LXT971A Transceiver LQFP Numeric Pin List (Sheet 2 of 2)

Pin	Symbol	Type
37	LED/CFG2	I/O
38	LED/CFG1	I/O
39	PWRDWN	I
40	VCCIO	–
41	GND	–
42	MDIO	I/O
43	MDC	I
44	NC	–
45	RXD3	O
46	RXD2	O
47	RXD1	O
48	RXD0	O
49	RX_DV	O
50	GND	–
51	VCCD	–
52	RX_CLK	O
53	RX_ER	O
54	TX_ER	I
55	TX_CLK	O
56	TX_EN	I
57	TXD0	I
58	TXD1	I
59	TXD2	I
60	TXD3	I
61	GND	–
62	COL	O
63	CRS	O
64	MDINT_L	OD

4.0 Signal Descriptions for Intel® LXT971A Transceiver

Intel recommends the following configurations for unused pins:

- **Unused inputs.** Configure all unused inputs and unused multi-function pins for inactive states.
- **Unused outputs.** Leave all unused outputs floating.
- **No connects.** Do not use pins designated as NC (no connect), and do not terminate them.

Note: For the tables in this section, the following abbreviations listed in Table 3 are used for the "Type" column.

Table 3. Intel® LXT971A Transceiver Signal Types

Abbreviation	Meaning
A	Analog
AI	Analog Input
I	Input
I/O	Input/Output
O	Output
OD	Open Drain

Tables in this section include the following

- Table 4, "Intel® LXT971A Transceiver MII Data Interface Signal Descriptions"
- Table 5, "Intel® LXT971A Transceiver MII Controller Interface Signal Descriptions"
- Table 6, "Intel® LXT971A Transceiver Network Interface Signal Descriptions"
- Table 7, "Intel® LXT971A Transceiver Standard Bus and Interface Signal Descriptions"
- Table 8, "Intel® LXT971A Transceiver Configuration and LED Driver Signal Descriptions"
- Table 9, "Intel® LXT971A Transceiver Power, Ground, No-Connect Signal Descriptions"
- Table 10, "Intel® LXT971A Transceiver JTAG Test Signal Descriptions"
- Table 11, "Intel® LXT971A Transceiver Pin Types and Modes"

Table 4 lists signal descriptions of the LXT971A Transceiver MII data interface pins.

Table 4. Intel® LXT971A Transceiver MII Data Interface Signal Descriptions (Sheet 1 of 2)

PBGA Pin#	LQFP Pin#	Symbol	Type	Signal Description
A3 B3 C4 A4	60 59 58 57	TXD3 TXD2 TXD1 TXD0	I	**Transmit Data.** TXD is a group of parallel data signals that are driven by the MAC. TXD[3:0] transition synchronously with respect to TX_CLK. TXD[0] is the least-significant bit.
B4	56	TX_EN	I	**Transmit Enable.** The MAC asserts this signal when it drives valid data on TXD. This signal must be synchronized to TX_CLK.
C5	55	TX_CLK	O	**Transmit Clock.** TX_CLK is sourced by the PHY in both 10 and 100 Mbps operations. 2.5 MHz for 10 Mbps operation 25 MHz for 100 Mbps operation.
D6 C8 B8 A8	45 46 47 48	RXD3 RXD2 RXD1 RXD0	O	**Receive Data.** RXD is a group of parallel signals that transition synchronously with respect to RX_CLK. RXD[0] is the least-significant bit.
A7	49	RX_DV	O	**Receive Data Valid.** The LXT971A Transceiver asserts this signal when it drives valid data on RXD. This output is synchronous to RX_CLK.
A5	53	RX_ER	O	**Receive Error.** Signals a receive error condition has occurred. This output is synchronous to RX_CLK.
B5	54	TX_ER	I	**Transmit Error.** Signals a transmit error condition. This signal must be synchronized to TX_CLK.
B6	52	RX_CLK	O	**Receive Clock.** 25 MHz for 100 Mbps operation. 2.5 MHz for 10 Mbps operation. For details, see “Clock Requirements” on page 32 in Chapter 5.0, “Functional Description”.
B2	62	COL	O	**Collision Detected**. The LXT971A Transceiver asserts this output when a collision is detected. This output remains High for the duration of the collision. This signal is asynchronous and is inactive during full- duplex operation.

Table 4. Intel® LXT971A Transceiver MII Data Interface Signal Descriptions (Sheet 2 of 2)

PBGA Pin#	LQFP Pin#	Symbol	Type	Signal Description
A2	63	CRS	O	**Carrier Sense**. During half-duplex operation (Register bit 0.8 = 0), the LXT971A Transceiver asserts this output when either transmitting or receiving data packets. During full-duplex operation (Register bit 0.8 = 1), CRS is asserted only during receive. CRS assertion is asynchronous with respect to RX_CLK. CRS is de-asserted on loss of carrier, synchronous to RX_CLK.

Table 5 lists signal descriptions of the LXT971A Transceiver MII controller interface pins.

Table 5. Intel® LXT971A Transceiver MII Controller Interface Signal Descriptions

PBGA Pin#	LQFP Pin#	Symbol	Type	Signal Description
D3	3	MDDIS	I	**Management Data Disable**. When MDDIS is High, the MDIO is disabled from read and write operations. When MDDIS is Low at power-up or reset, the Hardware Control Interface pins control only the initial or “default” values of their respective register bits. After the power-up/reset cycle is complete, bit control reverts to the MDIO serial channel.
E7	43	MDC	I	**Management Data Clock**. Clock for the MDIO serial data channel. Maximum frequency is 8 MHz.
D8	42	MDIO	I/O	**Management Data Input/Output**. Bidirectional serial data channel for PHY/STA communication.
A1	64	MDINT_L	OD	**Management Data Interrupt**. When Register bit 18.1 = 1, an active Low output on this pin indicates status change. Interrupt is cleared by reading Register 19.

Table 6 lists signal descriptions of the LXT971A Transceiver network interface pins.

Table 6. Intel® LXT971A Transceiver Network Interface Signal Descriptions

PBGA Pin#	LQFP Pin#	Symbol	Type	Signal Description
H2 H3	19 20	TPFOP TPFON	O	**Twisted-Pair/Fiber Outputs, Positive and Negative.** During 100BASE-TX or 10BASE-T operation, TPFOP/N pins drive IEEE 802.3 compliant pulses onto the line. During 100BASE-FX operation, TPFOP/N pins produce differential LVPECL outputs for fiber transceivers.
H4 H5	23 24	TPFIP TPFIN	I	**Twisted-Pair/Fiber Inputs, Positive and Negative.** During 100BASE-TX or 10BASE-T operation, TPFIP/N pins receive differential 100BASE-TX or 10BASE-T signals from the line. During 100BASE-FX operation, TPFIP/N pins receive differential LVPECL inputs from fiber transceivers.
G2	26	SD/TP_L	I	**Signal Detect** / Twisted Pair. SD/TP_L acts as a dual-function input, depending on the LXT971A Transceiver mode. **Normal, Reset, and Power-Up Operations.** “Normal” operation is operation other than reset or power-up. In either reset or power-up, SD/TP_L is used to select one of the two following media modes. • Twisted-pair mode - Connect SD/TP_L Low (Register bit 16.0 = 0). • Fiber mode - Connect SD/TP_L High (Register bit 16.0 = 1). **Twisted-Pair Mode.** For normal operation that uses the twisted-pair mode, connect SD/TP_L to ground. **Fiber Mode.** For normal operation that uses the fiber mode, SD/TP_L acts as the SD input from the fiber transceiver.

Table 7 lists signal descriptions of the LXT971A Transceiver standard bus and interface signals.

Table 7. Intel® LXT971A Transceiver Standard Bus and Interface Signal Descriptions

PBGA Pin#	LQFP Pin#	Symbol	Type	Signal Description
G1 F1 F2 E2 E1	16 15 14 13 12	ADDR0	I I I I I	**Address**. Sets device address.

Table 8 lists signal descriptions of the LXT971A Transceiver configuration and LED driver pins.

Note: Pull-up/pull-down resistors of 10k Ohms can be implemented if LEDs are not used in the design.

Table 8. Intel® LXT971A Transceiver Configuration and LED Driver Signal Descriptions

<table>
<tr><th>PBGA Pin#</th><th>LQFP Pin#</th><th>Symbol</th><th>Type</th><th>Signal Description</th></tr>
<tr><td rowspan="6">D1
D2</td><td rowspan="6">5
6</td><td rowspan="6">TxSLEW0
TxSLEW1</td><td rowspan="6">I</td><td>Tx Output Slew Controls 0 and 1.
These pins select the TX output slew rate (rise and fall time) as follows:</td></tr>
<tr><td>TxSLEW1 | TxSLEW0 | Slew Rate (Rise and Fall Time)</td></tr>
<tr><td>0 | 0 | 3.0 ns</td></tr>
<tr><td>0 | 1 | 3.4 ns</td></tr>
<tr><td>1 | 0 | 3.9 ns</td></tr>
<tr><td>1 | 1 | 4.4 ns</td></tr>
<tr><td>C2</td><td>4</td><td>RESET_L</td><td>I</td><td>Reset.
This active Low input is ORed with the control register Reset bit (Register bit 0.15). The LXT971A Transceiver reset cycle is extended to 258 µs (nominal) after reset is de-asserted.</td></tr>
<tr><td>H1</td><td>17</td><td>RBIAS</td><td>AI</td><td>Reference Current Bias.
This pin provides bias current for the internal circuitry. Must be tied to ground through a 22.1 kΩ, 1% resistor.</td></tr>
<tr><td>H8</td><td>33</td><td>PAUSE</td><td>I</td><td>Pause.
When set High, the LXT971ATransceiver advertises Pause capabilities during auto-negotiation.</td></tr>
<tr><td>H7</td><td>32</td><td>SLEEP</td><td>I</td><td>Sleep.
When set High, this pin enables the LXT971A Transceiver to go into a low-power sleep mode. The value of this pin can be overridden by Register bit 16.6 when in managed mode.</td></tr>
<tr><td>E8</td><td>39</td><td>PWRDWN</td><td>I</td><td>Power Down.
When set High, this pin puts the LXT971A Transceiver in a power-down mode.</td></tr>
<tr><td>B1
C1</td><td>1
2</td><td>REFCLK/XI
XO</td><td>I and O</td><td>Reference Clock Input / Crystal Input and Crystal Output.
A 25 MHz crystal oscillator circuit can be connected across XI and XO. A clock can also be used at XI.
For clock requirements, see Section 5.3.2, “Clock Requirements” on page 32 in the Functional Description section.</td></tr>
<tr><td>E6
F7
F8</td><td>38
37
36</td><td>LED/CFG1
LED/CFG2
LED/CFG3</td><td>I/O</td><td>LED Drivers 1-3.
These pins drive LED indicators. Each LED can display one of several available status conditions as selected by the LED Configuration Register. (For details, see Table 59, “LED Configuration Register - Address 20, Hex 14” on page 101.)
Configuration Inputs 1-3.
These pins also provide initial configuration settings. (For details, see Table 12, “Hardware Configuration Settings for Intel® LXT971A Transceiver” on page 37.)</td></tr>
</table>

Table 9 lists signal descriptions of the LXT971A Transceiver power, ground, and no-connect pins.

Table 9. Intel® LXT971A Transceiver Power, Ground, No-Connect Signal Descriptions

PBGA Pin#	LQFP Pin#	Symbol	Type	Signal Description
A6	51	VCCD	–	**Digital Power.** Requires a 3.3 V power supply.
D4, E3, E4, F3, F4, C6, C3, G7, G8	7, 11, 18, 25, 34, 35, 41, 50, 61	GND	–	**Ground.**
E5, D5	8, 40	VCCIO	–	**MII Power.** Requires either a 3.3 V or a 2.5 V supply. Must be supplied from the same source used to power the MAC on the other side of the MII.
G3, G4	21, 22	VCCA	–	**Analog Power.** Requires a 3.3 V power supply.
B7, C7 D7	9, 10, 44	NC	-	**No Connection**. These pins are not used and should not be terminated.

Table 10 lists signal descriptions of LXT971A Transceiver Joint Test Action Group (JTAG) pins.

Note: If a JTAG port is not used, these pins do not need to be terminated.

Table 10. Intel® LXT971A Transceiver JTAG Test Signal Descriptions

PBGA Pin#	LQFP Pin#	Symbol	Type	Signal Description
F5	27	TDI	I	**Test Data Input**. Test data sampled with respect to the rising edge of TCK.
G5	28	TDO	O	**Test Data Output**. Test data driven with respect to the falling edge of TCK.
F6	29	TMS	I	**Test Mode Select**.
G6	30	TCK	I	**Test Clock**. Clock input for boundary scan.
H6	31	TRST_L	I	**Test Reset**. This active-low test reset input is sourced by ATE.

Table 11 lists pin types and modes of the LXT971A Transceiver.

Note:

- DH = Driven High (Logic 1)
- DL = Driven Low (Logic 0)
- HZ = High Impedance
- ID = Internal Pull-Down (Weak)

Table 11. Intel® LXT971A Transceiver Pin Types and Modes

Modes	RXD3:0	RX_DV	Tx/Rx CLKS Output	RX_ER Output	COL Output	CRS Output	TXD3:0 Input	TX_EN Input	TX_ER Input
HWReset	DL	DL	DH	DL	DL	DL	ID	ID	ID
SFTPWRDN	DL	DL	Active	DL	DL	DL	ID	ID	ID
HWPWRDN	High Z	High Z	High Z	High Z	High Z	High Z	High Z	High Z	High Z
ISOLATE	HZ with ID	HZ with ID	HZ with ID	HZ with ID	HZ with ID	HZ with ID	ID	ID	ID
SLEEP	DL	DL	DL	DL	DL	DL	ID	ID	ID

5.0 Functional Description

This chapter has the following sections:

5.1 Device Overview

The LXT971A Transceiver is a single-port Fast Ethernet 10/100 transceiver that supports 10 Mbps and 100 Mbps networks. It complies with applicable requirements of IEEE 802.3. It directly drives either a 100BASE-TX line or a 10BASE-T line.

Note: The LXT971A Transceiver also supports 100BASE-FX operation through an LVPECL interface.

5.1.1 Comprehensive Functionality

The LXT971A Transceiver provides a standard Media Independent Interface (MII) for 10/100 MACs. The LXT971A Transceiver performs all functions of the Physical Coding Sublayer (PCS) and Physical Media Attachment (PMA) sublayer as defined in the IEEE 802.3 100BASE-X standard. It also performs all functions of the Physical Media Dependent (PMD) sublayer for 100BASE-TX connections.

The LXT971A Transceiver reads its configuration pins on power-up to check for forced operation settings.

If the LXT971A Transceiver is not set for forced operation, it uses auto-negotiation/parallel detection to automatically determine line operating conditions. If the PHY device on the other side of the link supports auto-negotiation, the LXT971A Transceiver auto-negotiates with it using Fast Link Pulse (FLP) Bursts. If the PHY partner does not support auto-negotiation, the LXT971A Transceiver automatically detects the presence of either link pulses (10 Mbps PHY) or Idle symbols (100 Mbps PHY) and sets its operating conditions accordingly.

The LXT971A Transceiver provides half-duplex and full-duplex operation at 100 Mbps and 10 Mbps.

5.1.2 Optimal Signal Processing Architecture

The LXT971A Transceiver incorporates high-efficiency Optimal Signal Processing (OSP) design techniques, which combine optimal properties of digital and analog signal processing.

The receiver utilizes decision feedback equalization to increase noise and cross-talk immunity by as much as 3 dB over an ideal all-analog equalizer. Using OSP mixed-signal processing techniques in the receive equalizer avoids the quantization noise and calculation truncation errors found in traditional DSP-based receivers (typically complex DSP engines with A/D converters). This results in improved receiver noise and cross-talk performance.

The OSP signal processing scheme also requires substantially less computational logic than traditional DSP-based designs. This lowers power consumption and also reduces the logic switching noise generated by DSP engines. This logic switching noise can be a considerable source of EMI generated on the device's power supplies.

The OSP-based LXT971A Transceiver provides improved data recovery, EMI performance, and low power consumption.

5.2 Network Media / Protocol Support

This section includes the following:

The LXT971A Transceiver supports both 10BASE-T and 100BASE-TX Ethernet over twisted-pair or 100 Mbps Ethernet over fiber media (100BASE-FX).

5.2.1 10/100 Network Interface

The network interface port consists of five external pins (two differential signal pairs and a signal detect pin). The I/O pins are shared between twisted-pair (TP) and fiber. For specific pin assignments, see Chapter 4.0, “Signal Descriptions for Intel® LXT971A Transceiver”.

The LXT971A Transceiver output drivers can generate one of the following outputs:

- 100BASE-TX
- 10BASE-T
- 100BASE-FX

When not transmitting data, the LXT971A Transceiver generates IEEE 802.3-compliant link pulses or idle code. Depending on the mode selected, input signals are decoded as one of the following:

- 100BASE-TX
- 10BASE-T
- 100BASE-FX

Auto-negotiation/parallel detection or manual control is used to determine the speed of this interface.

5.2.1.1 Twisted-Pair Interface

The LXT971A Transceiver supports either 100BASE-TX or 10BASE-T connections over 100 Ω, Category 5, Unshielded Twisted Pair (UTP) cable. When operating at 100 Mbps, the LXT971A Transceiver continuously transmits and receives MLT3 symbols. When not transmitting data, the LXT971A Transceiver generates “IDLE” symbols.

During 10 Mbps operation, Manchester-encoded data is exchanged. When no data is being exchanged, the line is left in an idle state. Link pulses are transmitted periodically to keep the link up.

Only a transformer, RJ-45 connector,load resistor, and bypass capacitors are required to complete this interface. On the transmit side, the LXT971A Transceiver has an active internal termination and does not require external termination resistors. Intel's patented waveshaping technology shapes the outgoing signal to help reduce the need for external EMI filters. Four slew rate settings allow the designer to match the output waveform to the magnetic characteristics. On the receive side, the internal impedance is high enough that it has no practical effect on the external termination circuit. (For the slew rate settings, see Table 62, “Transmit Control Register - Address 30, Hex 1E” on page 104.)

5.2.1.2 Fiber Interface

The LXT971A Transceiver fiber port is designed to interface with common industry-standard fiber modules. It incorporates an LVPECL interface that complies with the ANSI X3.166 standard for seamless integration.

Fiber mode is selected through Register bit 16.0 by the following two methods:

1. Drive the SD input to a value greater than 600 mV during power-up and reset states (all LVPECL signaling levels from a fiber transceiver are acceptable).
2. Configure Register bit 16.0 = 1 through the MDIO interface.

5.2.1.3 Remote Fault Detection and Reporting

The LXT971A Transceiver supports two remote fault detection and reporting mechanisms.

- “Remote Fault” refers to a MAC-to-MAC communication function that is transparent to PHY layer devices. It is used only during auto-negotiation, and is applicable only to twisted-pair links.
- “Far-End Fault” is an optional PMA-layer function that may be embedded within PHY devices.

Remote Fault Detection. Register bit 4.13 in the Auto-Negotiation Advertisement Register is reserved for Remote Fault indications. It is typically used when re-starting the auto-negotiation sequence to indicate to the link partner that the link is down because the advertising device detected a local fault.

When the LXT971A Transceiver receives a Remote Fault indication from its partner during auto-negotiation, the following occurs:

- Register bit 5.13 in the Link Partner Base Page Ability Register is set.
- Remote Fault Register bit 1.4 in the MII Status Register is set to pass this information to the local controller.

100BASE-FX Far-End Fault Indication. The LXT971A Transceiver independently detects signal faults from the local fiber transceivers through the SD/TP_L pin. The LXT971A Transceiver also uses Register bit 1.4 to report Remote Fault indications received from its link partner. The LXT971A Transceiver ORs both fault conditions to set bit 1.4 to '1'. Register bit 1.4 is set once and clears to '0' when it is read. In fiber operations, the far-end fault detection process requires idles to establish link. Link does not establish if a far-end fault pattern is the initial signal detected.

Either fault condition causes the LXT971A Transceiver to drop the link unless Forced Link Pass is selected by setting Register bit 16.14 to '1'. A 'link is down' condition is then reported with interrupts and status bits.

In response to locally detected signal faults (that is, the SD/TP_L pin is activated by the local fiber transceiver), the affected port can transmit the far-end fault code if the fault code transmission is enabled by Register bit 16.2.

- When Register bit 16.2 = 0, the LXT971A Transceiver does not transmit far end fault code. It continues to transmit idle code and may or may not drop link depending on the setting for Register bit 16.14.
- When Register bit 16.2 = 1, transmission of the far end fault code is enabled. The LXT971A Transceiver transmits far end fault code if fault conditions are detected by the SD/TP_L pin.

The occurrence of a Far End Fault causes all transmission of data from the Reconciliation Sublayer to stop and the Far End fault code to begin. The Far End Fault code consists of 84 ones followed by a single zero. (This pattern must be repeated three times.)

If the LXT971A Transceiver detects a signal fault condition, it can transmit the Far-End Fault Indication (FEFI) over the fiber link. The FEFI consists of 84 consecutive ones followed by a single zero. This pattern must be repeated at least three times. The LXT971A Transceiver transmits the far-end fault code a minimum of three times if all the following conditions are true:

- Fiber mode is selected.
- Fault Code transmission is enabled (Register bit 16.2 = 1).
- Either Signal Detect indicates no signal, or the receive PLL cannot lock.
- Loopback is not enabled.

5.2.2 MII Data Interface

The LXT971A Transceiver supports a standard Media Independent Interface (MII). The MII consists of a data interface and a management interface. The MII Data Interface passes data between the LXT971A Transceiver and a Media Access Controller (MAC). Separate parallel buses are provided for transmit and receive. This interface operates at either 10 Mbps or 100 Mbps. The speed is set automatically, once the operating conditions of the network link have been determined. For details, see Section 5.6, “MII Operation” on page 41.

Increased MII Drive Strength. A higher Media Independent Interface (MII) drive strength may be desired in some designs to drive signals over longer PCB trace lengths, or over high-capacitive loads, through multiple vias, or through a connector. The MII drive strength in the LXT971A Transceiver can be increased by setting Register bit 26.11 through software control. Setting Register bit 26.11 = 1 through the MDC/MDIO interface sets the MII pins (RXD[3:0], RX_DV, RX_CLK, RX_ER, COL, CRS, and TX_CLK) to a higher drive strength.

5.2.3 Configuration Management Interface

The LXT971A Transceiver provides both an MDIO interface and a reduced hardware control interface for device configuration and management.

5.2.3.1 MDIO Management Interface

MDIO management interface topics include the following:

- Section 5.2.3.1.1, “MDIO Addressing for Intel® LXT971A Transceiver”
- Section 5.2.3.1.2, “MDIO Frame Structure”
- Section 5.2.3.1.3, “MII Interrupts”

The LXT971A Transceiver supports the IEEE 802.3 MII Management Interface also known as the Management Data Input/Output (MDIO) Interface. This interface allows upper-layer devices to monitor and control the state of the LXT971A Transceiver. The MDIO interface consists of a physical connection, a specific protocol that runs across the connection, and an internal set of addressable registers.

Some registers are required and their functions are defined by the IEEE 802.3 standard. The LXT971A Transceiver also supports additional registers for expanded functionality. The LXT971A Transceiver supports multiple internal registers, each of which is 16 bits wide. Specific register bits are referenced using an “X.Y” notation, where X is the register number (0-31) and Y is the bit number (0-15).

The physical interface consists of a data line (MDIO) and clock line (MDC). Operation of this interface is controlled by the MDDIS input pin. When MDDIS is High, the MDIO read and write operations are disabled and the Hardware Control Interface provides primary configuration control. When MDDIS is Low, the MDIO port is enabled for both read and write operations and the Hardware Control Interface is not used.

5.2.3.1.1 MDIO Addressing for Intel® LXT971A Transceiver

The MDIO addressing protocol allows a controller to communicate with multiple LXT971A Transceivers. Pins ADDR[4:0] can be used to determine the PHY device address that is selected.

5.2.3.1.2 MDIO Frame Structure

The physical interface consists of a data line (MDIO) and clock line (MDC). The frame structure is shown in Figure 4 and Figure 5 (Read and Write).

MDIO Interface timing is given in Chapter 7.0, “Electrical Specifications”.

Figure 4. Management Interface Read Frame Structure

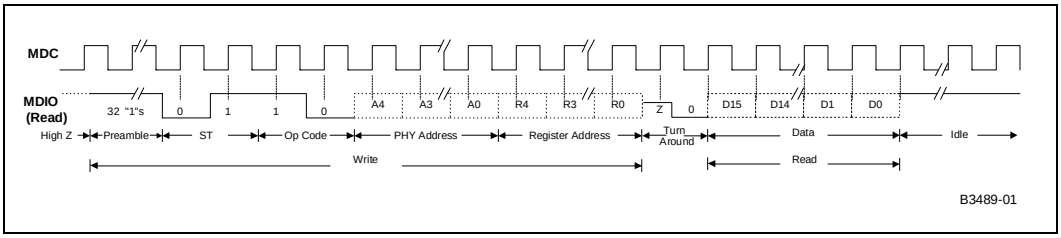
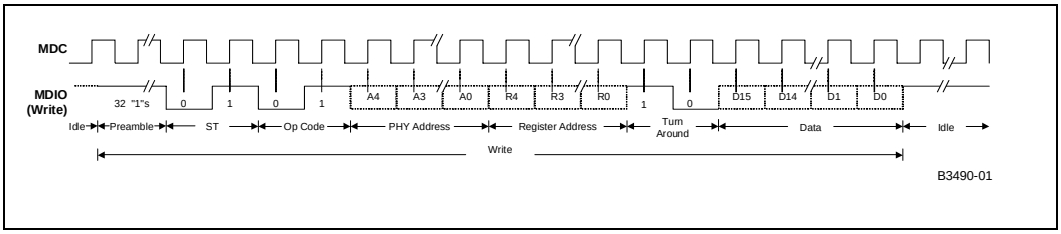


Figure 5. Management Interface Write Frame Structure

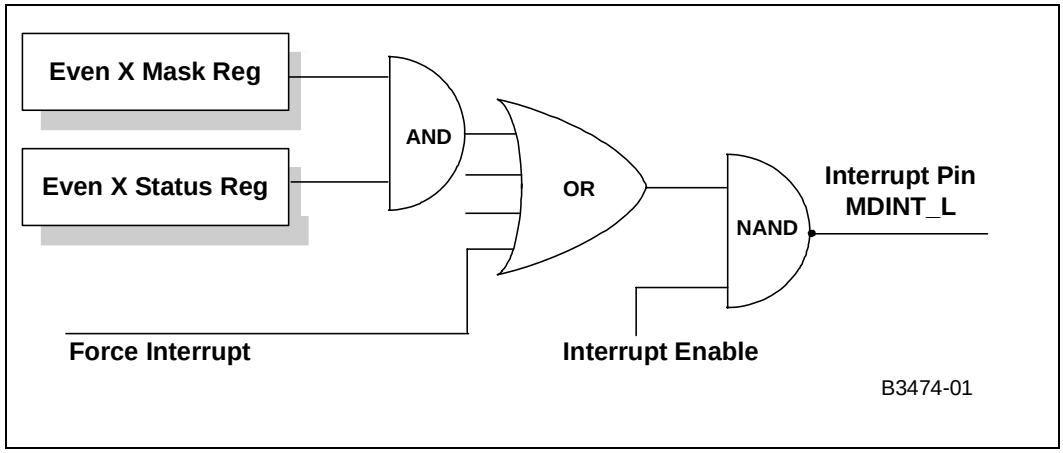


5.2.3.1.3 MII Interrupts

Figure 6 shows the MII interrupt logic. The LXT971A Transceiver provides a hardware interrupt pin (MDINT_L) and two dedicated interrupt registers, Register 18 and Register 19.

- Register 18 provides interrupt enable and mask functions. Setting Register bit 18.1 = 1 enables the device to request interrupt via the MDINT_L pin. An active Low on this pin indicates a status change on the LXT971A Transceiver. Interrupts may be caused by any of the following four conditions:
  - — Auto-negotiation complete
  - — Speed status change
  - — Duplex status change
  - — Link status change
- Register 19 provides the interrupt status.

Figure 6. Intel® LXT971A Transceiver MII Interrupt Logic



5.2.3.2 Hardware Control Interface

The LXT971A Transceiver provides a Hardware Control Interface for applications where the MDIO is not desired. The Hardware Control Interface uses the hardware configuration pins to set device configuration. For details, see Section 5.4.4, “Hardware Configuration Settings” on page 37.

5.3 Operating Requirements

5.3.1 Power Requirements

The LXT971A Transceiver requires three power supply inputs:

- VCCA
- VCCD
- VCCIO

The digital and analog circuits require 3.3 V supplies (VCCA and VCCD). These inputs may be supplied from a single source. Each supply input must be de-coupled to ground.

An additional supply may be used for the MII (VCCIO). The supply may be either +2.5 V or +3.3 V. Also, the inputs on the MII interface are tolerant to 5 V signals from the controller on the other side of the MII interface. For MII I/O characteristics, see Table 23, “Digital I/O Characteristics1 - MII Pins” on page 72.

Note: Bring up power supplies as close to the same time as possible.

Note: As a matter of good practice, keep power supplies as clean as possible.

5.3.2 Clock Requirements

5.3.2.1 External Crystal/Oscillator

The LXT971A Transceiver requires a reference clock input that is used to generate transmit signals and recover receive signals. It may be provided by either of two methods: by connecting a crystal across the oscillator pins (XI and XO) with load capacitors, or by connecting an external clock source to pin XI.

The connection of a clock source to the XI pin requires the XO pin to be left open. To minimize transmit jitter, Intel recommends a crystal-based clock instead of a derived clock (that is, a PLL-based clock).

A crystal is typically used in NIC applications. An external 25 MHz clock source, rather than a crystal, is frequently used in switch applications. For clock timing requirements, see Table 24, “I/O Characteristics - REFCLK/XI and XO Pins” on page 73.

5.3.2.2 MDIO Clock

The MII management channel (MDIO) also requires an external clock. The managed data clock (MDC) speed is a maximum of 8 MHz. For details, see Table 41, “Intel® LXT971A Transceiver MDIO Timing” on page 85.

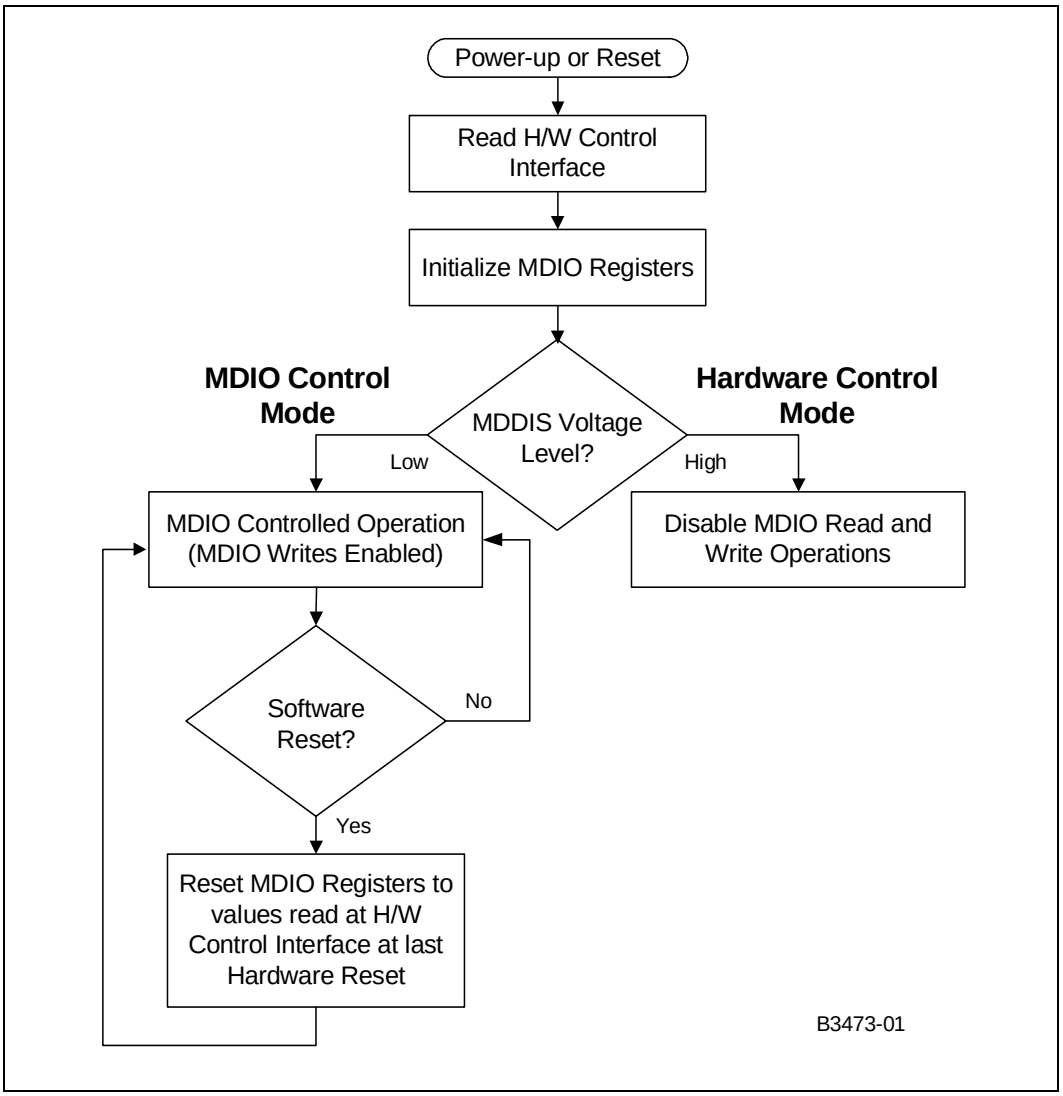
5.4 Initialization

This section includes the following topics:

When the LXT971A Transceiver is first powered on, reset, or encounters a link failure state, it checks the MDIO register configuration bits to determine the line speed and operating conditions to use for the network link.

Figure 7 shows the initialization sequence for the LXT971A Transceiver. The configuration bits may be set by the Hardware Control or MDIO interface.

Figure 7. Initialization Sequence for Intel® LXT971A Transceiver



5.4.1 MDIO Control Mode and Hardware Control Mode

In the MDIO Control mode, the LXT971A Transceiver reads the Hardware Control Interface pins to set the initial (default) values of the MDIO registers. Once the initial values are set, bit control reverts to the MDIO interface.

The following modes are available using either Hardware Control or MDIO control:

- Force network link to 100BASE-FX (Fiber)
- Force network link operation to:
  - 100BASE-TX, Full-Duplex
  - 100BASE-TX, Half-Duplex
  - 10BASE-T, Full-Duplex
  - 10BASE-T, Half-Duplex
- Allow auto-negotiation/parallel-detection

In the Hardware Control Mode, the LXT971A Transceiver disables direct-write operations to the MDIO registers through the MDIO Interface. On power-up or hardware reset, the LXT971A Transceiver reads the Hardware Control Interface pins and sets the MDIO registers accordingly.

When the network link is forced to a specific configuration, the LXT971A Transceiver immediately begins operating the network interface as commanded. When auto-negotiation is enabled, the LXT971A Transceiver begins the auto-negotiation/parallel-detection operation.

5.4.2 Reduced-Power Modes

This section discusses the LXT971A Transceiver reduced-power modes.

5.4.2.1 Hardware Power Down

The hardware power-down mode is controlled by the PWRDWN pin. When PWRDWN is High, the following conditions are true:

- The LXT971A Transceiver network port and clock are shut down.
- All outputs are tristated.
- All weak pad pull-up and pull-down resistors are disabled.
- The MDIO registers are not accessible.

5.4.2.2 Software Power Down

Software power-down control is provided by Register bit 0.11 in the Control Register. (See Table 45 on page 88.) During soft power-down, the following conditions are true:

- The network port is shut down.
- The MDIO registers remain accessible.

5.4.2.3 Sleep Mode

The LXT971A Transceiver supports a power-saving sleep mode. Sleep mode is enabled when SLEEP is asserted via pin 32(LQFP)/H7(PBGA). The value of pin 32/H7 can be overridden by Register bit 16.6 in managed mode as listed in Table 55, "Configuration Register - Address 16, Hex 10" on page 97. The LXT971A Transceiver enters into sleep mode when SLEEP is enabled and no energy is detected on the twisted-pair input for 1 to 3 seconds. (The time is controlled by Register bits 16.4:3 in the Configuration Register, with a default of 3.04 seconds.)

During this mode, the LXT971A Transceiver still responds to management transactions (MDC/MDIO). In this mode the power consumption is minimized, and the supply current is reduced below the maximum value given in Table 21 on page 70. If the LXT971A Transceiver detects activity on the twisted-pair inputs, it comes out of the sleep state and checks for link. If no link is detected in from 1 to 3 seconds (the time is programmable) it reverts to the low power sleep state.

Note: Sleep mode is not functional in fiber network applications.

5.4.3 Reset for Intel® LXT971A Transceiver

The LXT971A Transceiver provides both hardware and software resets, each of which manage differently the configuration control of auto-negotiation, speed, and duplex-mode selection.

For a software reset, Register bit 0.15 = 1. For register bit definitions used for software reset, see Table 45, "Control Register - Address 0, Hex 0" on page 88.

- During a software reset, bit settings in Table 49, "Auto-Negotiation Advertisement Register - Address 4, Hex 4" on page 92 are not re-read from the LXT971A Transceiver configuration pins. Instead, the bit settings revert to the values that were read in during the last hardware reset. Therefore, any changes to pin values made since the last hardware reset are not detected during a software reset.
- During a software reset, registers are available for reading. To see when the LXT971A Transceiver has completed reset, the reset bit can be polled (that is, Register bit 0.15 = 0).

For pin settings used during a hardware reset, see Section 5.4.4, "Hardware Configuration Settings". During a hardware reset, configuration settings for auto-negotiation and speed are read in from pins, and register information is unavailable for 1 ms after de-assertion of the reset.

5.4.4 Hardware Configuration Settings

The LXT971A Transceiver provides a hardware option to set the initial device configuration. As listed in Table 12, the hardware option uses the hardware configuration pins, the settings for which provide control bits.

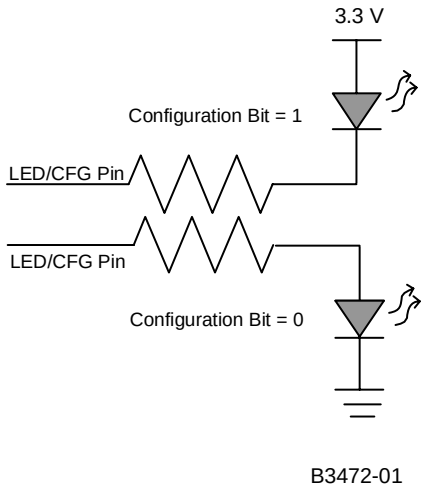
Table 12. Hardware Configuration Settings for Intel® LXT971A Transceiver

Desired Mode			LED/CFG Pin Settings[1]			Resulting Register Bit Values						
						Control Register			Auto-Negotiation Advertisement Register			
Auto-Neg.	Speed (Mbps)	Duplex	1	2	3	Auto-Neg. 0.12	Speed 0.13	Full-Duplex 0.8	100 BASE-TX Full-Duplex 4.8	100 BASE-TX 4.7	10 BASE-T Full-Duplex 4.6	10 BASE-T 4.5
Disabled	10	Half	L	L	L	0	0	0	N/A Auto-Negotiation Advertisement			
		Full	L	L	H		0	1				
	100	Half	L	H	L		1	0				
		Full	L	H	H		1	1				
Enabled	100 Only	Half	H	L	L	1	1	0	0	1	0	0
		Full/Half	H	L	H		1	1	1	1	0	0
	10/100	Half Only	H	H	L		1	0	0	1	0	1
		Full or Half	H	H	H		1	1	1	1	1	1

1. L = Low, and H = High. For LED/CFG pin assignments, see Chapter 3.0, "Ball and Pin Assignments for Intel® LXT971A Transceiver".

As shown in Figure 8, the LED drivers can operate as either open-drain or open-source circuits.

Figure 8. Hardware Configuration Settings



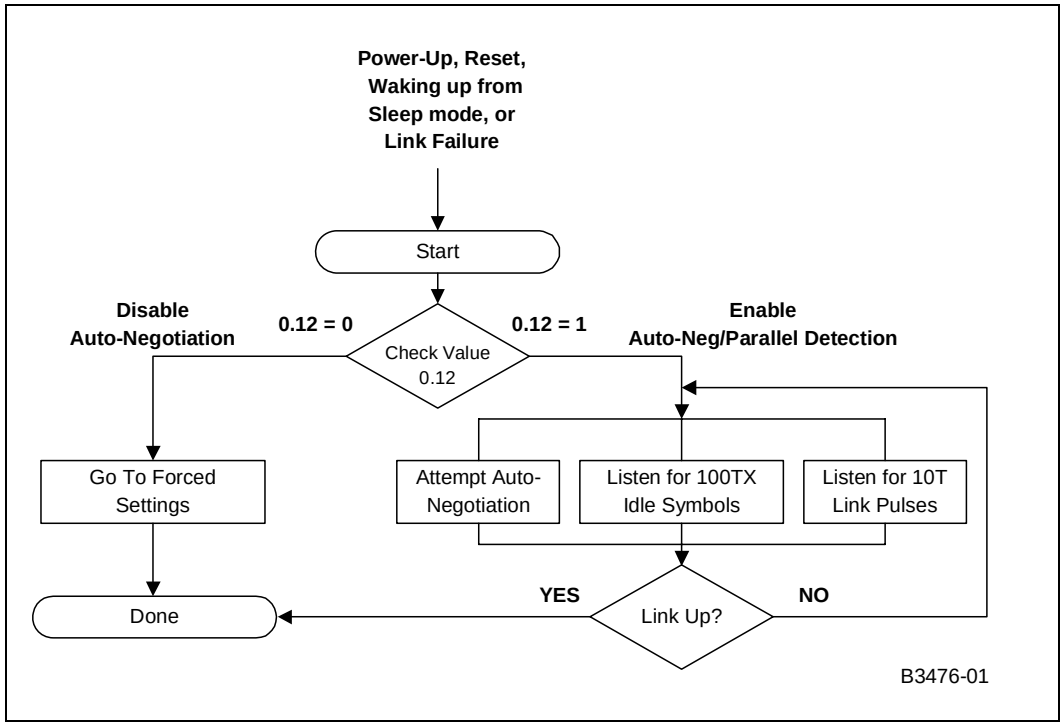
1. The LED/CFG pins automatically adjust their polarity upon power-up or reset.
2. Unused LEDs may be implemented with pull-up/ pull-down resistors of 10 K.

5.5 Establishing Link

Figure 9 shows an overview of link establishment for the LXT971A Transceiver.

Note: When a link is established by using parallel detection, the LXT971A Transceiver sets the duplex mode to half-duplex, as defined by the IEEE 802.3 standard.

Figure 9. Intel® LXT971A Transceiver Link Establishment Overview



5.5.1 Auto-Negotiation

If not configured for forced operation, the LXT971A Transceiver attempts to auto-negotiate with its link partner by sending Fast Link Pulse (FLP) bursts. Each burst consists of up to 33 link pulses spaced 62.5 µs apart. Odd link pulses (clock pulses) are always present. Even link pulses (data pulses) may be absent or present to indicate a '0' or a '1'. Each FLP burst exchanges 16 bits of data, which are referred to as a "link code word". All devices that support auto-negotiation must implement the "Base Page" defined by the IEEE 802.3 standard (Registers 4 and 5).

The LXT971A Transceiver also supports the optional "Next Page" function as listed in Table 52, "Auto-Negotiation Next Page Transmit Register - Address 7, Hex 7" on page 95 and Table 53, "Auto-Negotiation Link Partner Next Page Receive Register - Address 8, Hex 8" on page 95.

5.5.1.1 Base Page Exchange

By exchanging Base Pages, the LXT971A Transceiver and its link partner communicate their capabilities to each other. Both sides must receive at least three consecutive identical base pages for negotiation to continue. Each side identifies the highest common capabilities that both sides support, and each side configures itself accordingly.

5.5.1.2 Manual Next Page Exchange

"Next Page Exchange" information is additional information that exceeds the information required by Base Page exchange and that is sent by "Next Pages". The LXT971A Transceiver fully supports the IEEE 802.3 standard method of negotiation through the Next Page exchange.

The Next Page exchange uses Register 7 to send information and Register 8 to receive it. Next Page exchange occurs only if both ends of the link partners advertise their ability to exchange Next Pages. Register bit 6.1 is used to make manual next page exchange easier for software. This register bit is cleared when a new negotiation occurs, preventing the user from reading an old value in Register 6 and assuming there is valid information in Registers 5 and 8.

5.5.1.3 Controlling Auto-Negotiation

When auto-negotiation is controlled by software, Intel recommends the following steps:

1. After power-up, power-down, or reset, the power-down recovery time (specified in Table 43, "Intel® LXT971A Transceiver RESET_L Pulse Width and Recovery Timing" on page 87) must be exhausted before proceeding.
2. Set the Auto-Negotiation Advertisement Register bits.
3. Enable auto-negotiation. (Set MDIO Register bit 0.12 = 1.)
4. To ensure proper operation, enable or restart auto-negotiation as soon as possible after writing to Register 4.

5.5.2 Parallel Detection

In parallel with auto-negotiation, the LXT971A Transceiver also monitors for 10 Mbps Normal Link Pulses (NLP) or 100 Mbps Idle symbols. If either symbol is detected, the device automatically reverts to the corresponding speed in half-duplex mode. Parallel detection allows the LXT971A Transceiver to communicate with devices that do not support auto-negotiation.

When parallel detection resolves a link, the link must be established in half-duplex mode. According to IEEE standards, the forced link partner cannot be configured to full-duplex. If the auto-negotiation link partner does not advertise half-duplex capability at the speed of the forced link partner, link is not established. The IEEE Standard prevents full-duplex-to-half-duplex link connections.

5.6 MII Operation

This section includes the following topics:

The LXT971A Transceiver implements the Media Independent Interface (MII) as defined by the IEEE 802.3 standard. Separate channels are provided for transmitting data from the MAC to the LXT971A Transceiver (TXD), and for passing data received from the line (RXD) to the MAC. Each channel has its own clock, data bus, and control signals.

The following signals are used to pass received data to the MAC:

- COL
- CRS
- RX_CLK
- RX_DV
- RX_ER
- RXD[3:0]

The following signals are used to transmit data from the MAC:

- TX_CLK
- TX_EN
- TX_ER
- TXD[3:0]

The LXT971A Transceiver supplies both clock signals as well as separate outputs for carrier sense and collision. Data transmission across the MII is normally implemented in 4-bit-wide nibbles.

5.6.1 MII Clocks

The LXT971A Transceiver is the master clock source for data transmission, and it supplies both MII clocks (RX_CLK and TX_CLK). It automatically sets the clock speeds to match link conditions.

- When the link is operating at 100 Mbps, the clocks are set to 25 MHz.
- When the link is operating at 10 Mbps, the clocks are set to 2.5 MHz.

Figure 10 through Figure 12 show the clock cycles for each mode.

Note: The transmit data and control signals must always be synchronized to TX_CLK by the MAC. The LXT971A Transceiver samples these signals on the rising edge of TX_CLK.

Figure 10. Clocking for 10BASE-T

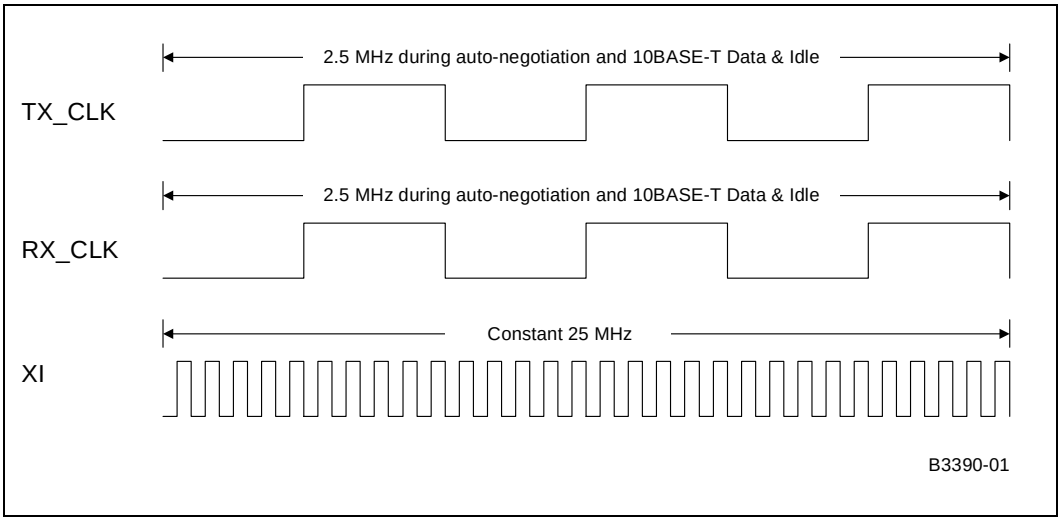


Figure 11. Clocking for 100BASE-X

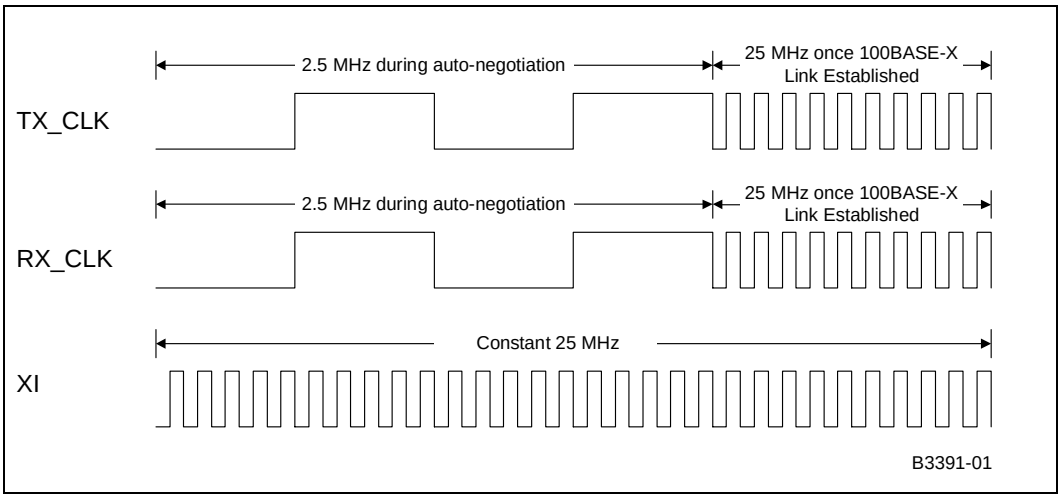
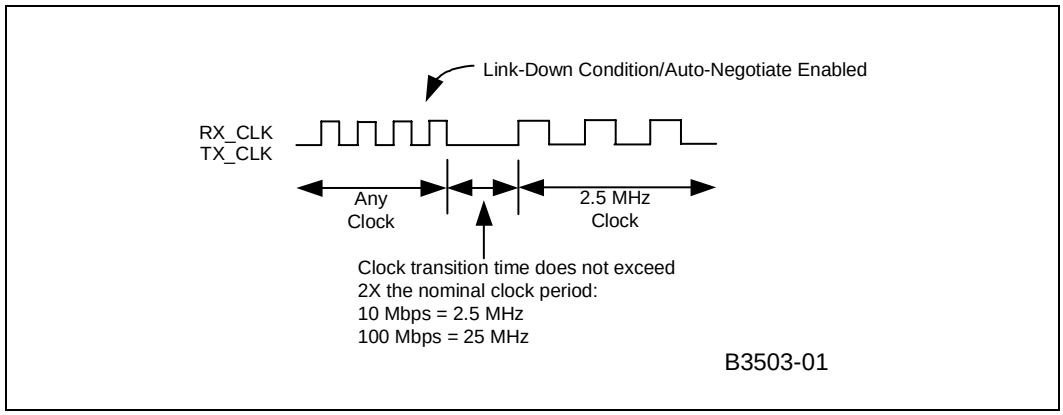


Figure 12. Clocking for Link Down Clock Transition



5.6.2 Transmit Enable

The MAC must assert TX_EN the same time as the first nibble of preamble and de-assert TX_EN after the last nibble of the packet.

5.6.3 Receive Data Valid

The LXT971A Transceiver asserts RX_DV when it receives a valid packet. Timing changes depend on line operating speed:

- For 100BASE-TX links, RX_DV is asserted from the first nibble of preamble to the last nibble of the data packet.
- For 10BASE-T links, the entire preamble is truncated. RX_DV is asserted with the first nibble of the Start of Frame Delimiter (SFD) “5D” and remains asserted until the end of the packet.

5.6.4 Carrier Sense

Carrier Sense (CRS) is an asynchronous output.

- CRS is always generated when the LXT971A Transceiver receives a packet from the line.
- CRS is also generated when the LXT971A Transceiver is in half-duplex mode when a packet is transmitted.

Table 13 summarizes the conditions for assertion of carrier sense, data loopback, and collision signals. Carrier sense is not generated when a packet is transmitted and in full-duplex mode.

Table 13. Carrier Sense, Loopback, and Collision Conditions

Speed	Duplex Condition	Carrier Sense	Test Loop-back[1, 2]	Operational Loop-back[1, 2]	Collision
100 Mbps	Full-Duplex	Receive Only	Yes	No	None
	Half-Duplex	Transmit or Receive	No	No	Transmit and Receive
10 Mbps	Full-Duplex	Receive Only	Yes	No	None
	Half-Duplex, Register bit 16.8 = 0	Transmit or Receive	Yes	Yes	Transmit and Receive
	Half-Duplex, Register bit 16.8 = 1	Transmit or Receive	No	No	Transmit and Receive

1. Test Loopback is enabled when Register bit 0.14 = 1.
2. For descriptions of Test Loopback and Operational Loopback, see Section 5.6.7, “Loopback” on page 45.

5.6.5 Error Signals

When the LXT971A Transceiver is in 100 Mbps mode and receives an invalid symbol from the network, it asserts RX_ER and drives “0101” on the RXD pins.

When the MAC asserts TX_ER, the LXT971A Transceiver drives “H” symbols out on the TPFOP/N pins.

5.6.6 Collision

The LXT971A Transceiver asserts its collision signal asynchronously to any clock whenever the line state is half-duplex and the transmitter and receiver are active at the same time. Table 13 summarizes the conditions for assertion of carrier sense, data loopback, and collision signals.

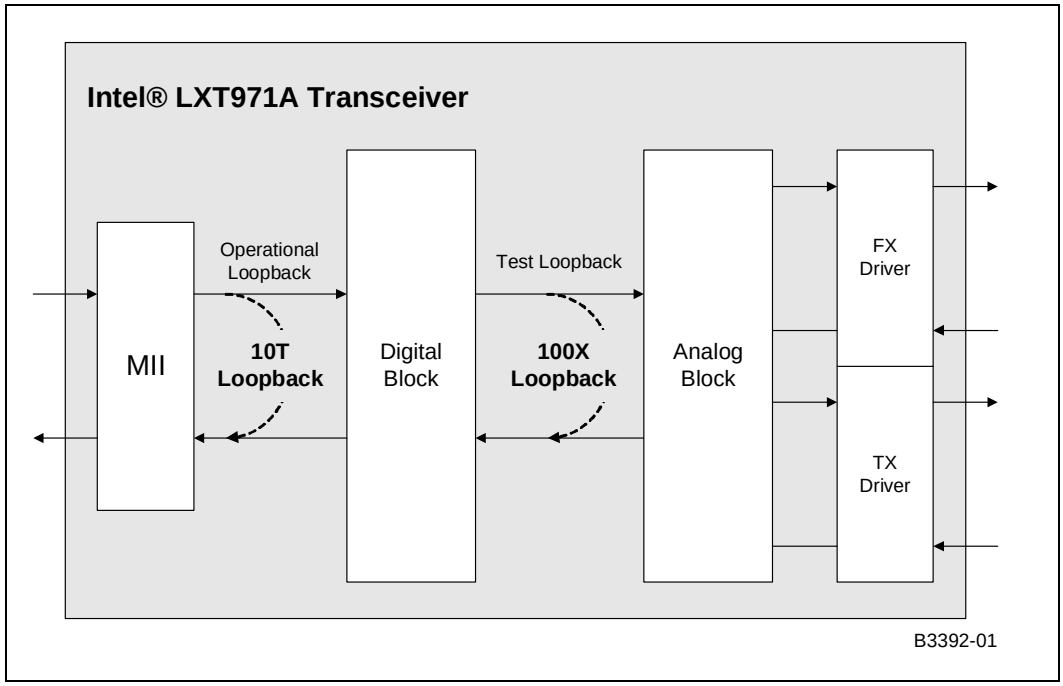
5.6.7 Loopback

The LXT971A Transceiver provides the following loopback functions:

- Section 5.6.7.1, “Operational Loopback”
- Section 5.6.7.2, “Internal Digital Loopback (Test Loopback)”

Figure 13 shows LXT971A Transceiver operational and test loopback paths. (An internal digital loopback path is not shown.) For more information on loopback functions, see Table 13, “Carrier Sense, Loopback, and Collision Conditions” on page 44.)

Figure 13. Intel® LXT971A Transceiver Loopback Paths



5.6.7.1 Operational Loopback

- Operational loopback is provided for 10 Mbps half-duplex links when Register bit 16.8 = 0. Data that the MAC (TXData) transmits loops back on the receive side of the MII (RXData).
- Operational loopback is not provided for 100 Mbps links, full-duplex links, or when Register 16.8 = 1.

5.6.7.2 Internal Digital Loopback (Test Loopback)

A test loopback function is provided for diagnostic testing of the LXT971A Transceiver. During test loopback, twisted-pair and fiber interfaces are disabled. Data transmitted by the MAC is internally looped back by the LXT971A Transceiver and returned to the MAC.

Test loopback is available for both 100BASE-TX and 10BASE-T operation, and is enabled by setting the following register bits:

- Register bit 0.14 = 1 (Setting to enable loopback mode)
- Register bit 0.8 = 1 (Setting for full-duplex mode)
- Register bit 0.12 = 0. (Disable auto-negotiation.)

Test loopback is also available for 100BASE-FX operation. Test loopback in this mode is enabled by setting Register bit 0.14 = 1 and tying the SD input to an LVPECL logic High value (2.4 V).

5.7 100 Mbps Operation

5.7.1 100BASE-X Network Operations

During 100BASE-X operation, the LXT971A Transceiver transmits and receives 5-bit symbols across the network link.

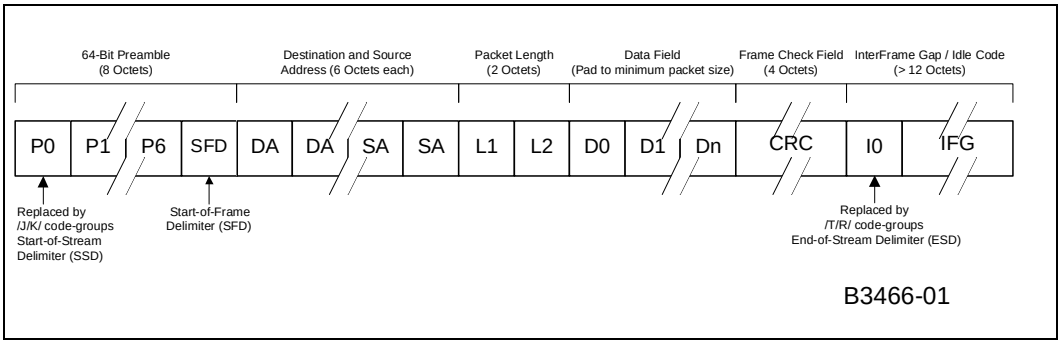
Figure 14 shows the structure of a standard frame packet in 100BASE-X mode. When the MAC is not actively transmitting data, the LXT971A Transceiver sends out Idle symbols on the line.

As Figure 14 shows, the MAC starts each transmission with a preamble pattern. As soon as the LXT971A Transceiver detects the start of preamble, it transmits a Start-of-Stream Delimiter (SSD, symbols J and K) to the network. It then encodes and transmits the rest of the packet, including the balance of the preamble, the SFD, packet data, and CRC.

Once the packet ends, the LXT971A Transceiver transmits the End-of-Stream Delimiter (ESD, symbols T and R) and then returns to transmitting Idle symbols.

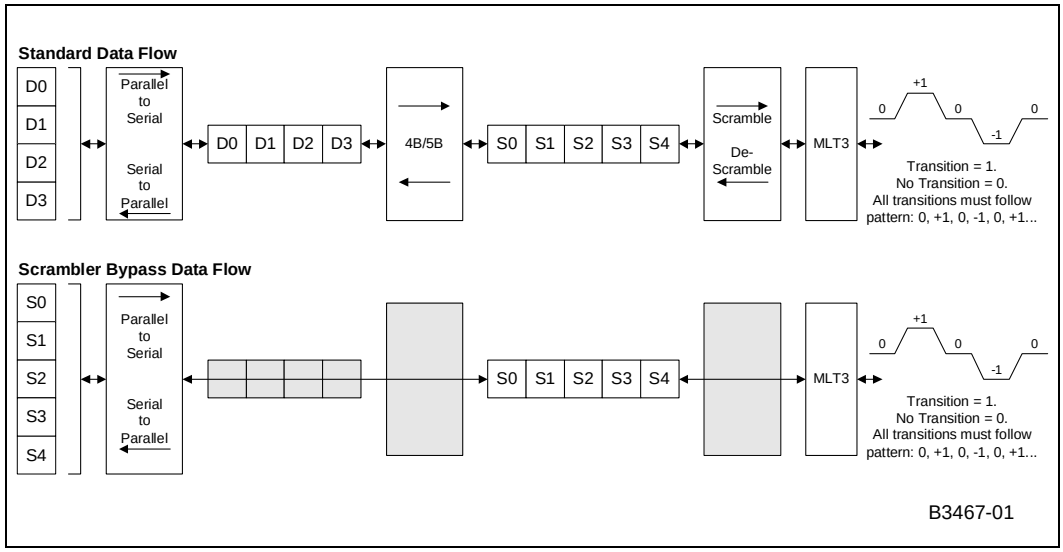
For details on the symbols used, see 4B/5B coding listed in Table 14, “4B/5B Coding” on page 51.

Figure 14. 100BASE-X Frame Format



As shown in Figure 15, in 100BASE-TX mode, the LXT971A Transceiver scrambles and transmits the data to the network using MLT-3 line code. MLT-3 signals received from the network are de-scrambled, decoded, and sent across the MII to the MAC.

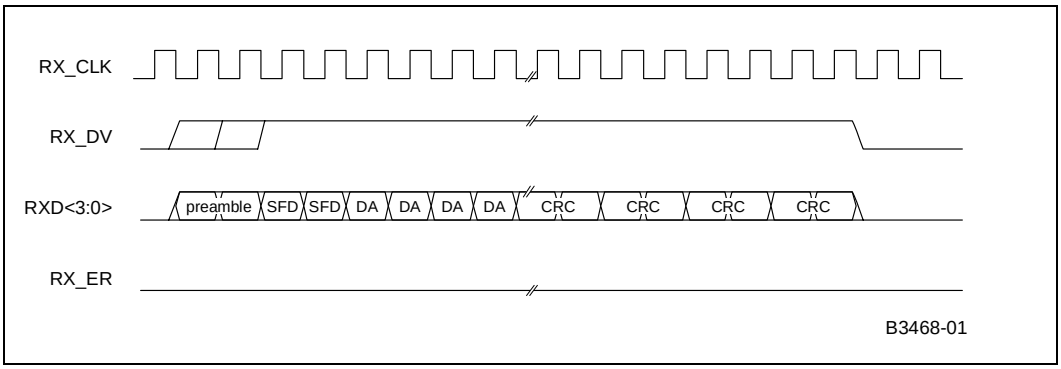
Figure 15. 100BASE-TX Data Path



Note: In 100BASE-FX mode, the LXT971A Transceiver transmits and receives NRZI signals across the LVPECL interface. An external 100BASE-FX transceiver module is required to complete the fiber connection. To enable 100BASE-FX operation, auto-negotiation must be disabled and fiber mode selected.

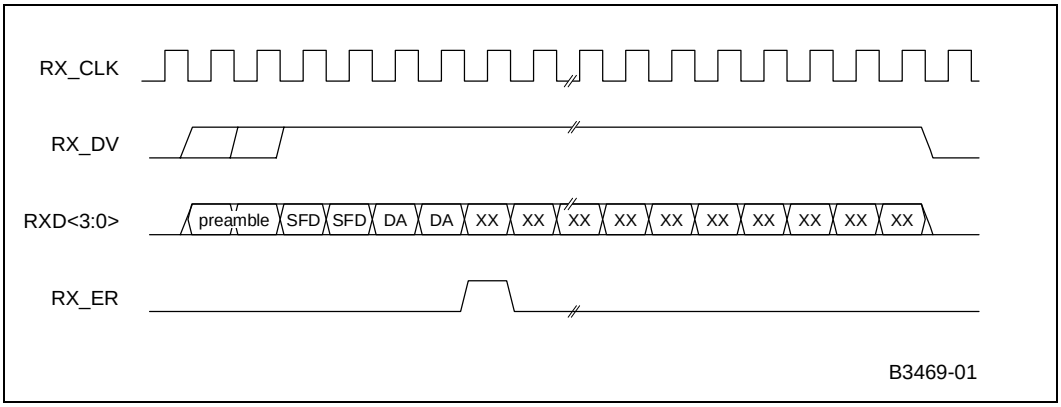
Figure 16 shows normal reception with no errors.

Figure 16. 100BASE-TX Reception with No Errors



As shown in Figure 17, when the LXT971A Transceiver receives invalid symbols from the line, it asserts RX_ER.

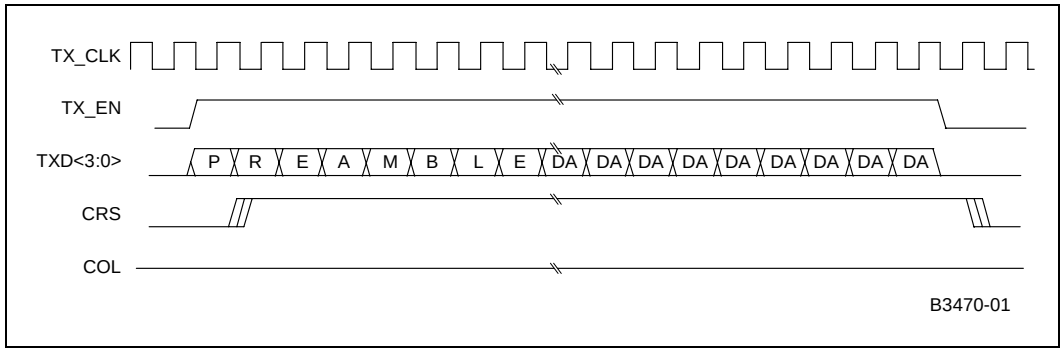
Figure 17. 100BASE-TX Reception with Invalid Symbol



5.7.2 Collision Indication

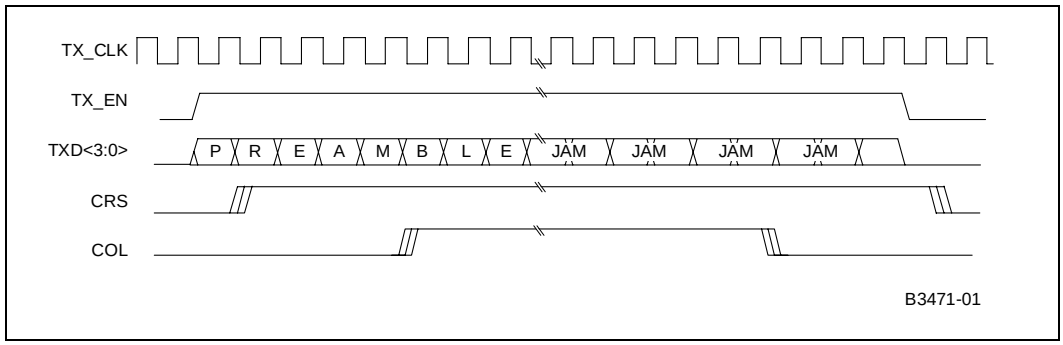
Figure 18 shows normal transmission.

Figure 18. 100BASE-TX Transmission with No Errors



Upon detection of a collision, the COL output is asserted and remains asserted for the duration of the collision as shown in Figure 19.

Figure 19. 100BASE-TX Transmission with Collision



5.7.3 100BASE-X Protocol Sublayer Operations

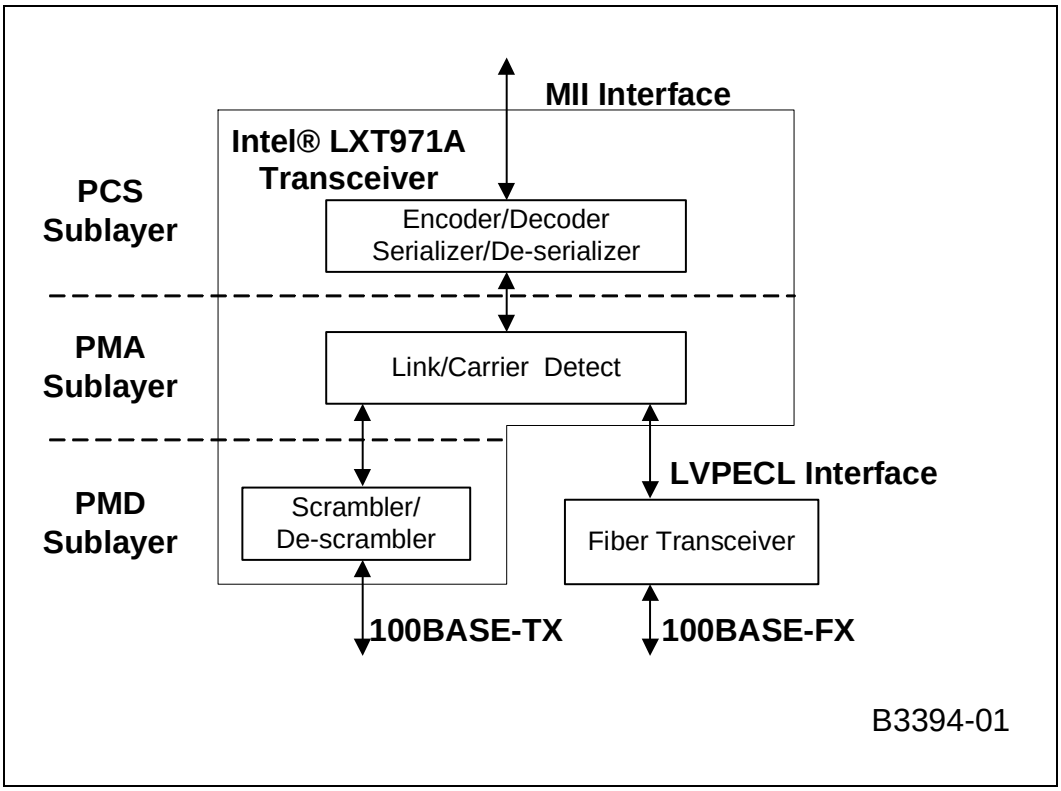
With respect to the 7-layer communications model, the LXT971A Transceiver is a Physical Layer 1 (PHY) device.

The LXT971A Transceiver implements the following sublayers of the reference model defined by the IEEE 802.3 standard, and discussed from the reference model point of view:

- Section 5.7.3.1, “Physical Coding Sublayer”
- Section 5.7.3.2, “Physical Medium Attachment Sublayer”
- Section 5.7.3.3, “Twisted-Pair Physical Medium Dependent Sublayer”
- Section 5.7.3.4, “Fiber PMD Sublayer”

Figure 20 shows the LXT971A Transceiver protocol sublayers.

Figure 20. Intel® LXT971A Transceiver Protocol Sublayers



5.7.3.1 Physical Coding Sublayer

The Physical Coding Sublayer (PCS) provides the MII interface, as well as the 4B/5B encoding/decoding function.

For 100BASE-TX and 100BASE-FX operation, the PCS layer provides IDLE symbols to the PMD-layer line driver as long as TX_EN is de-asserted.

5.7.3.1.1 Preamble Handling

When the MAC asserts TX_EN, the PCS substitutes a /J/K symbol pair, also known as the Start-of-Stream Delimiter (SSD), for the first two nibbles received across the MII. The PCS layer continues to encode the remaining MII data, following the 4B/5B coding in Table 14, until TX_EN is de-asserted. It then returns to supplying IDLE symbols to the line driver.

In the receive direction, the PCS layer performs the opposite function, substituting two preamble nibbles for the SSD. In 100 Mbps operation, preamble is always passed through the PCS layer to the MII interface.

Table 14. 4B/5B Coding (Sheet 1 of 2)

Code Type	4B Code 3 2 1 0	Name	5B Code 4 3 2 1 0	Interpretation
DATA	0 0 0 0	0	1 1 1 1 0	Data 0
	0 0 0 1	1	0 1 0 0 1	Data 1
	0 0 1 0	2	1 0 1 0 0	Data 2
	0 0 1 1	3	1 0 1 0 1	Data 3
	0 1 0 0	4	0 1 0 1 0	Data 4
	0 1 0 1	5	0 1 0 1 1	Data 5
	0 1 1 0	6	0 1 1 1 0	Data 6
	0 1 1 1	7	0 1 1 1 1	Data 7
	1 0 0 0	8	1 0 0 1 0	Data 8
	1 0 0 1	9	1 0 0 1 1	Data 9
	1 0 1 0	A	1 0 1 1 0	Data A
	1 0 1 1	B	1 0 1 1 1	Data B
	1 1 0 0	C	1 1 0 1 0	Data C
	1 1 0 1	D	1 1 0 1 1	Data D
	1 1 1 0	E	1 1 1 0 0	Data E
	1 1 1 1	F	1 1 1 0 1	Data F
IDLE	undefined	I [1]	1 1 1 11	Used as inter-stream fill code

1. The /I/ (Idle) code group is sent continuously between frames.
2. The /J/ and /K/ (SSD) code groups are always sent in pairs, and /K/ follows /J/.
3. The /T/ and /R/ (ESD) code groups are always sent in pairs, and /R/ follows /T/.
4. An /H/ (Error) code group is used to signal an error condition.

Table 14. 4B/5B Coding (Sheet 2 of 2)

Code Type	4B Code 3 2 1 0	Name	5B Code 4 3 2 1 0	Interpretation
CONTROL	0 1 0 1	J [2]	1 1 0 0 0	Start-of-Stream Delimiter (SSD), part 1 of 2
	0 1 0 1	K [2]	1 0 0 0 1	Start-of-Stream Delimiter (SSD), part 2 of 2
	Undefined	T [3]	0 1 1 0 1	End-of-Stream Delimiter (ESD), part 1 of 2
	Undefined	R [3]	0 0 1 1 1	End-of-Stream Delimiter (ESD), part 2 of 2
INVALID	Undefined	H [4]	0 0 1 0 0	Transmit Error. Used to force signaling errors
	Undefined	Invalid	0 0 0 0 0	Invalid
	Undefined	Invalid	0 0 0 0 1	Invalid
	Undefined	Invalid	0 0 0 1 0	Invalid
	Undefined	Invalid	0 0 0 1 1	Invalid
	Undefined	Invalid	0 0 1 0 1	Invalid
	Undefined	Invalid	0 0 1 1 0	Invalid
	Undefined	Invalid	0 1 0 0 0	Invalid
	Undefined	Invalid	0 1 1 0 0	Invalid
	Undefined	Invalid	1 0 0 0 0	Invalid
	Undefined	Invalid	1 1 0 0 1	Invalid

1. The /I/ (Idle) code group is sent continuously between frames.
2. The /J/ and /K/ (SSD) code groups are always sent in pairs, and /K/ follows /J/.
3. The /T/ and /R/ (ESD) code groups are always sent in pairs, and /R/ follows /T/.
4. An /H/ (Error) code group is used to signal an error condition.

5.7.3.2 Physical Medium Attachment Sublayer

5.7.3.2.1 Link

In 100 Mbps mode, link is established when the descrambler becomes locked and remains locked for approximately 50 ms. Link remains up unless the descrambler receives less than 16 consecutive idle symbols in any 2 ms period. This operation filters out small noise hits that may disrupt the link.

In 100 Mbps mode, link is established when the descrambler becomes locked and remains locked for approximately 50 ms. Link remains up unless the descrambler receives less than 16 consecutive idle symbols in any 2 ms period. This operation filters out small noise hits that may disrupt the link.

For short periods, MLT-3 idle waveforms meet all criteria for 10BASE-T start delimiters. A working 10BASE-T receive may temporarily indicate link to 100BASE-TX waveforms. However, the PHY does not bring up a permanent 10 Mbps link.

The LXT971A Transceiver reports link failure through the MII status bits (Register bits 1.2 and 17.10) and interrupt functions. Link failure causes the LXT971A Transceiver to re-negotiate if auto-negotiation is enabled.

5.7.3.2.2 Link Failure Override

The LXT971A Transceiver normally transmits data packets only if it detects the link is up. Setting Register bit 16.14 = 1 overrides this function, allowing the LXT971A Transceiver to transmit data packets even when the link is down. This feature is provided as a transmit diagnostic tool.

Note: Auto-negotiation must be disabled to transmit data packets in the absence of link. If auto-negotiation is enabled, the LXT971A Transceiver automatically transmits FLP bursts if the link is down.

Caution: During normal operation, Intel does not recommend setting Register bit 16.14 for 100 Mbps receive functions because receive errors may be generated.

5.7.3.2.3 Carrier Sense

For 100BASE-TX and 100BASE-FX links, a start-of-stream delimiter (SSD) or /J/K symbol pair causes assertion of carrier sense (CRS). An end-of-stream delimiter (ESD) or /T/R symbol pair causes de-assertion of CRS. The PMA layer also de-asserts CRS if IDLE symbols are received without /T/R. However, in this case RX_ER is asserted for one clock cycle when CRS is de-asserted.

Intel does not recommend using CRS for Interframe Gap (IFG) timing for the following reasons:

- CRS de-assertion time is slightly longer than CRS assertion time. As a result, an IFG interval appears somewhat shorter to the MAC than it actually is on the wire.
- CRS de-assertion is not aligned with TX_EN de-assertion on transmit loopbacks in half-duplex mode.

5.7.3.2.4 Receive Data Valid

The LXT971A Transceiver asserts RX_DV to indicate that the received data maps to valid symbols. In 100 Mbps operation, RX_DV is active with the first nibble of preamble.

5.7.3.3 Twisted-Pair Physical Medium Dependent Sublayer

The twisted-pair Physical Medium Dependent (PMD) layer provides signal scrambling and de-scrambling functions, line coding and decoding functions (MLT-3 for 100BASE-TX, Manchester for 10BASE-T), as well as receiving, polarity correction, and baseline wander correction functions.

5.7.3.3.1 Scrambler/Descrambler

The purpose of the scrambler/descrambler is to spread the signal power spectrum and further reduce EMI using an 11-bit, data-independent polynomial. The receiver automatically decodes the polynomial whenever IDLE symbols are received.

Scrambler Seeding. Once the transmit data (or Idle symbols) are properly encoded, they are scrambled to further reduce EMI and to spread the power spectrum using an 11-bit scrambler seed. Five seed bits are determined by the PHY address, and the remaining bits are hard coded in the design.

Scrambler Bypass. The scrambler/de-scrambler can be bypassed by setting Register bit 16.12 = 1. The scrambler is automatically bypassed when the fiber port is enabled. Scrambler bypass is provided for diagnostic and test support.

5.7.3.3.2 Polarity Correction

The 100 Mbps twisted pair signaling is not polarity sensitive. As a result, the polarity status is not a valid status indicator.

5.7.3.3.3 Baseline Wander Correction

The LXT971A Transceiver provides a baseline wander correction function for when the LXT971A Transceiver is under network operating conditions. The MLT3 coding scheme used in 100BASE-TX is by definition “unbalanced”. As a result, the average value of the signal voltage can “wander” significantly over short time intervals (tenths of seconds). This wander can cause receiver errors at long-line lengths (100 meters) in less robust designs. Exact characteristics of the wander are completely data dependent.

The LXT971A Transceiver baseline wander correction characteristics allow the device to recover error-free data while receiving worst-case packets over all cable lengths.

5.7.3.3.4 Programmable Slew Rate Control

The LXT971A Transceiver device supports a programmable slew-rate mechanism whereby one of four pre-selected slew rates can be used. (For details, see Table 62, “Transmit Control Register - Address 30, Hex 1E” on page 104.) The slew-rate mechanism allows the designer to optimize the output waveform to match the characteristics of the magnetics.

Note: For hardware control of the slew rate, use the TxSLEW pins.

5.7.3.4 Fiber PMD Sublayer

The LXT971A Transceiver provides an LVPECL interface for connection to an external 3.3 V or 5 V fiber-optic transceiver. (The external transceiver provides the PMD function for the optical medium.) The LXT971A Transceiver uses a 125 Mbaud NRZI format for the fiber interface and does not support 10BASE-FL applications.

5.8 10 Mbps Operation

The LXT971A Transceiver operates as a standard 10BASE-T transceiver and LXT971A supports standard 10 Mbps functions. During 10BASE-T operation, the LXT971A Transceiver transmits and receives Manchester-encoded data across the network link. When the MAC is not actively transmitting data, the LXT971A Transceiver drives link pulses onto the line.

In 10BASE-T mode, the polynomial scrambler/de-scrambler is inactive. Manchester-encoded signals received from the network are decoded by the LXT971A Transceiver and sent across the MII to the MAC.

Note: The LXT971A Transceiver does not support fiber connections at 10 Mbps.

5.8.1 10BASE-T Preamble Handling

The LXT971A Transceiver offers two options for preamble handling, selected by Register bit 16.5.

- In 10BASE-T mode when Register bit 16.5 = 0, the LXT971A Transceiver strips the entire preamble off of received packets. CRS is asserted coincident with the start of the preamble. RX_DV is held Low for the duration of the preamble. When RX_DV is asserted, the very first two nibbles driven by the LXT971A Transceiver are the SFD “5D” hex followed by the body of the packet.
- In 10BASE-T mode when Register bit 16.5 = 1, the LXT971A Transceiver passes the preamble through the MII and asserts RX_DV and CRS simultaneously. (In 10BASE-T loopback, the LXT971A Transceiver loops back whatever the MAC transmits to it, including the preamble.)

5.8.2 10BASE-T Carrier Sense

For 10BASE-T links, CRS assertion is based on reception of valid preamble, and CRS de-assertion is based on reception of an end-of-frame (EOF) marker. Register bit 16.7 allows CRS de-assertion to be synchronized with RX_DV de-assertion. For details, see Table 55, “Configuration Register - Address 16, Hex 10” on page 97.

5.8.3 10BASE-T Dribble Bits

The LXT971A Transceiver handles dribble bits in all modes. If one to four dribble bits are received, the nibble is passed across the MII, padded with ones if necessary. If five to seven dribble bits are received, the second nibble is not sent to the MII bus.

5.8.4 10BASE-T Link Integrity Test

In 10BASE-T mode, the LXT971A Transceiver always transmits link pulses.

- If the Link Integrity Test function is enabled (the normal configuration), the LXT971A Transceiver monitors the connection for link pulses. Once link pulses are detected, data transmission is enabled and remains enabled as long as either the link pulses or data transmission continue. If the link pulses stop, the data transmission is disabled.
- If the Link Integrity Test function is disabled (which can be done by setting Configuration Register bit 16.14 to ‘1’), the LXT971A Transceiver transmits to the connection regardless of detected link pulses.

5.8.5 Link Failure

Link failure occurs if the Link Integrity Test is enabled and link pulses or packets stop being received. If this condition occurs, the LXT971A Transceiver returns to the auto-negotiation phase if auto-negotiation is enabled. If the Link Integrity Test function is disabled by setting Configuration Register bit 16.14 to ‘1’, the LXT971A Transceiver transmits packets, regardless of link status.

5.8.6 10BASE-T SQE (Heartbeat)

By default, the Signal Quality Error (SQE) or heartbeat function is disabled on the LXT971A Transceiver. To enable this function, set Register bit 16.9 = 1. When this function is enabled, the LXT971A Transceiver asserts its COL output for 5 to 15 bit times (BT) after each packet.

5.8.7 10BASE-T Jabber

If a transmission exceeds the jabber timer, the LXT971A Transceiver disables the transmit and loopback functions. For jabber timing parameters, see Figure 34, “Intel® LXT971A Transceiver 10BASE-T Jabber and Unjabber Timing” on page 82.

The LXT971A Transceiver automatically exits jabber mode after the unjabber time has expired. This function can be disabled by setting Register bit 16.10 = 1.

5.8.8 10BASE-T Polarity Correction

The LXT971A Transceiver automatically detects and corrects for the condition in which the receive signal (TPFIP/N) is inverted. Reversed polarity is detected if eight inverted link pulses, or four inverted end-of-frame (EOF) markers, are received consecutively. If link pulses or data are not received by the maximum receive time-out period (96 to 128 ms), the polarity state is reset to a non-inverted state.

5.9 Monitoring Operations

5.9.1 Monitoring Auto-Negotiation

Auto-negotiation can be monitored as follows:

- Register bit 17.7 is set to ‘1’ once the auto-negotiation process is completed.
- Register bits 1.2 and 17.10 are set to ‘1’ once the link is established.
- Register bits 17.14 and 17.9 can be used to determine the link operating conditions (speed and duplex).

Note: When the LXT971A Transceiver detects incorrect polarity for a 10BASE-T operation, Register bit 17.5 is set to ‘1’.

5.9.2 Monitoring Next Page Exchange

The LXT971A Transceiver offers an Alternate Next Page mode to simplify the next page exchange process. Normally, Register bit 6.1 (Page Received) remains set until read. When Alternate Next Page mode is enabled, Register bit 6.1 is automatically cleared whenever a new negotiation process takes place. This action prevents the user from reading an old value in bit 6.1 and assuming that Registers 5 and 8 (Partner Ability) contain valid information. Additionally, the LXT971A Transceiver uses Register bit 6.5 to indicate when the current received page is the base page. This information is useful for recognizing when next pages must be resent due to a new negotiation process starting. Register bits 6.1 and 6.5 are cleared when read.

5.9.3 LED Functions

The LXT971A Transceiver has these direct LED driver pins: LED1/CFG1, LED2/CFG2, and LED3/CFG3.

On power-up, all the drivers are asserted for approximately 1 second after reset de-asserts. Each LED driver can be programmed using the LED Configuration Register (Table 59, “LED Configuration Register - Address 20, Hex 14” on page 101) to indicate one of the following conditions:

- Collision Condition
- Duplex Mode
- Link Status
- Operating Speed
- Receive Activity
- Transmit Activity

The LED drivers can also be programmed to display various combined status conditions. For example, setting Register bits 20.15:12 to ‘1101’ produces the following combination of Link and Activity indications:

- If Link is down, LED is off. If activity is detected from the MAC, the LED still blinks even if the link is down.
- If Link is up, LED is on.
- If Link is up and activity is detected, the LED blinks at the stretch interval selected by Register bits 20.3:2 and continues to blink as long as activity is present.

For the LXT971A Transceiver, the LED driver pins also provide initial configuration settings. The LED pins are sensitive to polarity and automatically pull up or pull down to configure for either open drain or open collector circuits (10 mA Max current rating) as required by the hardware configuration. For details, see the discussion of “Hardware Configuration Settings” on page 37.

5.9.4 LED Pulse Stretching

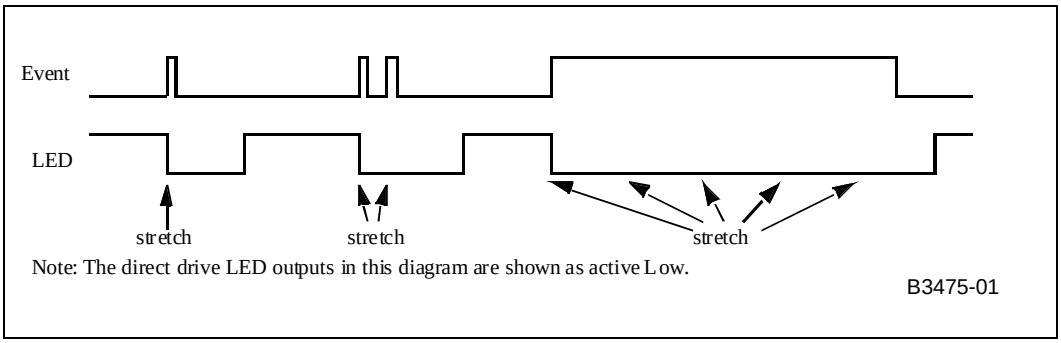
The LED Configuration Register also provides optional LED pulse stretching to 30, 60, or 100 ms. The pulse stretch time is extended further if the event occurs again during this pulse stretch period.

When an event such as receiving a packet occurs, the event is edge detected and it starts the stretch timer. The LED driver remains asserted until the stretch timer expires. If another event occurs before the stretch timer expires, then the stretch timer is reset and the stretch time is extended.

When a long event (such as duplex status) occurs, the event is edge detected and it starts the stretch timer. When the stretch timer expires, the edge detector is reset so that a long event causes another pulse to be generated from the edge detector, which resets the stretch timer and causes the LED driver to remain asserted.

Figure 21 shows how the stretch operation functions.

Figure 21. LED Pulse Stretching



5.10 Boundary Scan (JTAG 1149.1) Functions

The LXT971A Transceiver includes a IEEE 1149.1 boundary scan test port for board level testing. All digital input, output, and input/output pins are accessible.

Note: For the related BSDL file, contact your local sales office or access the Intel website (www.intel.com).

5.10.1 Boundary Scan Interface

The boundary scan interface consists of five pins (TMS, TDI, TDO, TRST_L, and TCK). It includes a state machine, data register array, and instruction register. The TMS and TDI pins are pulled up internally. TCK is pulled down internally. TDO does not have an internal pull-up or pull-down.

5.10.2 State Machine

The TAP controller is a state machine, with 16 states driven by the TCK and TMS pins. Upon reset, the TEST_LOGIC_RESET state is entered. The state machine is also reset when TMS and TDI are high for five TCK periods.

5.10.3 Instruction Register

After the state machine resets, the IDCODE instruction is always invoked. The decode logic ensures the correct data flow to the Data registers according to the current instruction.

Table 15 lists valid JTAG instructions for the LXT971A Transceiver.

Table 15. Valid JTAG Instructions

Name	Code	Description	Mode	Data Register
EXTEST	1111 1111 1110 1000	External Test	Test	BSR
IDCODE	1111 1111 1111 1110	ID Code Inspection	Normal	ID REG
SAMPLE	1111 1111 1111 1000	Sample Boundary	Normal	BSR
HIGHZ	1111 1111 1100 1111	Force Float	Normal	Bypass
CLAMP	1111 1111 1110 1111	Control Boundary to 1/0	Test	Bypass
BYPASS	1111 1111 1111 1111	Bypass Scan	Normal	Bypass

5.10.4 Boundary Scan Register

Each Boundary Scan Register (BSR) cell has two stages. A flip-flop and a latch are used for the serial shift stage and the parallel output stage. Table 16 lists the four BSR modes of operation.

Table 16. BSR Mode of Operation

Mode	Description
1	Capture
2	Shift
3	Update
4	System Function

5.10.5 Device ID Register

Table 17 lists the bits for the Device ID register. For the current version of the JEDEC continuation characters, see the specification update for the LXT971A Transceiver.

Table 17. Device ID Register for Intel® LXT971A Transceiver

Bits 31:28	Bits 27:12	Bits 11:8	Bits 7:1	Bit 0
Version	Part ID (Hex)	JEDEC Continuation Characters	JEDEC ID[1]	Reserved
XXXX	03CB	0000	111 1110	1

1. The JEDEC ID is an 8-bit identifier. The MSB is for parity and is ignored. The Intel JEDEC ID is FE (1111 1110), which becomes 111 1110.

6.0 Application Information

6.1 Magnetics Information

The LXT971A Transceiver requires a 1:1 ratio for both the receive and transmit transformers. The transformer isolation voltage should be rated at 2 kV to protect the circuitry from static voltages across the connectors and cables. For transformer/magnetics requirements, see Table 18.

Note: Before committing to a specific component, contact the manufacturer for current product specifications and validate the magnetics for the specific application.

Table 18. Magnetics Requirements

Parameter	Min	Nom	Max	Units	Test Condition
Rx turns ratio	–	1 : 1	–	–	–
Tx turns ratio	–	1 : 1	–	–	–
Insertion loss	0.0	0.6	1.1	dB	–
Primary inductance	350	–	–	µH	–
Transformer isolation	–	1.5	–	kV	–
Differential to common mode rejection	40	–	–	dB	0.1 to 60 MHz
	35	–	–	dB	60 to 100 MHz
Return Loss	-16	–	–	dB	30 MHz
	-10	–	–	dB	80 MHz

6.2 Typical Twisted-Pair Interface

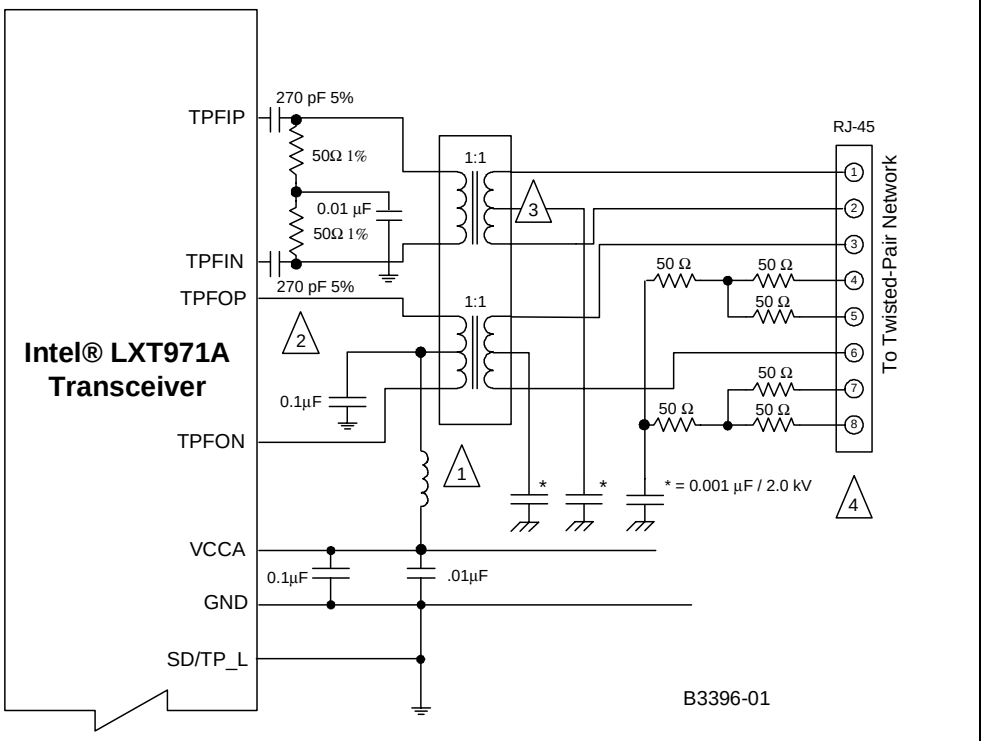
Table 19 provides a comparison of the RJ-45 connections for NIC and Switch applications in a typical twisted-pair interface setting.

Table 19. I/O Pin Comparison of NIC and Switch RJ-45 Setups

Symbol	RJ-45	
	Switch	NIC
TPFIP	1	3
TPFIN	2	6
TPFOP	3	1
TPFON	6	2

Figure 22 shows the LXT971A Transceiver in a typical twisted-pair interface, with the RJ-45 connections crossed over for a Switch configuration.

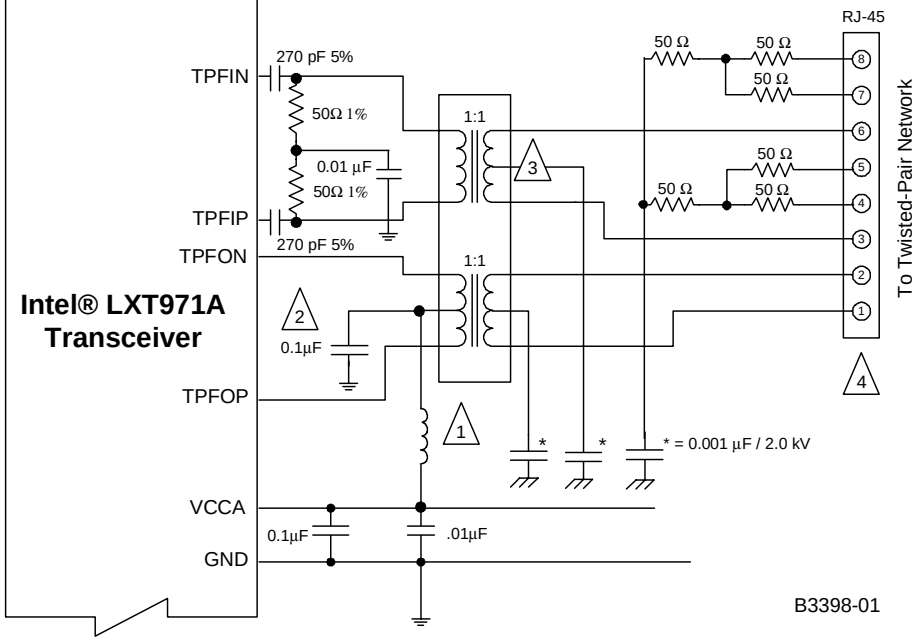
Figure 22. Intel® LXT971A Transceiver Typical Twisted-Pair Interface - Switch



1. Center tap current may be supplied from 3.3 V VCCA as shown. Additional power savings may be realized by supplying the center tap from a 2.5 V current source. A separate ferrite bead (rated at 50 mA) should be used to supply center tap current.
2. The 100 Ω transmit load termination resistor typically required is integrated in the transceiver.
3. Magnetics without a receive pair center-tap do not require a 2 kV termination.
4. RJ-45 connections shown are for a standard switch application. For a standard NIC RJ-45 setup, see Figure 23 on page 64.

Figure 23 shows the LXT971A Transceiver in a typical twisted-pair interface, with the RJ-45 connections configured for a NIC application.

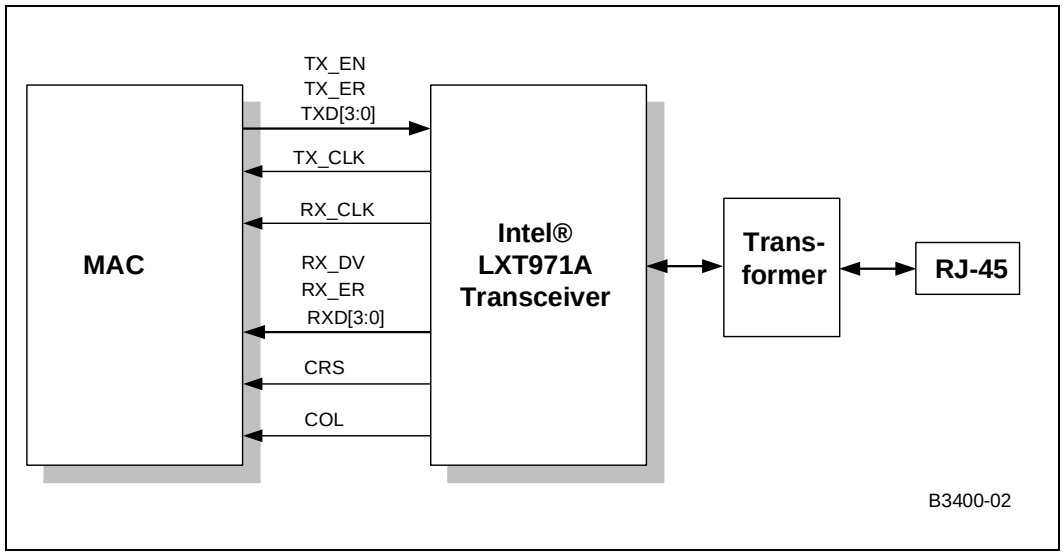
Figure 23. Intel® LXT971A Transceiver Typical Twisted-Pair Interface - NIC



1. Center tap current may be supplied from 3.3 V VCCA as shown. Additional power savings may be realized by supplying the center tap from a 2.5 V current source. A separate ferrite bead (rated at 50 mA) should be used to supply center-tap current.
2. The 100 Ω transmit load termination resistor typically required is integrated in the LXT971A Transceiver.
3. Magnetics without a receive pair center tap do not require a 2 kV termination.
4. RJ-45 connections shown for standard NIC. TX/RX crossover may be required for repeater and switch applications.

Figure 24 show a typical media independent interface (MII) for the LXT971A Transceiver.

Figure 24. Intel® LXT971A Transceiver Typical Media Independent Interface



6.3 Fiber Interface

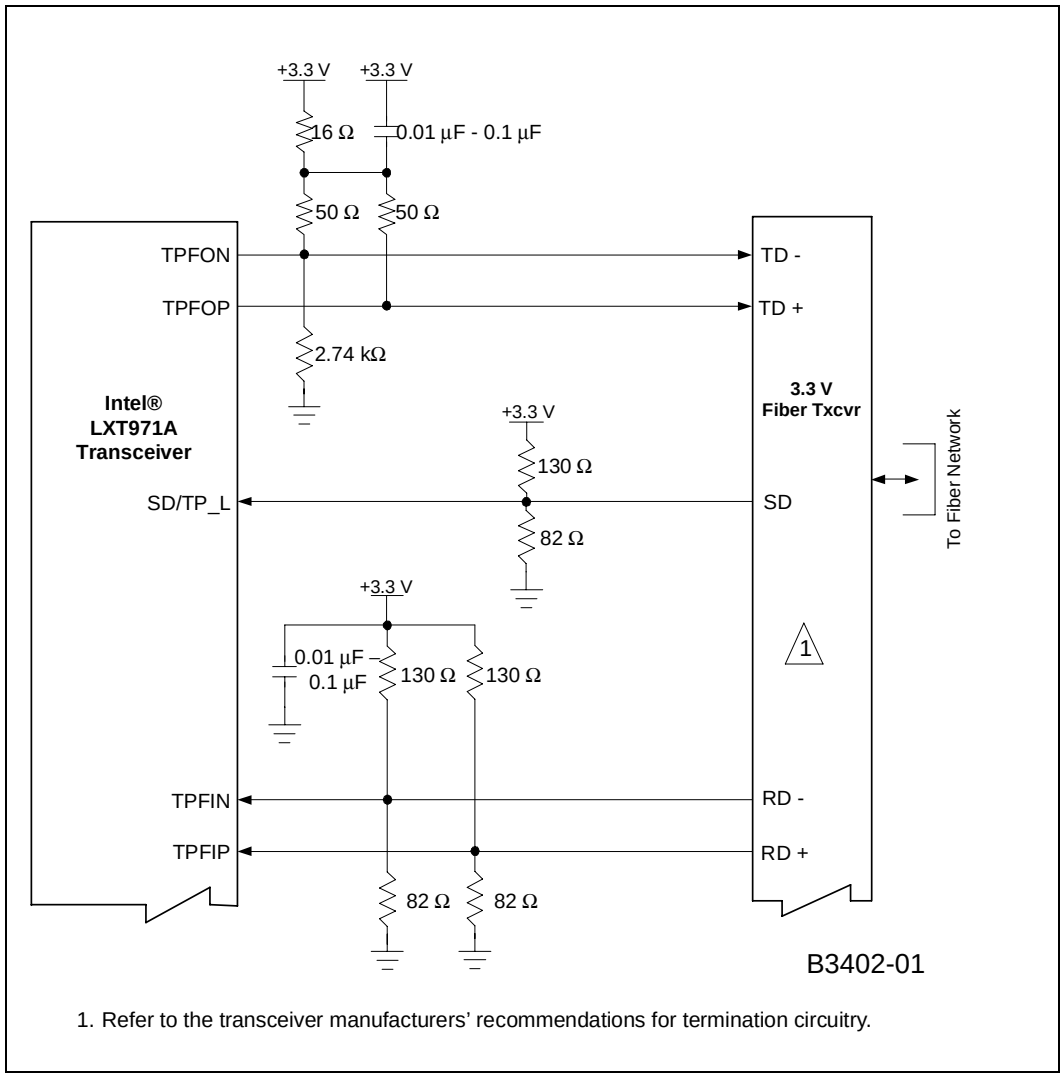
The fiber interface consists of an LVPECL transmit and receive pair to an external fiber-optic transceiver. Both 3.3 V fiber-optic transceivers and 5 V fiber-optic transceivers can be used with the LXT971A Transceiver. For details on fiber interface designs and recommendations for Intel PHYs, see the document on 100BASE-FX fiber optics listed in Chapter 1.0, “Related Documents”.

As shown in Figure 25, the following should occur in 3.3 V fiber transceiver applications:

- The transmit pair should be DC-coupled with the 50 Ω/16 Ω pull-up combination.
- The transmit pair should have a 2.74 kΩ pull-down resistor to prevent PHY-to-fiber transceiver crosstalk amplification in power-down, loopback, and reset states. (See the fiber interface application note.)
- The receive pair should be DC-coupled with an emitter current path for the fiber transceiver.
- The signal detect pin should be DC-coupled with an emitter current path for the fiber transceiver.

Figure 25 shows a typical example of an interface between the LXT971A Transceiver and a 3.3 V fiber transceiver.

Figure 25. Typical Interface - Intel® LXT971ATransceiver to 3.3 V Fiber Transceiver



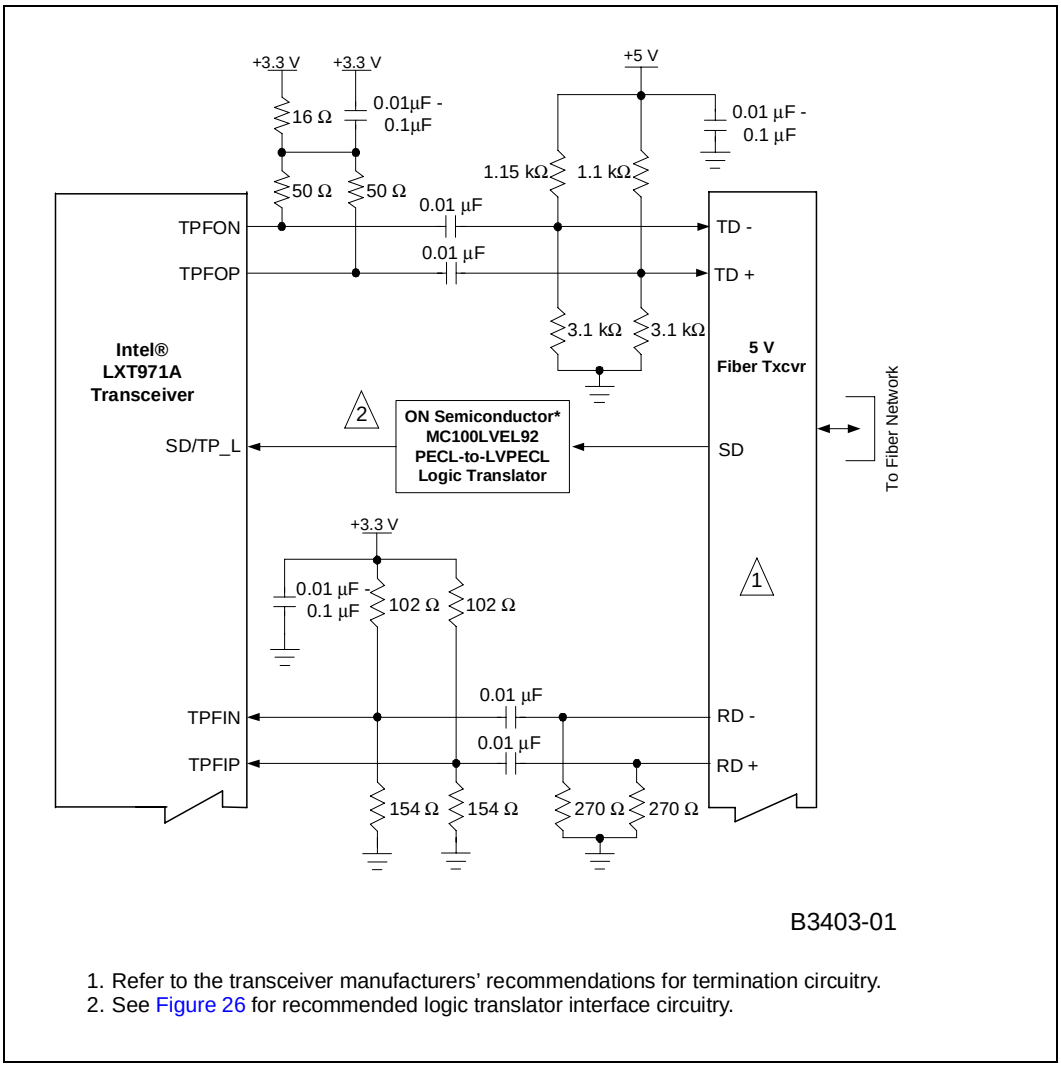
1. Refer to the transceiver manufacturers' recommendations for termination circuitry.

The following occurs in 5 V fiber transceiver applications as shown in Figure 26:

- The transmit pair should be AC-coupled and re-biased to 5 V PECL input levels.
- The transmit pair should contain a balance offset in the bias resistors to prevent PHY-to-fiber transceiver crosstalk amplification in power-down, loopback, and reset states. (See the fiber interface application note.)
- The receive pair should be AC-coupled with an emitter current path for the fiber transceiver and re-biased to 3.3 V LVPECL input levels.
- The signal detect pin on a 5 V fiber transceiver interface should use the logic translator circuitry as shown in Figure 26.

Figure 26 shows a typical example of an interface between the LXT971A Transceiver and a 5 V fiber transceiver.

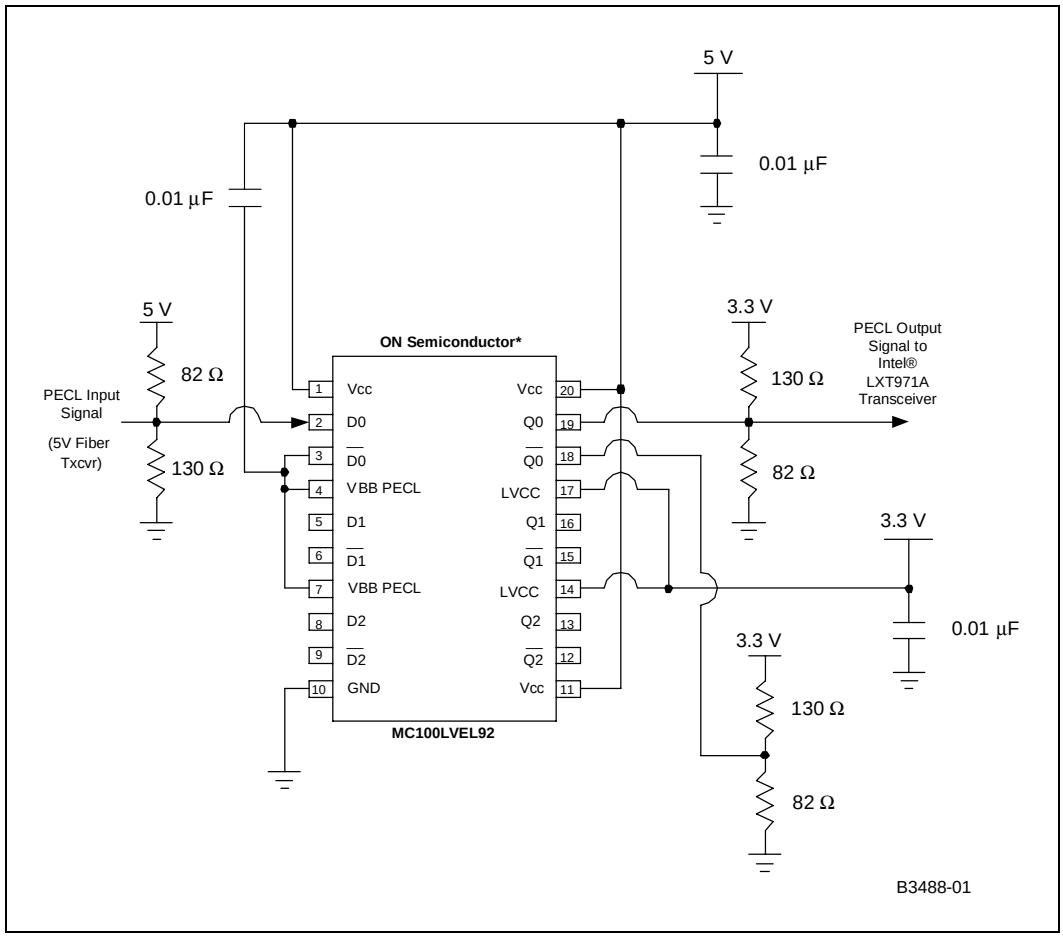
Figure 26. Typical Interface - Intel® LXT971A Transceiver to 5 V Fiber Transceiver



1. Refer to the transceiver manufacturers' recommendations for termination circuitry.
2. See Figure 26 for recommended logic translator interface circuitry.

Figure 27 (a close-up view of Figure 26) shows typical interface between the LXT971A Transceiver and a PECL-to-PECL logic translator.

Figure 27. Typical Interface - Intel® LXT971A Transceiver to Triple PECL-to-PECL Logic Translator



7.0 Electrical Specifications

This chapter includes test specifications for the LXT971A Transceiver. These specifications are guaranteed by test except where noted “by design”.

- Table 20 lists the absolute maximum ratings.
- Table 21 lists the recommended operating conditions.
- Table 22 through Table 43 list the minimum and maximum values that apply over the recommended operating conditions specified.

7.1 Electrical Parameters

Table 20 lists absolute maximum ratings for the LXT971A_C (commercial) Transceiver and the LXT971A_E (extended) Transceiver.

Caution:

- Exceeding the absolute maximum rating values may cause permanent damage.
- Functional operation under these conditions is not implied.
- Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 20. Absolute Maximum Ratings for Intel® LXT971A Transceiver

Parameter	Sym	Min	Max	Units
Supply Voltage	VCC	-0.3	4.0	V
Operating temperature LXT971A_C (Commercial)	TOPA	-15	+85	ºC
Operating temperature LXT971A_E (Extended)	TOPA	-55	+100	ºC
Storage Temperature	TST	-65	+150	ºC

Table 21 lists the recommended operating conditions for the LXT971A Transceiver.

Table 21. Recommended Operating Conditions for Intel® LXT971A Transceiver (Sheet 1 of 2)

Parameter	Sym	Min	Typ[1]	Max	Units
Recommended operating temperature - LXT971A_C (Commercial)	TOPA	0	–	70	ºC
Recommended operating temperature - LXT971A_E (Extended)	TOPA	-40	–	85	ºC
Recommended supply voltage[2] - Analog and digital	Vcca, Vccd	3.14	3.3	3.45	V
Recommended supply voltage[2] - I/O	Vccio	2.35	–	3.45	V
VCC current - 100 BASE-TX	ICC	–	92	110	mA
VCC current - 10 BASE-T	ICC	–	66	82	mA
VCC current - 100 BASE-FX	ICC	–	72	95	mA

1. Typical values are at 25 °C and are for design aid only, not guaranteed, and not subject to production testing.
2. Voltages are with respect to ground unless otherwise specified.

Table 21. Recommended Operating Conditions for Intel® LXT971A Transceiver (Sheet 2 of 2)

Parameter	Sym	Min	Typ[1]	Max	Units
Sleep Mode	Icc	–	40	45	mA
Hard Power Down	Icc	–	–	1	mA
Soft Power Down	Icc	–	51	–	mA
Auto-Negotiation	Icc	–	90	110	mA

1. Typical values are at 25 °C and are for design aid only, not guaranteed, and not subject to production testing.
2. Voltages are with respect to ground unless otherwise specified.

Table 22 lists digital I/O characteristics for all pins except the MII, XI/XO, and LED/CFG pins.

Table 22. Digital I/O Characteristics (Except for MII, XI/XO, and LED/CFG Pins)

Parameter	Sym	Min	Typ[2]	Max	Units	Test Conditions
Input Low voltage	V_{IL}	–	–	0.8	V	–
Input High voltage	V_{IH}	2.0	–	–	V	–
Input current	I_I	-10	–	10	µA	$0.0 < V_I < V_{CC}$
Output Low voltage	V_{OL}	–	–	0.4	V	I_{OL} = 4 mA
Output High voltage	V_{OH}	2.4	–	–	V	I_{OH} = -4 mA

1. Typical values are at 25 °C and are for design aid only, not guaranteed, and not subject to production testing.

Table 23 lists digital I/O characteristics for the MII pins.

Table 23. Digital I/O Characteristics[1] - MII Pins

Parameter	Sym	Min	Typ[2]	Max	Units	Test Conditions
Input Low voltage	V_{IL}	–	–	0.8	V	–
Input High voltage	V_{IH}	2.0	–	–	V	–
Input current	I_I	-10	–	10	µA	$0.0 < V_I <$ VCCIO
Output Low voltage	V_{OL}	–	–	0.4	V	I_{OL} = 4 mA
Output High voltage	V_{OH}	2.2	–	–	V	I_{OH} = -4 mA, VCCIO = 3.3 V
	V_{OH}	2.0	–	–	V	I_{OH} = -4 mA, VCCIO = 2.5 V
Driver output resistance (Line driver output enabled)	R_O[3]	–	100	–	Ω	VCCIO = 2.5 V
	R_O[3]	–	100	–	Ω	VCCIO = 3.3 V

1. MII digital I/O pins are tolerant to 5 V inputs.
2. Typical values are at 25 °C and are for design aid only, not guaranteed, and not subject to production testing.
3. Parameter is guaranteed by design and not subject to production testing.

Table 24 lists the I/O characteristics for the REFCLK/XI and XO pins.

Table 24. I/O Characteristics - REFCLK/XI and XO Pins

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Low Voltage	V_{IL}	–	–	0.8	V	–
Input High Voltage	V_{IH}	2.0	–	–	V	–
Input Clock Frequency Tolerance[2]	Δf	–	–	±100	ppm	–
Input Clock Duty Cycle[2]	Tdc	35	–	65	%	–
Input Capacitance	C_{IN}	–	3.0	–	pF	–

1. Typical values are at 25 °C and are for design aid only, not guaranteed, and not subject to production testing.
2. Parameter is guaranteed by design and not subject to production testing.

Table 25 lists the I/O characteristics for the LXT971A Transceiver LED/CFG pins.

Table 25. I/O Characteristics - LED/CFG Pins

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Input Low Voltage	V_{IL}	–	–	0.8	V	–
Input High Voltage	V_{IH}	2.0	–	–	V	–
Input Current	I_I	-10	–	10	µA	$0 < V_I < VCCIO$
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{OL} = 10 mA
Output High Voltage	V_{OH}	2.0	–	–	V	I_{OH} = -10 mA

Table 26 lists the I/O characteristics for the SD/TP_L pin.

Table 26. I/O Characteristics – SD/TP_L Pin

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Reset and Power-Up States – FX/TP Mode Configuration						
Fiber Mode (Register bit 16.0 = 1)	V_{FX}	600	1600-2400	–	mV	–
Twisted-Pair Mode (Register bit 16.0 = 0)	V_{TP}	–	GND	500	mV	–
100BASE-FX Mode Normal Operation – SD Input from Fiber Transceiver						
Input Low Voltage	V_{IL}	1.49	1.6	1.83	V	VCCD = 3.3 V
Input High Voltage	V_{IH}	2.14	2.4	2.42	V	VCCD = 3.3 V

1. Typical values are for design aid only, not guaranteed, and not subject to production testing.

Table 27 lists the 100BASE-TX characteristics.

Table 27. 100BASE-TX Transceiver Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Peak differential output voltage	VP	0.95	–	1.05	V	Note 2
Signal amplitude symmetry	Vss	98	–	102	%	Note 2
Signal rise/fall time	TRF	3.0	–	5.0	ns	Note 2
Rise/fall time symmetry	TRFS	–	–	0.5	ns	Note 2
Duty cycle distortion	DCD	35	50	65	%	Offset from 16 ns pulse width at 50% of pulse peak
Overshoot/Undershoot	VOS	–	–	5	%	–
Jitter (measured differentially)	–	–	–	1.4	ns	–

1. Typical values are at 25 °C and are for design aid only, not guaranteed, and not subject to production testing.
2. Measured at the line side of the transformer, line replaced by 100 Ω(+/-1%) resistor.

Table 28 lists the 100BASE-FX characteristics.

Table 28. 100BASE-FX Transceiver Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Transmitter						
Peak differential output voltage (single ended)	VOP	0.6	–	1.5	V	–
Signal rise/fall time	TRF	–	–	1.9	ns	10 <–> 90% 2.0 pF load
Jitter (measured differentially)	–	–	–	1.3	ns	–
Receiver						
Peak differential input voltage	VIP	0.55	–	1.5	V	–
Common mode input range	VCMIR	–	–	VCC - 0.7	V	–

1. Typical values are at 25 °C and are for design aid only, not guaranteed, and not subject to production testing.

Table 29 lists the 10BASE-T characteristics.

Table 29. 10BASE-T Transceiver Characteristics (Sheet 1 of 2)

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Transmitter						
Peak differential output voltage	VOP	2.2	2.5	2.8	V	With transformer, line replaced by 100 Ω resistor
Transition timing jitter added by the MAU and PLS sections	–	0	2	11	ns	After line model specified by IEEE 802.3 for 10BASE-T MAU

Table 29. 10BASE-T Transceiver Characteristics (Sheet 2 of 2)

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Receiver						
Receive Input Impedance	Z_{IN}	–	–	22	kΩ	–
Differential Squelch Threshold	V_{DS}	300	420	585	mV	–

Table 30 lists the 10BASE-T link integrity timing characteristics.

Table 30. 10BASE-T Link Integrity Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Time Link Loss Receive	T_{LL}	50	–	150	ms	–
Link Pulse	T_{LP}	2	–	7	Link Pulses	–
Link Min Receive Timer	$T_{LR\ MIN}$	2	–	7	ms	–
Link Max Receive Timer	$T_{LR\ MAX}$	50	–	150	ms	–
Link Transmit Period	Tlt	8	–	24	ms	–
Link Pulse Width	Tlpw	60	–	150	ns	–

1. Typical values are at 25 °C and are for design aid only, not guaranteed, and not subject to production testing.

Table 31 lists the thermal characteristics.

Table 31. Intel® LXT971A Transceiver Thermal Characteristics

Parameter	LXT971A Transceiver	LXT971ALE Transceiver	LXT971ABE Transceiver
Package	1 0x 10 x1.4 64 LD LQFP	10 x 10 x 1.4 64 LQFP	7 x 7 x .96 64 BGA-CSP
Theta-JA	58 C/W	56 C/W	42 C/W
Theta-JC	27 C/W	25 C/W	20 C/W
Psi - JT	3.4 C/W	3.0 C/W	–

7.2 Timing Diagrams

Figure 28. Intel® LXT971A Transceiver 100BASE-TX Receive Timing - 4B Mode

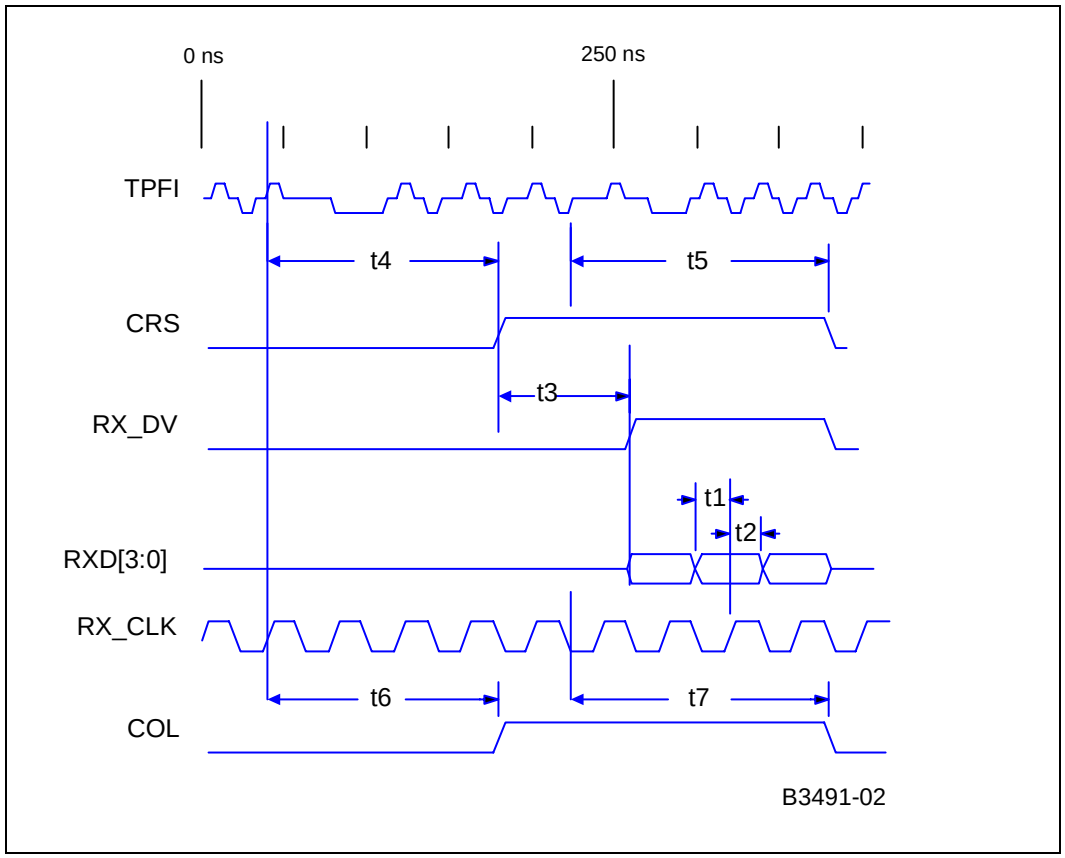


Table 32. Intel® LXT971A Transceiver 100BASE-TX Receive Timing Parameters - 4B Mode

Parameter	Sym	Min	Typ[1]	Max	Units[2]	Test Conditions
RXD[3:0], RX_DV, RX_ER[3] setup to RX_CLK High	t1	10	–	–	ns	–
RXD[3:0], RX_DV, RX_ER hold from RX_CLK High	t2	10	–	–	ns	–
CRS asserted to RXD[3:0], RX_DV	t3	3	–	5	BT	–
Receive start of “J” to CRS asserted	t4	12	–	16	BT	–
Receive start of “T” to CRS de-asserted	t5	10	–	17	BT	–
Receive start of “J” to COL asserted	t6	16	–	22	BT	–
Receive start of “T” to COL de-asserted	t7	17	–	20	BT	–

1. Typical values are at 25 °C and are for design aid only, not guaranteed, and not subject to production testing.
2. BT (Bit Time) is the duration of one bit as transferred to and from the MAC and is the reciprocal of the bit rate. 100BASE-T bit time = 10^{-8} s or 10 ns.
3. RX_ER is not shown in the figure.

Figure 29. Intel® LXT971A Transceiver 100BASE-TX Transmit Timing - 4B Mode

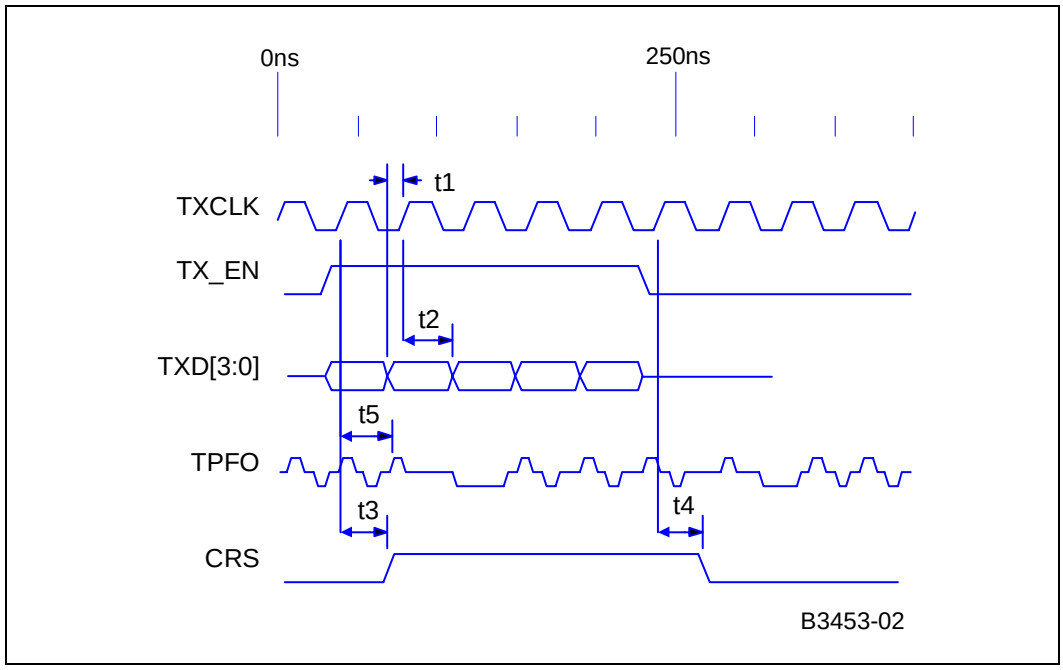


Table 33. Intel® LXT971A Transceiver 100BASE-TX Transmit Timing Parameters - 4B Mode

Parameter	Symbol	Min	Typ[1]	Max	Units[2]	Test Conditions
TXD[3:0], TX_EN, TX_ER[3] setup to TX_CLK High	t1	12	–	–	ns	–
TXD[3:0], TX_EN, TX_ER hold from TX_CLK High	t2	0	–	–	ns	–
TX_EN sampled to CRS asserted	t3	20	–	24	BT	–
TX_EN sampled to CRS de-asserted	t4	24	–	28	BT	–
TX_EN sampled to TPFO out (Tx latency)	t5	5.3	–	5.7	BT	–

1. Typical values are at 25 °C and are for design aid only, not guaranteed, and not subject to production testing.
2. BT (Bit Time) is the duration of one bit as transferred to and from the MAC and is the reciprocal of the bit rate. 100BASE-T bit time = 10^{-8} s or 10 ns.
3. TX_ER is not shown in the figure.

Figure 30. Intel® LXT971A Transceiver 100BASE-FX Receive Timing

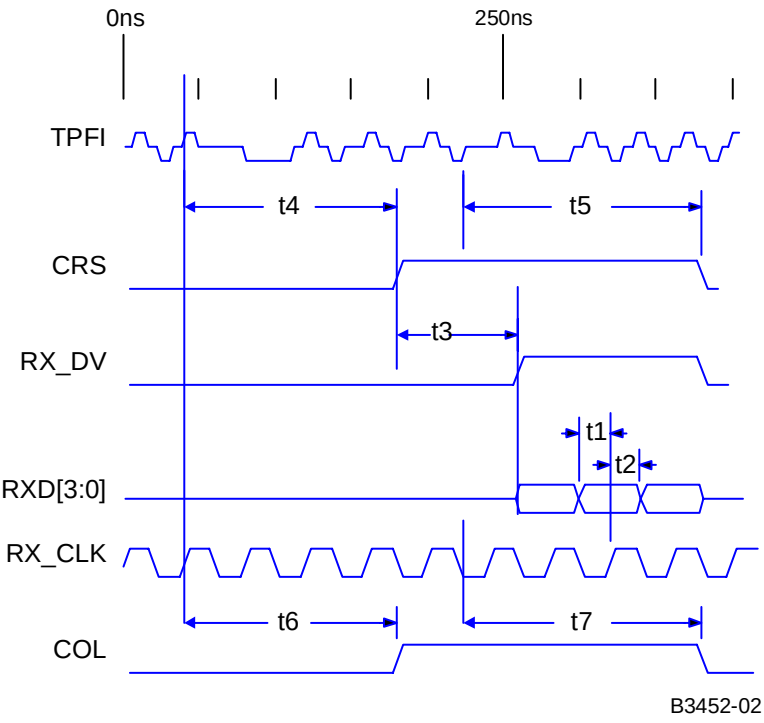


Table 34. Intel® LXT971A Transceiver 100BASE-FX Receive Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units[2]	Test Conditions
RXD[3:0], RX_DV, set up to RX_CLK High	t1	10	–	–	ns	–
RXD[3:0], RX_DV, RX_ER[3] hold from RX_CLK High	t2	10	–	–	ns	–
CRS asserted to RXD[3:0], RX_DV	t3	3	–	5	BT	–
Receive start of "J" to CRS asserted	t4	12	–	16	BT	–
Receive start of "T" to CRS de-asserted	t5	16	–	22	BT	–
Receive start of "J" to COL asserted	t6	10	–	15	BT	–
Receive start of "T" to COL de-asserted	t7	14	–	18	BT	–

1. Typical values are at 25 °C and are for design aid only, not guaranteed, and not subject to production testing.
2. BT (Bit Time) is the duration of one bit as transferred to and from the MAC and is the reciprocal of the bit rate. 100BASE-T bit time = 10^{-8} s or 10 ns.
3. The RX_ER signal is not shown in the figure.

Figure 31. Intel® LXT971A Transceiver 100BASE-FX Transmit Timing

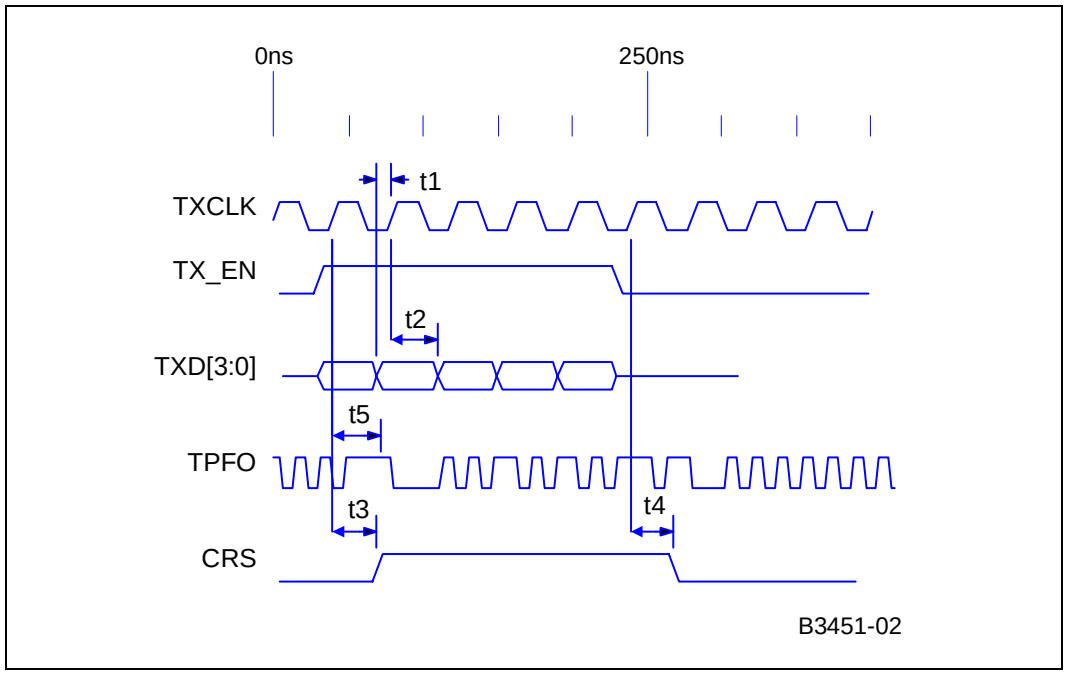


Table 35. Intel® LXT971A Transceiver 100BASE-FX Transmit Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units[2]	Test Conditions
TXD[3:0], TX_EN, TX_ER[3] setup to TX_CLK High	t1	12	–	–	ns	–
TXD[3:0], TX_EN, TX_ER hold from TX_CLK High	t2	0	–	–	ns	–
TX_EN sampled to CRS asserted	t3	17	–	20	BT	–
TX_EN sampled to CRS de-asserted	t4	22	–	24	BT	–
TX_EN sampled to TPFO out (Tx latency)	t5	5	–	5.3	BT	–

1. Typical values are at 25 °C and are for design aid only, not guaranteed, and not subject to production testing.
2. BT (Bit Time) is the duration of one bit as transferred to and from the MAC and is the reciprocal of the bit rate. 100BASE-T bit time = 10^{-8} s or 10 ns.
3. The TX_ER signal is not shown in the figure.

Figure 32. Intel® LXT971A Transceiver 10BASE-T Receive Timing

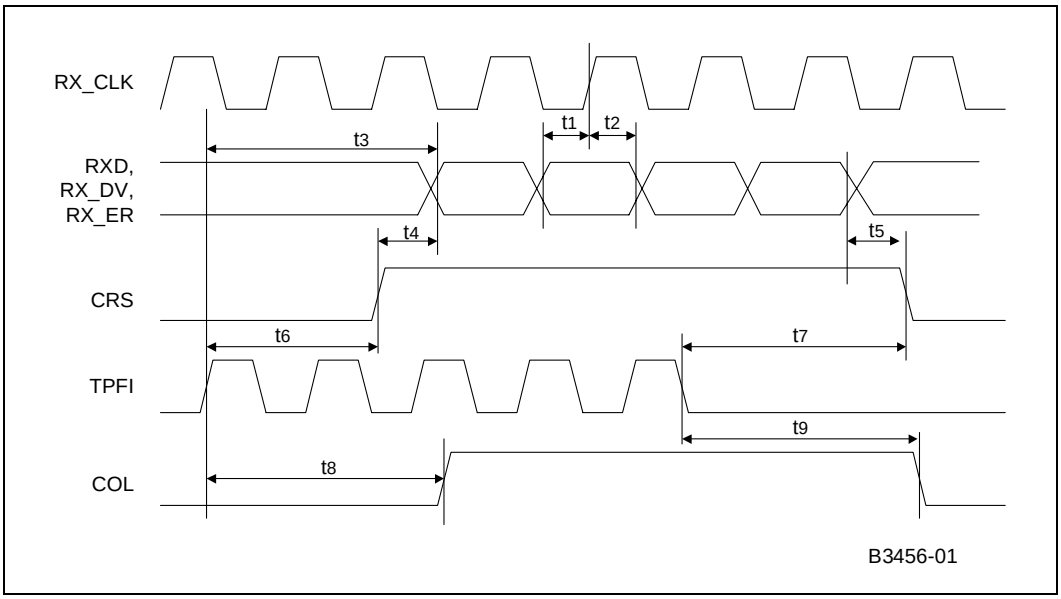


Table 36. Intel® LXT971A Transceiver 10BASE-T Receive Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units[2]	Test Conditions
RXD, RX_DV, RX_ER Setup to RX_CLK High	t1	10	–	–	ns	–
RXD, RX_DV, RX_ER Hold from RX_CLK High	t2	10	–	–	ns	–
TPFIP/N in to RXD out (Rx latency)	t3	4.2	–	6.6	BT	–
CRS asserted to RXD, RX_DV, RX_ER asserted	t4	5	–	32	BT	–
RXD, RX_DV, RX_ER de-asserted to CRS de-asserted	t5	0.3	–	0.5	BT	–
TPFI in to CRS asserted	t6	2	–	28	BT	–
TPFI quiet to CRS de-asserted	t7	6	–	10	BT	–
TPFI in to COL asserted	t8	1	–	31	BT	–
TPFI quiet to COL de-asserted	t9	5	–	10	BT	–

1. Typical values are at 25 °C and are for design aid only, not guaranteed, and not subject to production testing.
2. BT (Bit Time) is the duration of one bit as transferred to and from the MAC and is the reciprocal of the bit rate. 10BASE-T bit time = 10^{-7} s or 100 ns.

Figure 33. Intel® LXT971A Transceiver 10BASE-T Transmit Timing

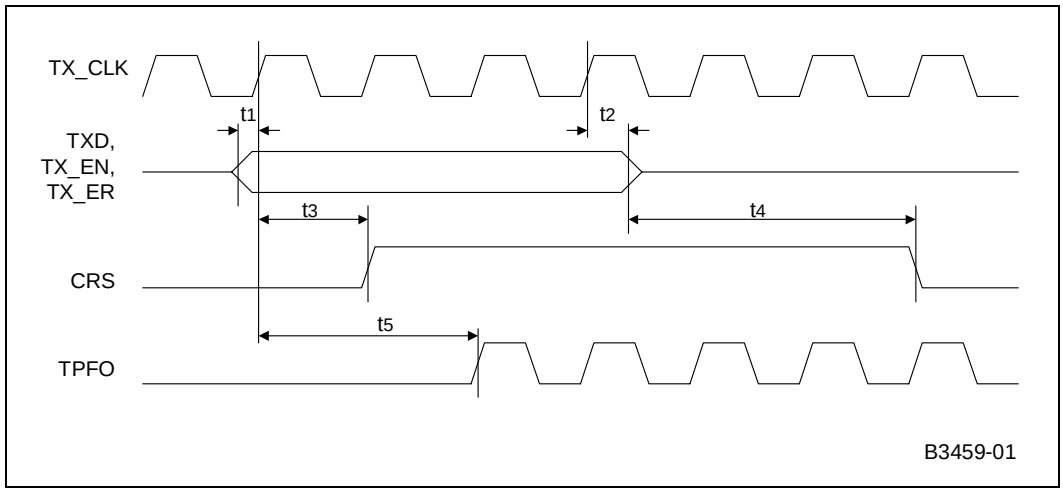


Table 37. Intel® LXT971A Transceiver 10BASE-T Transmit Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units[2]	Test Conditions
TXD, TX_EN, TX_ER setup to TX_CLK High	t1	10	–	–	ns	–
TXD, TX_EN, TX_ER hold from TX_CLK High	t2	0	–	–	ns	–
TX_EN sampled to CRS asserted	t3	–	2	–	BT	–
TX_EN sampled to CRS de-asserted	t4	–	1	–	BT	–
TX_EN sampled to TPFO out (Tx latency)	t5	–	72.5	–	BT	–

1. Typical values are at 25 °C and are for design aid only, not guaranteed, and not subject to production testing.
2. BT (Bit Time) is the duration of one bit as transferred to and from the MAC and is the reciprocal of the bit rate. 10BASE-T bit time = 10^{-7} s or 100 ns.

Figure 34. Intel® LXT971A Transceiver 10BASE-T Jabber and Unjabber Timing

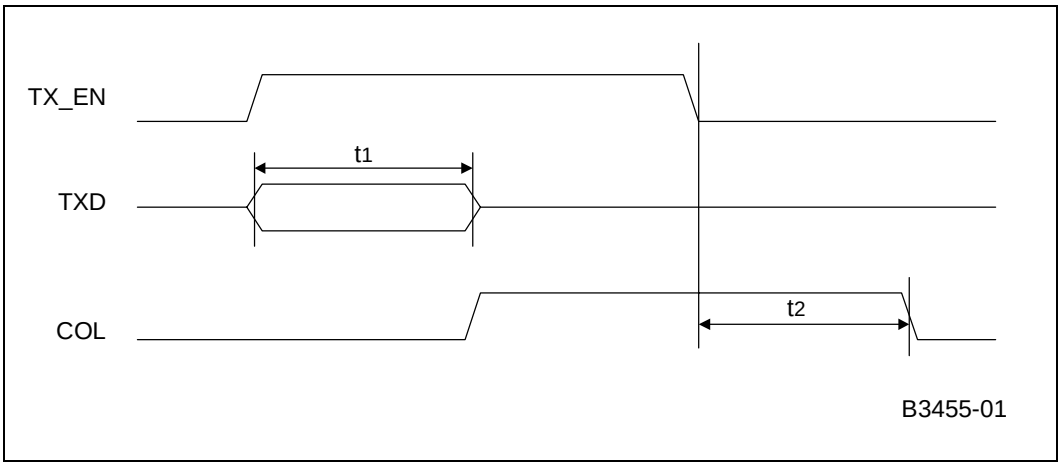


Table 38. Intel® LXT971A Transceiver 10BASE-T Jabber and Unjabber Timing

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Maximum transmit time	t1	20	–	150	ms	–
Unjabber time	t2	250	–	750	ms	–

1. Typical values are at 25 °C and are for design aid only, not guaranteed, and not subject to production testing.

Figure 35. Intel® LXT971A Transceiver 10BASE-T SQE (Heartbeat) Timing

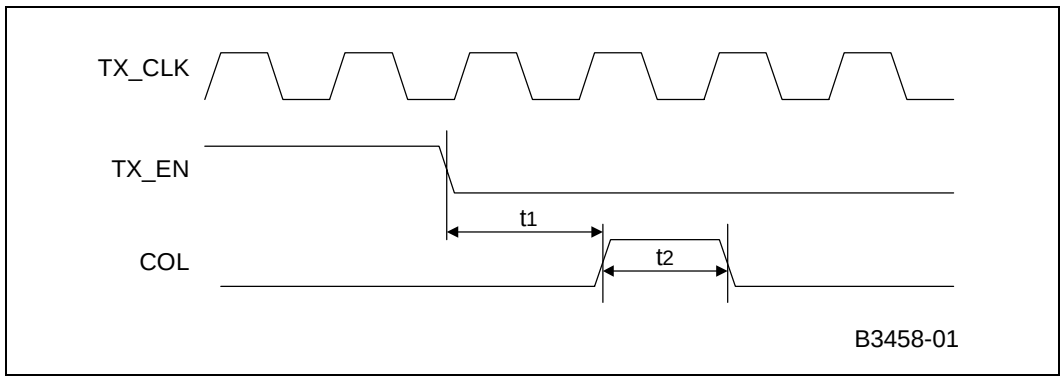


Table 39. Intel® LXT971A Transceiver 10BASE-T SQE (Heartbeat) Timing

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
COL (SQE) Delay after TX_EN off	t1	0.65	–	1.6	us	–
COL (SQE) Pulse duration	t2	0.5	–	1.5	us	–

1. Typical values are at 25 °C and are for design aid only, not guaranteed, and not subject to production testing.

Figure 36. Intel® LXT971A Transceiver Auto-Negotiation and Fast Link Pulse Timing

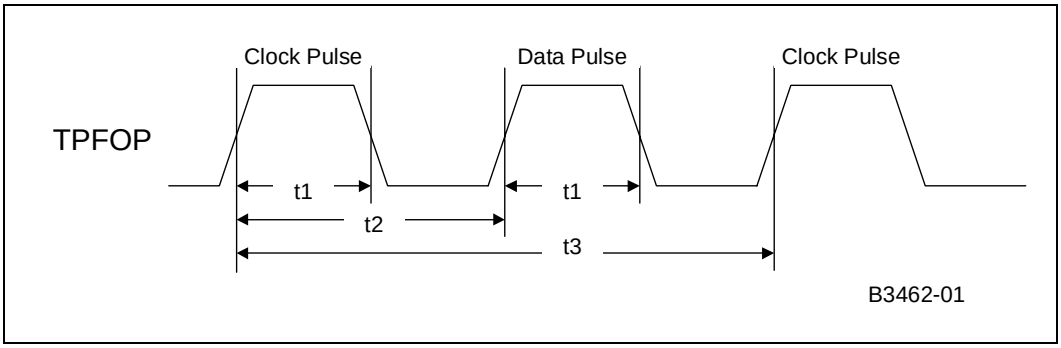


Figure 37. Intel® LXT971A Transceiver Fast Link Pulse Timing

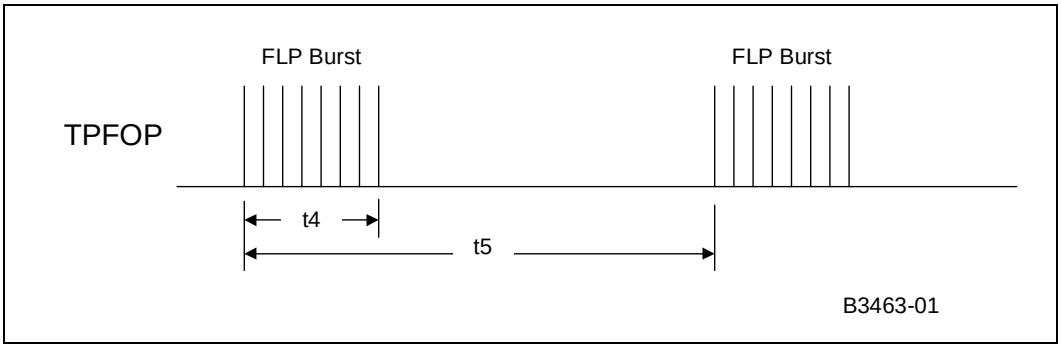


Table 40. Intel® LXT971A Transceiver Auto-Negotiation and Fast Link Pulse Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Clock/Data pulse width	t1	–	100	–	ns	–
Clock pulse to Data pulse	t2	55.5	–	63.8	µs	–
Clock pulse to Clock pulse	t3	123	–	127	µs	–
FLP burst width	t4	–	2	–	ms	–
FLP burst to FLP burst	t5	8	12	24	ms	–
Clock/Data pulses per burst	–	17	–	33	Each clock pulse or data pulse	–

1. Typical values are at 25 °C and are for design aid only, not guaranteed, and not subject to production testing.

Figure 38. Intel® LXT971A Transceiver MDIO Input Timing

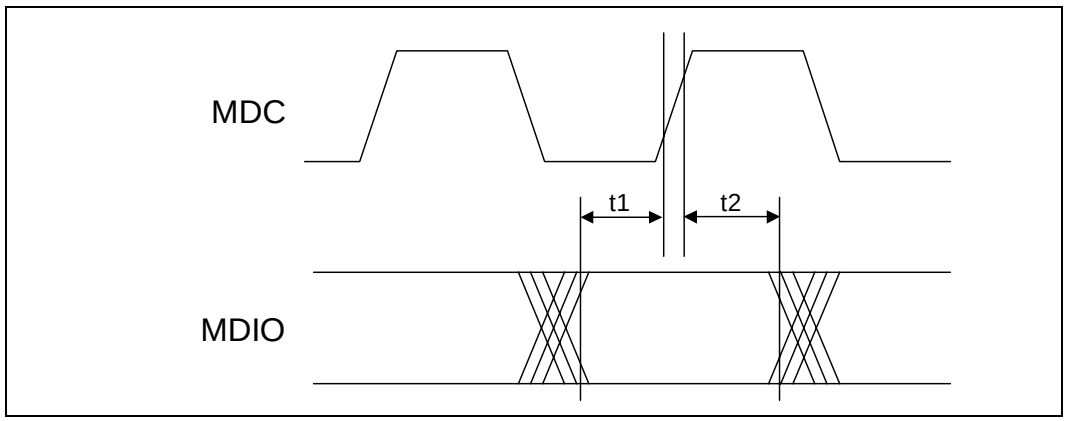


Figure 39. Intel® LXT971A Transceiver MDIO Output Timing

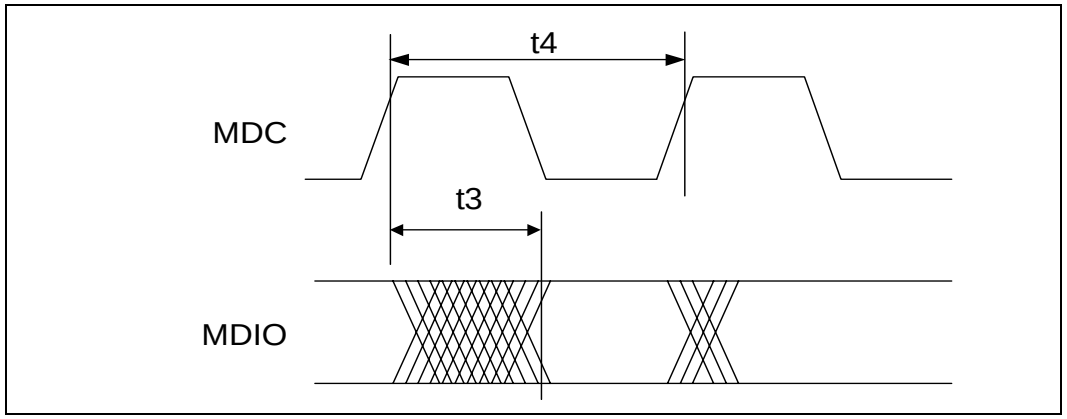


Table 41. Intel® LXT971A Transceiver MDIO Timing

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
MDIO setup before MDC, sourced by STA	t1	10	–	–	ns	–
MDIO hold after MDC, sourced by STA	t2	5	–	–	ns	–
MDC to MDIO output delay, sourced by PHY	t3	–	–	150	ns	–
MDC period	t4	125	–	–	ns	MDC = 8 MHz

1. Typical values are at 25° C and are for design aid only, not guaranteed, and not subject to production testing.

Figure 40. Intel® LXT971A Transceiver Power-Up Timing

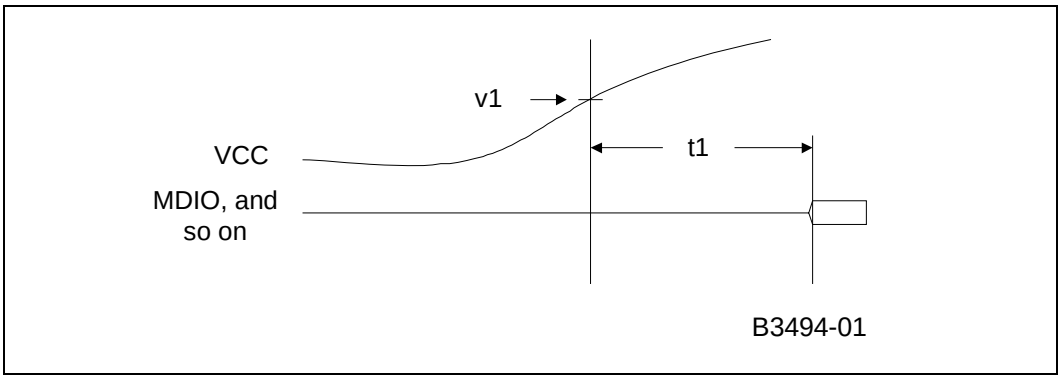


Table 42. Intel® LXT971A Transceiver Power-Up Timing

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Voltage threshold	v1	–	2.9	–	V	–
Power Up delay[2]	t1	–	–	300	µs	–

1. Typical values are at 25° C and are for design aid only, not guaranteed, and not subject to production testing.
2. Power-up delay is specified as a maximum value because it refers to the PHY guaranteed performance. The PHY comes out of reset after a delay of no more than 300 µs. System designers should consider this value as a minimum value. After threshold v1 is reached, the MAC should delay no less than 300 µs before accessing the MDIO port.

Figure 41. Intel® LXT971A Transceiver RESET_L Pulse Width and Recovery Timing

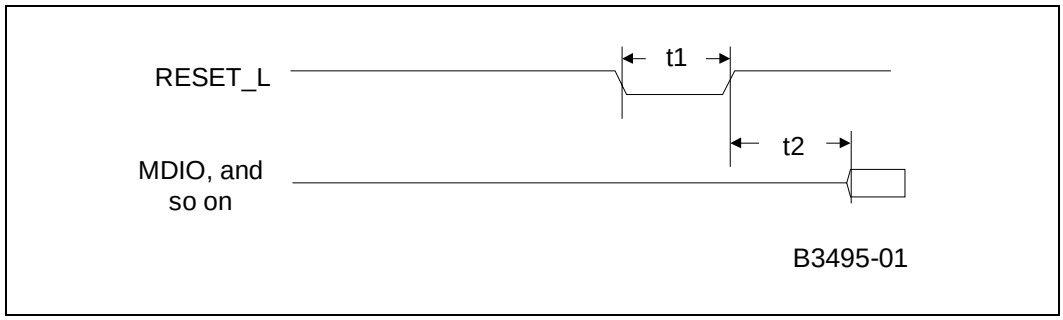


Table 43. Intel® LXT971A Transceiver RESET_L Pulse Width and Recovery Timing

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
RESET_L pulse width	t1	10	–	–	ns	–
RESET_L recovery delay[2]	t2	–		300	µs	–

1. Typical values are at 25° C and are for design aid only, not guaranteed, and not subject to production testing.
2. Reset Recovery Delay is specified as a maximum value because it refers to the PHY guaranteed performance. The PHY comes out of reset after a delay of no more than 300 µs. System designers should consider this value as a minimum value. After de-asserting RESET_L, the MAC should delay no less than 300 µs before accessing the MDIO port.

8.0 Register Definitions - IEEE Base Registers

This chapter includes definitions for the IEEE base registers used by the LXT971A Transceiver. Chapter 9.0, "Register Definitions - Product-Specific Registers" includes definitions of additional product-specific LXT971A Transceiver registers, which are defined in accordance with the IEEE 802.3 standard for adding unique device functions.

The LXT971A Transceiver register set has multiple 16-bit registers.

- Table 44 is a register set listing of the IEEE base registers.
- Table 45 through Table 53 provide bit descriptions of the base registers (address 0 through 8), which are defined in accordance with the "Reconciliation Sublayer and Media Independent Interface" and "Physical Layer Link Signaling for 10/100 Mbps Auto-Negotiation" sections of the IEEE 802.3 standard.

Table 44. Register Set for IEEE Base Registers

Address	Register Name	Bit Assignments
0	Control Register	See Table 45
1	Status Register #1	See Table 46.
2	PHY Identification Register 1	See Table 47.
3	PHY Identification Register 2	See Table 48.
4	Auto-Negotiation Advertisement Register	See Table 49
5	Auto-Negotiation Link Partner Base Page Ability Register	See Table 50.
6	Auto-Negotiation Expansion Register	See Table 51.
7	Auto-Negotiation Next Page Transmit Register	See Table 52.
8	Auto-Negotiation Link Partner Next Page Receive Register	See Table 53.
9	1000BASE-T/100BASE-T2 Control Register	Not Implemented
10	1000BASE-T/100BASE-T2 Status Register	Not Implemented
11 to 14	Reserved	Not Implemented
15	Extended Status Register	Not Implemented

Table 45 lists control register bits.

Table 45. Control Register - Address 0, Hex 0 (Sheet 1 of 2)

Bit	Name	Description			Type [1]	Default
0.15	Reset	0 = Normal operation 1 = PHY reset			R/W SC	0
0.14	Loopback	0 = Disable loopback mode 1 = Enable loopback mode			R/W	0
0.13	Speed Selection	0.6	0.13	Speed Selected	R/W	Note 2
		0	0	10 Mbps		
		0	1	100 Mbps		
		1	0	1000 Mbps (not supported)		
		1	1	Reserved		

Table 45. Control Register - Address 0, Hex 0 (Sheet 2 of 2)

Bit	Name	Description	Type [1]	Default
0.12	Auto-Negotiation Enable	0 = Disable auto-negotiation process 1 = Enable auto-negotiation process	R/W	Note 2
0.11	Power-Down	0 = Normal operation 1 = Power-down	R/W	0
0.10	Isolate	0 = Normal operation 1 = Electrically isolate PHY from MII	R/W	0
0.9	Restart Auto-Negotiation	0 = Normal operation 1 = Restart auto-negotiation process	R/W SC	0
0.8	Duplex Mode	0 = Half-duplex 1 = Full-duplex	R/W	Note 2
0.7	Collision Test	0 = Disable COL signal test 1 = Enable COL signal test	R/W	0
0.6	Speed Selection	0.6 / 0.13 / Speed Selected 0 / 0 / 10 Mbps 0 / 1 / 100 Mbps 1 / 0 / 1000 Mbps (not supported) 1 / 1 / Reserved	R/W	0
0.5:0	Reserved	Write as '0'. Ignore on Read.	R/W	00000

1. R/W = Read/Write
   SC = Self Clearing
2. Some bits have their default values determined at reset by hardware configuration pins. For default details for these bits, see Section 5.4.4, "Hardware Configuration Settings".

Table 46 lists MII status register bits.

Table 46. MII Status Register #1 - Address 1, Hex 1 (Sheet 1 of 2)

Bit	Name	Description	Type [1]	Default
1.15	100BASE-T4 Not Supported	0 = PHY not able to perform 100BASE-T4 1 = PHY able to perform 100BASE-T4	RO	0
1.14	100BASE-X Full-Duplex	0 = PHY not able to perform full-duplex 100BASE-X 1 = PHY able to perform full-duplex 100BASE-X	RO	1
1.13	100BASE-X Half-Duplex	0 = PHY not able to perform half-duplex 100BASE-X 1 = PHY able to perform half-duplex 100BASE-X	RO	1
1.12	10 Mbps Full-Duplex	0 = PHY not able to operate at 10 Mbps full-duplex mode 1 = PHY able to operate at 10 Mbps in full-duplex mode	RO	1
1.11	10 Mbps Half-Duplex	0 = PHY not able to operate at 10 Mbps in half-duplex 1 = PHY able to operate at 10 Mbps in half-duplex mode	RO	1
1.10	100BASE-T2 Full-Duplex Not Supported	0 = PHY not able to perform full-duplex 100BASE-T2 1 = PHY able to perform full-duplex 100BASE-T2	RO	0

1. RO = Read Only
   LL = Latching Low
   LH = Latching High

Table 46. MII Status Register #1 - Address 1, Hex 1 (Sheet 2 of 2)

Bit	Name	Description	Type [1]	Default
1.9	100BASE-T2 Half-Duplex Not Supported	0 = PHY not able to perform half-duplex 100BASE-T2 1 = PHY able to perform half-duplex 100BASE-T2	RO	0
1.8	Extended Status	0 = No extended status information in register 15 1 = Extended status information in register 15	RO	0
1.7	Reserved	Ignore when read.	RO	0
1.6	MF Preamble Suppression	0 = PHY cannot accept management frames with preamble suppressed 1 = PHY accepts management frames with preamble suppressed	RO	0
1.5	Auto-Negotiation complete	0 = Auto-negotiation not complete 1 = Auto-negotiation complete	RO	0
1.4	Remote Fault	0 = No remote fault condition detected 1 = Remote fault condition detected	RO/LH	0
1.3	Auto-Negotiation Ability	0 = PHY is not able to perform auto-negotiation 1 = PHY is able to perform auto-negotiation	RO	1
1.2	Link Status	0 = Link is down 1 = Link is up	RO/LL	0
1.1	Jabber Detect	0 = Jabber condition not detected 1 = Jabber condition detected	RO/LH	0
1.0	Extended Capability	0 = Basic register capabilities 1 = Extended register capabilities	RO	1

1. RO = Read Only
   LL = Latching Low
   LH = Latching High

For Table 47 and Table 48, see Figure 42.

Table 47. PHY Identification Register 1 - Address 2, Hex 2

Bit	Name	Description	Type [1]	Default
2.15:0	PHY ID Number	The PHY identifier is composed of bits 3 through 18 of the Organizationally Unique Identifier (OUI).	RO	0013 hex

1. RO = Read Only

Table 48. PHY Identification Register 2 - Address 3, Hex 3 (Sheet 1 of 2)

Bit	Name	Description	Type [1]	Default
3.15:10	PHY ID number	The PHY identifier is composed of bits 19 through 24 of the OUI.	RO	011110

Table 48. PHY Identification Register 2 - Address 3, Hex 3 (Sheet 2 of 2)

Bit	Name	Description	Type [1]	Default
3.9:4	Manufacturer's model number	6 bits containing manufacturer's part number.	RO	001110
3.3:0	Manufacturer's revision number	4 bits containing manufacturer's revision number.	RO	For current revision ID information, see the Specification Update.

1. RO = Read Only

Figure 42. PHY Identifier Bit Mapping

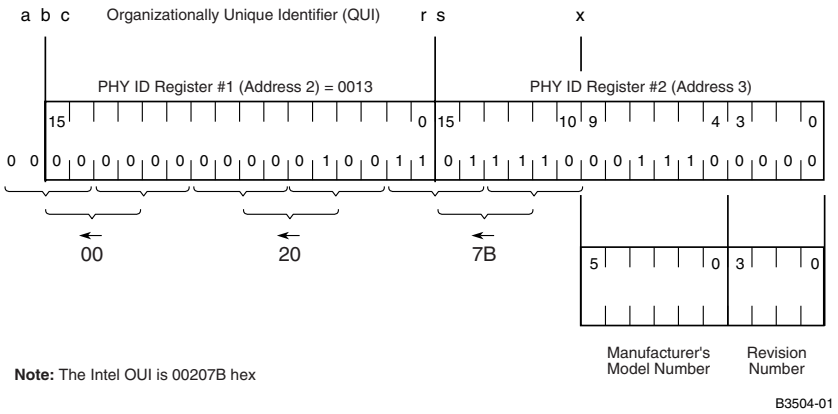


Table 49 lists auto-negotiation advertisement bits.

Table 49. Auto-Negotiation Advertisement Register - Address 4, Hex 4

Bit	Name	Description	Type [1]	Default
4.15	Next Page	0 = Port has no ability to send multiple pages. 1 = Port has ability to send multiple pages.	R/W	0
4.14	Reserved	Ignore when read.	RO	0
4.13	Remote Fault	0 = No remote fault. 1 = Remote fault.	R/W	0
4.12	Reserved	Write as '0'. Ignore on Read.	R/W	0
4.11	Asymmetric Pause	Pause operation defined in IEEE 802.3 Standard, Clause 40 and 27	R/W	0
4.10	Pause	0 = Pause operation disabled. 1 = Pause operation enabled for full-duplex links.	R/W	Note 2
4.9	100BASE-T4	0 = 100BASE-T4 capability is not available. 1 = 100BASE-T4 capability is available. **NOTE:** The LXT971A Transceiver does not support 100BASE-T4 but allows this bit to be set to advertise in the auto-negotiation sequence for 100BASE-T4 operation. An external 100BASE-T4 Transceiver can be switched in if this capability is desired.	R/W	0
4.8	100BASE-TX Full-duplex	0 = Port is not 100BASE-TX full-duplex capable. 1 = Port is 100BASE-TX full-duplex capable.	R/W	Note 3
4.7	100BASE-TX	0 = Port is not 100BASE-TX capable. 1 = Port is 100BASE-TX capable.	R/W	Note 3
4.6	10BASE-T Full-duplex	0 = Port is not 10BASE-T full-duplex capable. 1 = Port is 10BASE-T full-duplex capable.	R/W	Note 3
4.5	10BASE-T	0 = Port is not 10BASE-T capable. 1 = Port is 10BASE-T capable.	R/W	Note 3
4.4:0	Selector Field, S<4:0>	<00001> = IEEE 802.3. <00010> = IEEE 802.9 ISLAN-16T. <00000> = Reserved for future auto-negotiation development. <11111> = Reserved for future auto-negotiation development **NOTE:** Unspecified or reserved combinations must not be transmitted.	R/W	00001

1. R/W = Read/Write
   RO = Read Only
2. Default setting is determined by pin 33/H8 at reset.
3. Some bits have their default values determined at reset by hardware configuration pins. For default details for these bits, see Section 5.4.4, "Hardware Configuration Settings".

Table 50 lists auto-negotiation link partner base page ability bits.

Table 50. Auto-Negotiation Link Partner Base Page Ability Register - Address 5, Hex 5

Bit	Name	Description	Type [1]	Default
5.15	Next Page	0 = Link Partner has no ability to send multiple pages. 1 = Link Partner has ability to send multiple pages.	RO	0
5.14	Acknowledge	0 = Link Partner has not received Link Code Word from the LXT971A Transceiver. 1 = Link Partner has received Link Code Word from the LXT971A Transceiver.	RO	0
5.13	Remote Fault	0 = No remote fault. 1 = Remote fault.	RO	0
5.12	Reserved	Ignore when read.	RO	0
5.11	Asymmetric Pause	Pause operation defined in IEEE 802.3 Standard, Clause 40 and 27. 0 = Link Partner is not Pause capable. 1 = Link Partner is Pause capable.	RO	0
5.10	Pause	0 = Link Partner is not Pause capable. 1 = Link Partner is Pause capable.	RO	0
5.9	100BASE-T4	0 = Link Partner is not 100BASE-T4 capable. 1 = Link Partner is 100BASE-T4 capable.	RO	0
5.8	100BASE-TX Full-Duplex	0 = Link Partner is not 100BASE-TX full-duplex capable. 1 = Link Partner is 100BASE-TX full-duplex capable.	RO	0
5.7	100BASE-TX	0 = Link Partner is not 100BASE-TX capable. 1 = Link Partner is 100BASE-TX capable.	RO	0
5.6	10BASE-T Full-Duplex	0 = Link Partner is not 10BASE-T full-duplex capable. 1 = Link Partner is 10BASE-T full-duplex capable.	RO	0
5.5	10BASE-T	0 = Link Partner is not 10BASE-T capable. 1 = Link Partner is 10BASE-T capable.	RO	0
5.4:0	Selector Field S<4:0>	<00001> = IEEE 802.3. <00010> = IEEE 802.9 ISLAN-16T. <00000> = Reserved for future auto-negotiation development. <11111> = Reserved for future auto-negotiation development. Unspecified or reserved combinations must not be transmitted.	RO	0

1. RO = Read Only

Table 51 lists auto-negotiation expansion bits.

Table 51. Auto-Negotiation Expansion - Address 6, Hex 6

Bit	Name	Description	Type [1]	Default
6.15:6	Reserved	Ignore when read.	RO	0
6.5	Base Page	This bit indicates the status of the auto-negotiation variable base page. It flags synchronization with the auto-negotiation state diagram, allowing detection of interrupted links. This bit is used only if Register bit 16.1 (that is, Alternate NP feature) is set. 0 = Base page = False (base page not received) 1 = Base page = True (base page received)	RO/LH	0
6.4	Parallel Detection Fault	0 = Parallel detection fault has not occurred. 1 = Parallel detection fault has occurred.	RO/LH	0
6.3	Link Partner Next Page Able	0 = Link partner is not next page able. 1 = Link partner is next page able.	RO	0
6.2	Next Page Able	0 = Local device is not next page able. 1 = Local device is next page able.	RO	1
6.1	Page Received	This bit is cleared on Read. If Register bit 16.1 is set, the Page Received bit is also cleared when either mr_page_rx = false or transmit_disable = true. 1 = Indicates a new page is received and the received code word is loaded into Register 5 (Base Pages) or Register 8 (Next Pages) as specified in Clause 28 of IEEE 802.3.	RO/LH	0
6.0	Link Partner A/N Able	0 = Link partner is not auto-negotiation able. 1 = Link partner is auto-negotiation able.	RO	0
1. RO = Read Only LH = Latching High				

Table 52 lists auto-negotiation next page transmit bits.

Table 52. Auto-Negotiation Next Page Transmit Register - Address 7, Hex 7

Bit	Name	Description	Type [1]	Default
7.15	Next Page (NP)	0 = Last page 1 = Additional next pages follow	R/W	0
7.14	Reserved	Ignore when read.	RO	0
7.13	Message Page (MP)	0 = Register bits 7.10:0 are user defined. 1 = Register bits 7.10.0 follow IEEE message page format.	R/W	1
7.12	Acknowledge 2 (ACK2)	0 = Cannot comply with message 1 = Complies with message	R/W	0
7.11	Toggle (T)	0 = Previous value of the transmitted Link Code Word equalled logic one 1 = Previous value of the transmitted Link Code Word equalled logic zero	R/W	0
7.10:0	Message/ Unformatted Code Field	If Register bits 7.13 = 0, Register bits 7.10:0 are user-defined. If Register bits 7.13 = 1, Register bits 7.10:0 follow IEEE message page format.	R/W	00000000001
1. RO = Read Only. R/W = Read/Write				

Table 53 lists auto-negotiation link partner next page receive bits.

Table 53. Auto-Negotiation Link Partner Next Page Receive Register - Address 8, Hex 8

Bit	Name	Description	Type [1]	Default
8.15	Next Page (NP)	0 = Link Partner has no additional next pages to send 1 = Link Partner has additional next pages to send	RO	0
8.14	Acknowledge (ACK)	0 = Link Partner has not received Link Code Word from LXT971A Transceiver. 1 = Link Partner has received Link Code Word from LXT971A Transceiver.	RO	0
8.13	Message Page (MP)	0 = Register bits 8.10:0 are user defined. 1 = Register bits 8.10:0 follow IEEE message page format.	RO	0
8.12	Acknowledge 2 (ACK2)	0 = Link Partner cannot comply with the message 1 = Link Partner complies with the message	RO	0
8.11	Toggle (T)	0 = Previous value of transmitted Link Code Word equal to logic one 1 = Previous value of transmitted Link Code Word equal to logic zero	RO	0
8.10:0	Message/Unformatted Code Field	If Register bit 8.13 = 0, Register bits 18.10:0 are user defined. If Register bit 8.13 = 1, Register bits 18.10:0 follow IEEE message page format.	RO	0000000000
1. RO = Read Only.				

9.0 Register Definitions - Product-Specific Registers

This chapter includes definitions of product-specific LXT971A Transceiver registers that are defined in accordance with the IEEE 802.3 standard for adding unique device functions. (For definitions of the IEEE base registers used by the LXT971A Transceiver, see Chapter 8.0, "Register Definitions - IEEE Base Registers".)

- Table 54 lists the register set of the product-specific registers.
- Table 55 through Table 62 provide bit descriptions of the product-specific registers (address 17 through 30).

Table 54. Register Set for Product-Specific Registers

Address	Register Name	Bit Assignments
16	Port Configuration Register	See Table 55
17	Status Register #2	See Table 56
18	Interrupt Enable Register	See Table 57
19	Status Change Register	See Table 58
20	LED Configuration Register	See Table 59
21	Reserved	
22-25	Reserved	
26	Digital Configuration Register	See Table 60
27	Reserved	
28	Reserved	
29	Reserved	
30	Transmit Control Register	See Table 62
31	Reserved	

Table 55 lists configuration bits.

Table 55. Configuration Register - Address 16, Hex 10

Bit	Name	Description	Type [1]	Default
16.15	Reserved	Write as '0'. Ignore on Read.	R/W	0
16.14	Force Link Pass	0 = Normal operation 1 = Force Link pass	R/W	0
16.13	Transmit Disable	0 = Normal operation 1 = Disable Twisted Pair transmitter	R/W	0
16.12	Bypass Scrambler (100BASE-TX)	0 = Normal operation 1 = Bypass Scrambler and Descrambler	R/W	0
16.11	Reserved	Write as '0'. Ignore on Read.	R/W	0
16.10	Jabber (10BASE-T)	0 = Normal operation 1 = Disable Jabber Correction	R/W	0
16.9	SQE (10BASE-T)	0 = Disable Heart Beat 1 = Enable Heart Beat	R/W	0
16.8	TP Loopback (10BASE-T)	0 = Normal operation 1 = Disable TP loopback during half-duplex operation	R/W	0
16.7	CRS Select (10BASE-T)	0 = Normal Operation 1 = CRS deassert extends to RX_DV deassert	R/W	1
16.6	Sleep Mode	0 = Disable Sleep Mode 1 = Enable Sleep Mode	R/W	Default value is determined by state of SLEEP pin 32/H7.
16.5	PRE_EN	Preamble Enable. 0 = Set RX_DV high coincident with SFD. 1 = Set RX_DV high and RXD = preamble when CRS is asserted. **NOTE:** Preamble is always enabled in 100 Mbps operation.	R/W	0
16.4:3	Sleep Timer	00 = 3.04 seconds 01 = 2.00 seconds 10 = 1.04 seconds	R/W	00
16.2	Fault Code Enable	0 = Disable FEFI transmission 1 = Enable FEFI transmission	R/W	1
16.1	Alternate NP feature	0 = Disable alternate auto negotiate next page feature. 1 = Enable alternate auto negotiate next page feature. This bit enables or disables the register bit 6.5 capability.	R/W	0
16.0	Fiber Select	0 = Select TP mode. 1 = Select fiber mode.	R/W	Default value is determined by state of pin 26/G2 (SD/TP_L).

1. R/W = Read /Write

Table 56 lists register #2 status bits.

Table 56. Status Register #2 - Address 17, Hex 11

Bit	Name	Description	Type [1]	Default
17.15	Reserved	Always 0.	RO	0
17.14	10/100 Mode	0 = LXT971A Transceiver is not operating 100BASE-TX mode. 1 = LXT971A Transceiver is operating in 100BASE-TX mode.	RO	0
17.13	Transmit Status	0 = LXT971A Transceiver is not transmitting a packet. 1 = LXT971A Transceiver is transmitting a packet.	RO	0
17.12	Receive Status	0 = LXT971A Transceiver is not receiving a packet. 1 = LXT971A Transceiver is receiving a packet.	RO	0
17.11	Collision Status	0 = No collision. 1 = Collision is occurring.	RO	0
17.10	Link	0 = Link is down. 1 = Link is up.	RO	0
17.9	Duplex Mode	0 = Half-duplex. 1 = Full-duplex.	RO	0
17.8	Auto-Negotiation	0 = LXT971A Transceiver is in manual mode. 1 = LXT971A Transceiver is in auto-negotiation mode.	RO	0
17.7	Auto-Negotiation Complete	0 = Auto-negotiation process not completed. 1 = Auto-negotiation process completed. This bit is valid only when auto negotiate is enabled. The value is equivalent to the value of Register bit 1.5.	RO	0
17.6	Reserved	Always 0.	RO	0
17.5	Polarity	0 = Polarity is not reversed. 1 = Polarity is reversed. **NOTE:** Polarity is not a valid status in 100 Mbps mode.	RO	0
17.4	Pause	0 = The LXT971A Transceiver is not Pause capable. 1 = The LXT971A Transceiver is Pause capable.	R	0
17:3	Error	0 = No error occurred 1 = Error occurred (Remote Fault, jabber, parallel detect fault) **NOTE:** The register bit is cleared when the registers that generate the error condition are read.	RO	0
17:2	Reserved	Always 0.	RO	0
17:1	Reserved	Always 0.	RO	0
17.0	Reserved	Always 0.	RO	0

1. RO = Read Only. R/W = Read/Write

Table 57 lists interrupt enable bits.

Table 57. Interrupt Enable Register - Address 18, Hex 12

Bit	Name	Description	Type [1]	Default
18.15:9	Reserved	Write as '0'. Ignore on Read.	R/W	N/A
18.8	Reserved	Write as '0'. Ignore on Read.	R/W	0
18.7	ANMSK	Mask for Auto Negotiate Complete 0 = Do not allow event to cause interrupt. 1 = Enable event to cause interrupt.	R/W	0
18.6	SPEEDMSK	Mask for Speed Interrupt 0 = Do not allow event to cause interrupt. 1 = Enable event to cause interrupt.	R/W	0
18.5	DUPLEXMSK	Mask for Duplex Interrupt 0 = Do not allow event to cause interrupt. 1 = Enable event to cause interrupt.	R/W	0
18.4	LINKMSK	Mask for Link Status Interrupt 0 = Do not allow event to cause interrupt. 1 = Enable event to cause interrupt.	R/W	0
18.3	Reserved	Write as '0'. Ignore on Read.	R/W	0
18.2	Reserved	Write as '0'. Ignore on Read.	R/W	0
18.1	INTEN	Interrupt Enable. 0 = Disable interrupts. 1 = Enable interrupts.	R/W	0
18.0	TINT	Test Force Interrupt 0 = Normal operation. 1 = Force interrupt on MDINT_L	R/W	0

1. R/W = Read /Write

Table 58 lists status change bits.

Table 58. Status Change Register - Address 19, Hex 13

Bit	Name	Description	Type [1]	Default
19.15:9	Reserved	Ignore on Read.	RO	N/A
19.8	Reserved	Ignore on Read.	RO	0
19.7	ANDONE	Auto-negotiation Status 0 = Auto-negotiation has not completed. 1 = Auto-negotiation has completed.	RO/ SC	N/A
19.6	SPEEDCHG	Speed Change Status 0 = A Speed Change has not occurred since last reading this register. 1 = A Speed Change has occurred since last reading this register.	RO/ SC	0
19.5	DUPLEXCHG	Duplex Change Status 0 = A Duplex Change has not occurred since last reading this register. 1 = A Duplex Change has occurred since last reading this register.	RO/ SC	0
19.4	LINKCHG	Link Status Change Status 0 = A Link Change has not occurred since last reading this register. 1 = A Link Change has occurred since last reading this register.	RO/ SC	0
19.3	Reserved	Ignore on Read.	RO	0
19.2	MDINT_L	0 = Management data interrupt (MII interrupt) Status.No MII interrupt pending. 1 = MII interrupt pending.	RO	0
19.1	Reserved	Ignore on Read.	RO	0
19.0	Reserved	Ignore on Read.	RO	0
1. R/W = Read/Write, RO = Read Only, SC = Self Clearing.				

Table 59 lists LED configuration bits.

Table 59. LED Configuration Register - Address 20, Hex 14 (Sheet 1 of 2)

Bit	Name	Description	Type [1]	Default
20.15:12	LED1 Programming bits	0000 = Display Speed Status (Continuous, Default) 0001 = Display Transmit Status (Stretched) 0010 = Display Receive Status (Stretched) 0011 = Display Collision Status (Stretched) 0100 = Display Link Status (Continuous) 0101 = Display Duplex Status (Continuous) 0110 = Unused 0111 = Display Receive or Transmit Activity (Stretched) 1000 = Test mode - turn LED on (Continuous) 1001 = Test mode - turn LED off (Continuous) 1010 = Test mode - blink LED fast (Continuous) 1011 = Test mode - blink LED slow (Continuous) 1100 = Display Link and Receive Status combined [2] (Stretched)[3] 1101 = Display Link and Activity Status combined [2] (Stretched)[3] 1110 = Display Duplex and Collision Status combined [4] (Stretched)[3] 1111 = Unused	R/W	0000
20.11:8	LED2 Programming bits	0000 = Display Speed Status 0001 = Display Transmit Status 0010 = Display Receive Status 0011 = Display Collision Status 0100 = Display Link Status (Default) 0101 = Display Duplex Status 0110 = Unused 0111 = Display Receive or Transmit Activity 1000 = Test mode - turn LED on 1001 = Test mode - turn LED off 1010 = Test mode - blink LED fast 1011 = Test mode - blink LED slow 1100 = Display Link and Receive Status combined [2] (Stretched)[3] 1101 = Display Link and Activity Status combined [2] (Stretched)[3] 1110 = Display Duplex and Collision Status combined [4] (Stretched)[3] 1111 = Unused	R/W	0100

1. R/W = Read /Write. RO = Read Only. LH = Latching High
2. Link status is the primary LED driver. The LED is asserted (solid ON) when the link is up. The secondary LED driver (Receive or Activity) causes the LED to change state (blink). Activity causes the LED to blink, regardless of the link status.
3. Combined event LED settings are not affected by Pulse Stretch Register bit 20.1. These display settings are stretched regardless of the value of 20.1.
4. Duplex status is the primary LED driver. The LED is asserted (solid ON) when the link is full-duplex. Collision status is the secondary LED driver. The LED changes state (blinks) when a collision occurs.
5. Values are approximations. Not guaranteed or production tested.

Table 59. LED Configuration Register - Address 20, Hex 14 (Sheet 2 of 2)

Bit	Name	Description	Type [1]	Default
20.7:4	LED3 Programming bits	0000 = Display Speed Status 0001 = Display Transmit Status 0010 = Display Receive Status (Default) 0011 = Display Collision Status 0100 = Display Link Status 0101 = Display Duplex Status 0110 = Unused 0111 = Display Receive or Transmit Activity 1000 = Test mode- turn LED on 1001 = Test mode- turn LED off 1010 = Test mode- blink LED fast 1011 = Test mode- blink LED slow 1100 = Display Link and Receive Status combined [2] (Stretched)[3] 1101 = Display Link and Activity Status combined [2] (Stretched)[3] 1110 = Display Duplex and Collision Status combined [4] (Stretched)[3] 1111 = Unused	R/W	0010
20.3:2	LEDFREQ[5]	00 = Stretch LED events to 30 ms. 01 = Stretch LED events to 60 ms. 10 = Stretch LED events to 100 ms. 11 = Reserved.	R/W	00
20.1	PULSE-STRETCH	0 = Disable pulse stretching of all LEDs. 1 = Enable pulse stretching of all LEDs.	R/W	1
20.0	Reserved	Write as ‘0’. Ignore on Read.	R/W	0

1. R/W = Read /Write. RO = Read Only. LH = Latching High
2. Link status is the primary LED driver. The LED is asserted (solid ON) when the link is up. The secondary LED driver (Receive or Activity) causes the LED to change state (blink). Activity causes the LED to blink, regardless of the link status.
3. Combined event LED settings are not affected by Pulse Stretch Register bit 20.1. These display settings are stretched regardless of the value of 20.1.
4. Duplex status is the primary LED driver. The LED is asserted (solid ON) when the link is full-duplex. Collision status is the secondary LED driver. The LED changes state (blinks) when a collision occurs.
5. Values are approximations. Not guaranteed or production tested.

Table 60 lists digital configuration bits for the LXT971A Transceiver.

Table 60. Digital Configuration Register - Address 26, Hex 1A (Sheet 1 of 2)

Bit	Name	Description	Type [1]	Default
26.15:12	Reserved	Write as ‘0’. Ignore on Read.	R/W	0000
26.11	MII Drive Strength	MII Drive Strength 0 = Normal MII drive strength 1 = Increase MII drive strength	R/W	0
26.10	Reserved	Write as ‘0’. Ignore on Read.	R/W	0
26.9	Show Symbol Error	Show Symbol Error 0 = Normal MII_RXER 1 = 100BASE-X Error Signal to MII_RxER	R/W	0
26.8:6	Reserved	Write as ‘0’. Ignore on Read.	RO	0

1. R/W = Read /Write, RO = Read Only

Table 60. Digital Configuration Register - Address 26, Hex 1A (Sheet 2 of 2)

Bit	Name	Description	Type [1]	Default
26.5:4	Reserved	Write as '0'. Ignore on Read.	R/W	00
26.3	Reserved	Write as '0'. Ignore on Read.	RO	0
26.2:0	Reserved	Write as '0'. Ignore on Read.	R/W	0
1. R/W = Read /Write, RO = Read Only				

Table 61 lists digital configuration bits for the LXT971A Transceiver.

Table 61. Digital Configuration Register - Address 26, Hex 1A

Bit	Name	Description	Type [1]	Default
26.15:12	Reserved	Write as '0'. Ignore on Read.	R/W	0000
26.11	MII Drive Strength	MII Drive Strength 0 = Normal MII drive strength 1 = Increase MII drive strength	R/W	0
26.10	Reserved	Write as '0'. Ignore on Read.	R/W	0
26.9	Show Symbol Error	Show Symbol Error 0 = Normal MII_RXER 1 = 100BASE-X Error Signal to MII_RxER	R/W	0
26.8:0	Reserved	Write as '0'. Ignore on Read.	RO	000000000
1. R/W = Read /Write, RO = Read Only				

Table 62 lists transmit control bits.

Table 62. Transmit Control Register - Address 30, Hex 1E

Bit	Name	Description	Type[2]	Default
30.15:13	Reserved	Write as '0'. Ignore on Read.	R/W	000
30.12	Transmit Low Power	Transmit Low Power 0 = Normal transmission. 1 = Forces the transmitter into low power mode. Also forces a zero-differential transmission.	R/W	0
30.11:10	Port Rise Time Control[1]	Port Rise Time Control 00 = 3.0 ns (Default = Setting on TXSLEW[1:0] pins) 01 = 3.4 ns 10 = 3.9 ns 11 = 4.4 ns	R/W	Note 3
30.9:0	Reserved	Ignore on Read.	R/W	0000000000

1. Values are approximations and may vary outside indicated values based upon implementation loading conditions. Not guaranteed.
2. R/W = Read/Write
3. Latch State during Reset is based on the state of hardware configuration pins at RESET_L.

10.0 Intel® LXT971A Transceiver Package Specifications

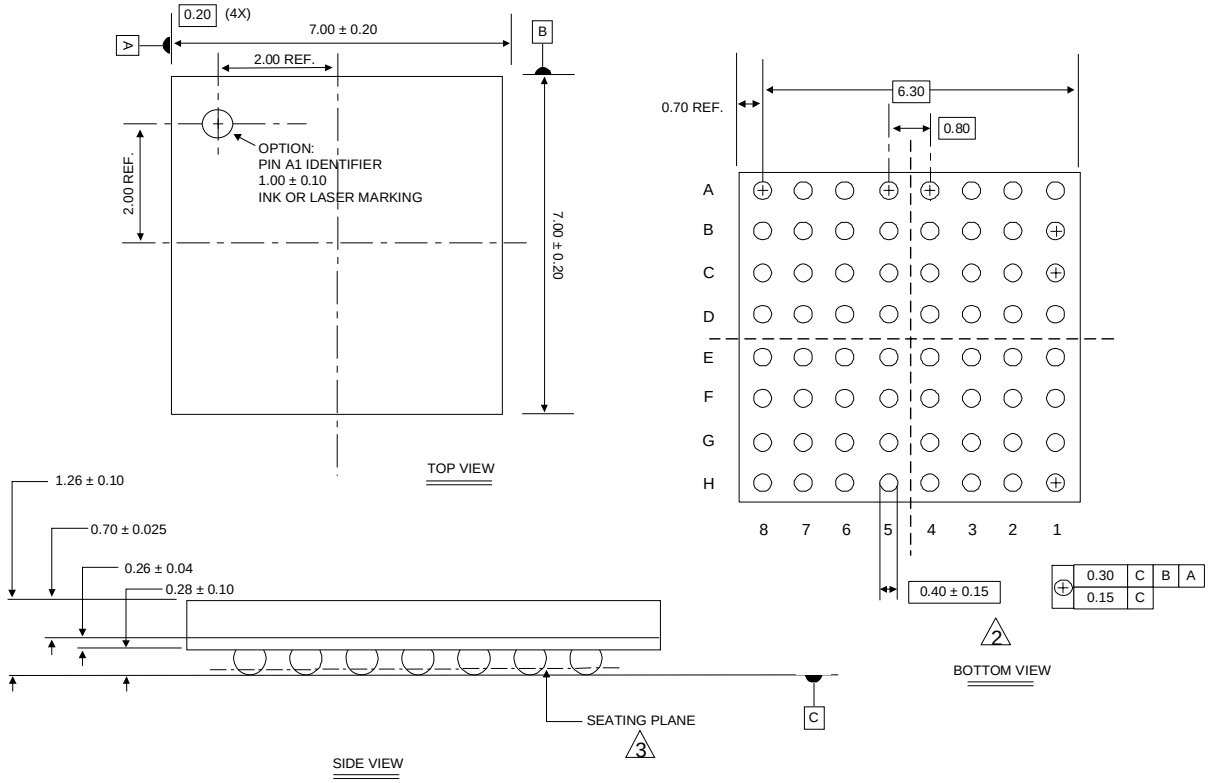
Figure 43. Intel® LXT971A Transceiver PBGA Package Specification

64-Ball Plastic Ball Grid Array Package

Part Number LXT971ABC - Commercial Temperature Range (0ºC to +70ºC)

Part Number LXT971ABE - Extended Temperature Range (-40ºC to +85ºC)

NOTE: The package figure is generic and used only to demonstrate package dimensions. (The figure does not show the same number of pins as for the Intel® LXT971A Transceiver PBGA.)



NOTES:
1. All dimensions and tolerances conform to ASME Y 14.5 M - 1994.
2. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
3. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
4. Maximum mold to substrate offset shall be 0.127.
5. The surface finish of the package shall be EDM Charmille #18 - #21.
6. Unless otherwise specified tolerance: Decimal ± 0.05 Angular ±2°.

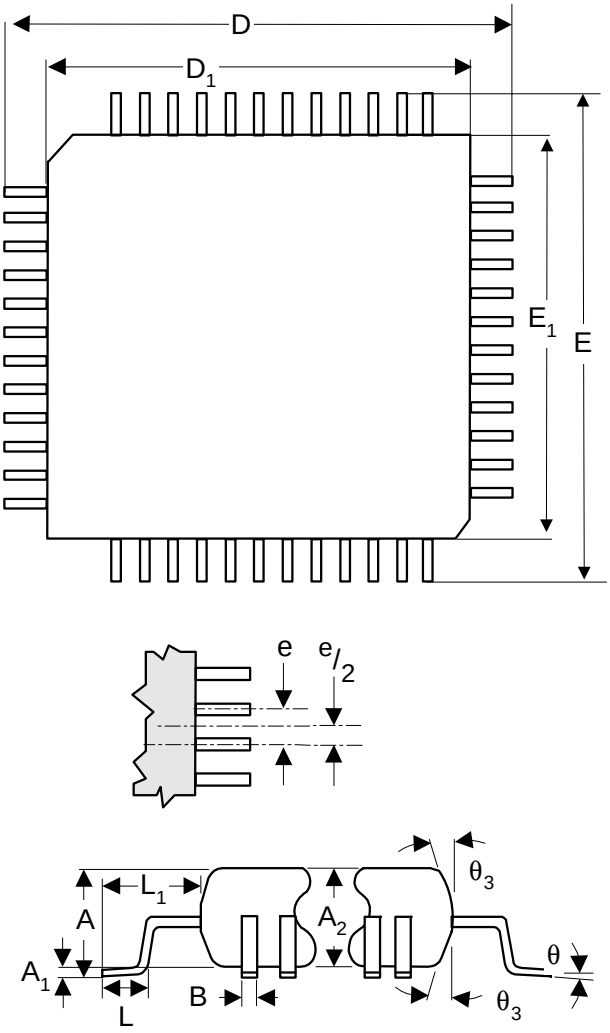
Figure 44. Intel® LXT971A Transceiver LQFP Package Specifications

64-Pin Low-Profile Quad Flat Pack

NOTE: The package figure is generic and used only to demonstrate package dimensions. (The figure does not show the same number of pins as for the Intel® LXT971A Transceiver LQFP.)

Dim	Millimeters	
	Min	Max
A	–	1.60
A_1	0.05	0.15
A_2	1.35	1.45
B	0.17	0.27
D	11.85	12.15
D_1	9.9	10.1
E	11.85	12.15
E_1	9.9	10.1
e	0.50 BSC[1]	
L	0.45	0.75
L_1	1.00 REF	
θ_3	11°	13°
θ	0°	7°

1. Basic Spacing between Centers



10.1 Top Label Markings

Figure 45 shows a sample LQFP package for the LXT971A Transceiver.

Note: In contrast to the Pb-Free (RoHS-compliant) LQFP packages, the non-RoHS-compliant packages do not have the “e3” symbol in the last line of the package label.

Figure 45. Sample LQFP Package - Intel® LXT971A Transceiver

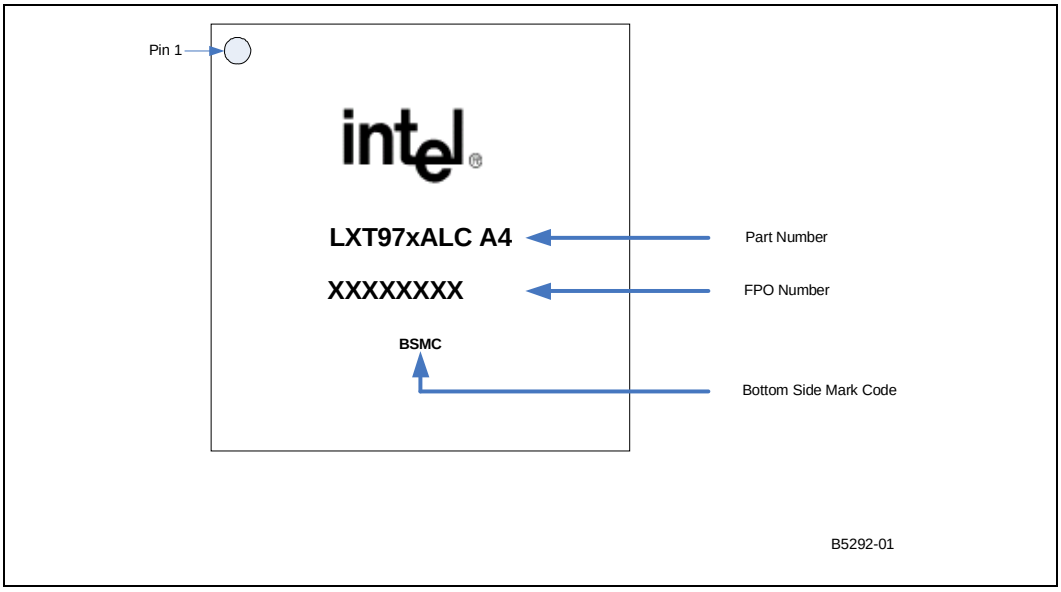


Figure 46 shows a sample Pb-Free (RoHS-compliant) LQFP package for the LXT971A Transceiver.

Figure 46. Sample Pb-Free (RoHS-Compliant) LQFP Package - Intel® LXT971A Transceiver

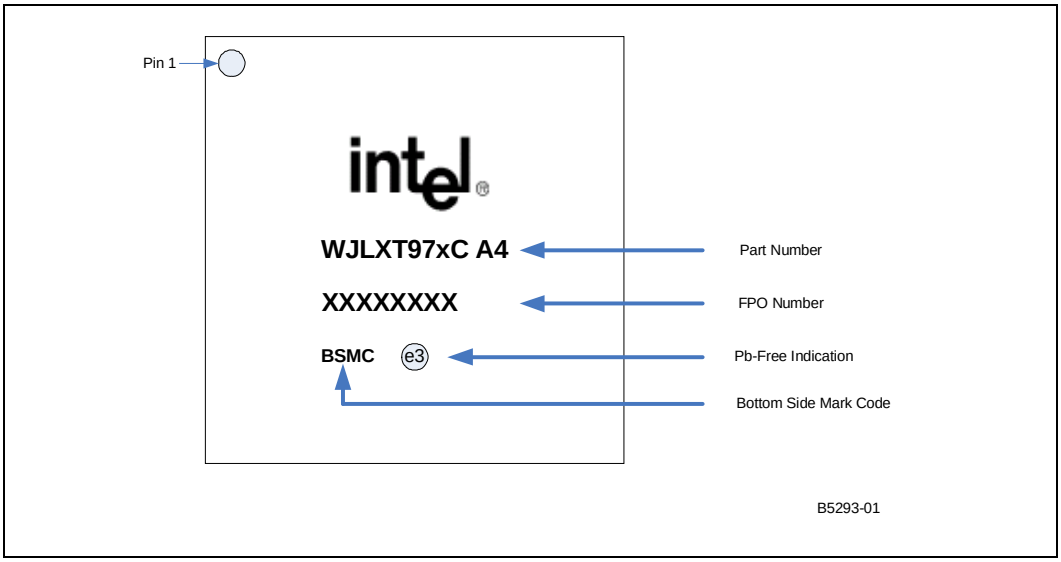


Figure 47 shows a sample TPBGA package for the LXT971A Transceiver.

Note: In contrast to the Pb-Free (RoHS-compliant) TPBGA package, the non-RoHS-compliant package does not have the “e3” symbol in the last line of the package label.

Figure 47. Sample TPBGA Package - Intel® LXT971A Transceiver

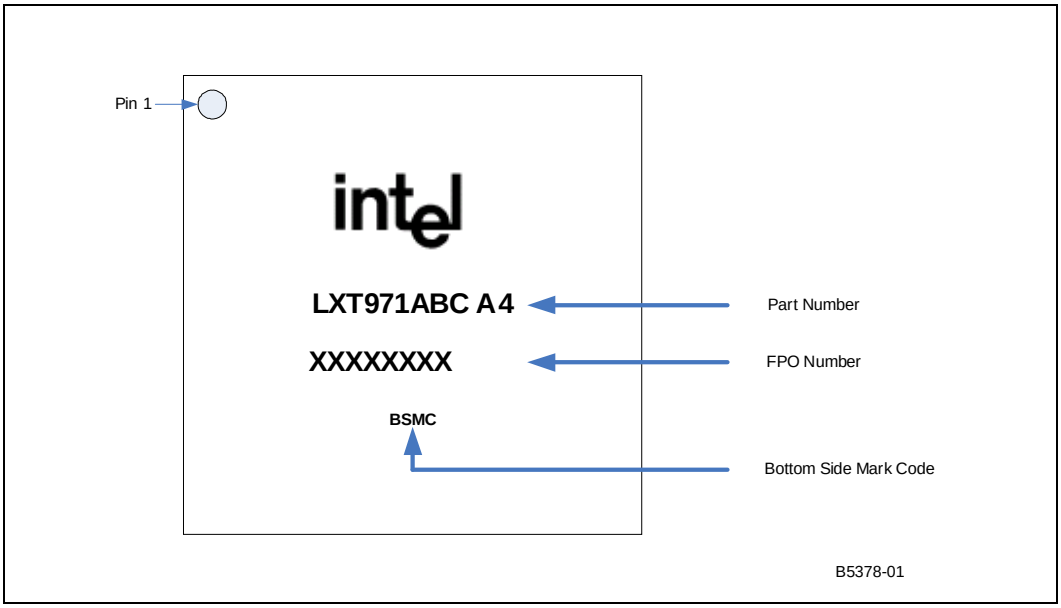
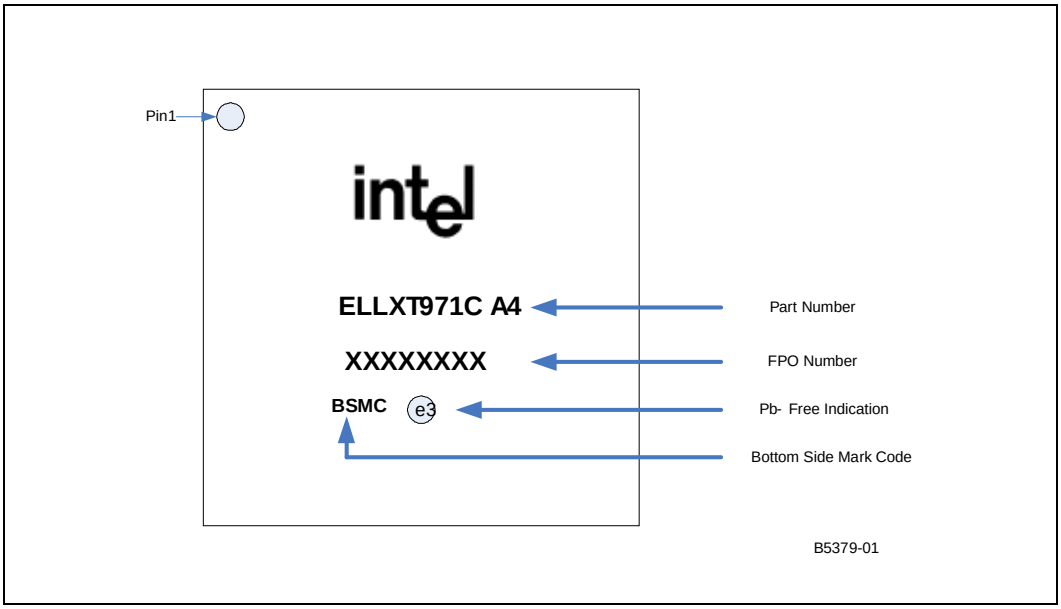


Figure 48 shows a sample Pb-Free (RoHS-Compliant) TPBGA package for the LXT971A Transceiver.

Figure 48. Sample Pb-Free (RoHS Compliant) TPBGA Package - Intel® LXT971A Transceiver



11.0 Product Ordering Information

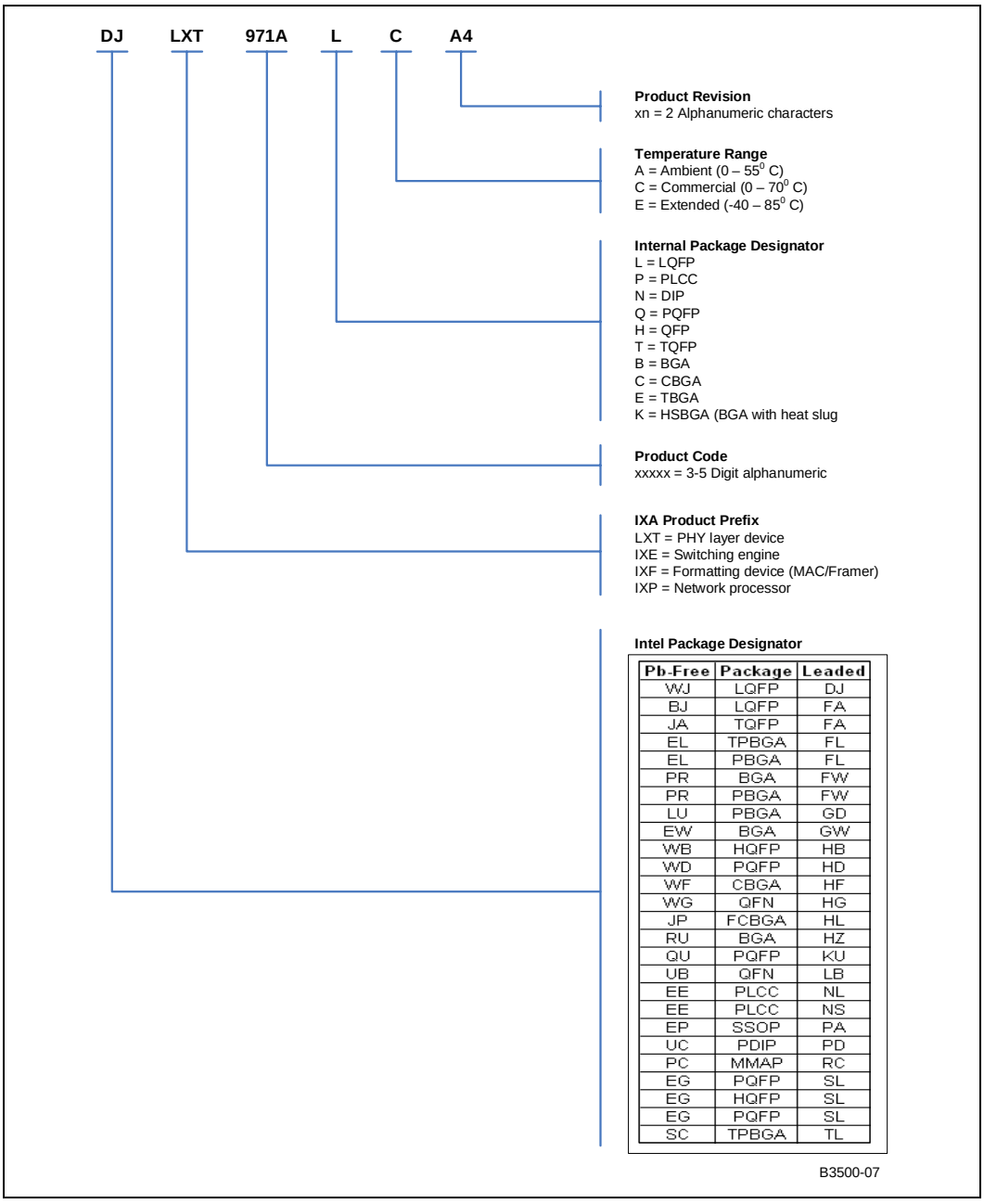
Table 63 lists product ordering information for the LXT971A Transceiver.

Table 63. Product Ordering Information

Number	Revision	Package Type	Pin Count	RoHS Compliant
DJLXT971ALC.A4	A4	LQFP	64	No
DJLXT971ALE.A4	A4	LQFP	64	No
WJLXT971ALC.A4	A4	LQFP	64	Yes
WJLXT971ALE.A4	A4	LQFP	64	Yes
FLLXT971ABC.A4	A4	TPBGA	64	No
FLLXT971ABE.A4	A4	TPBGA	64	No
ELLXT971ABC.A4	A4	TPBGA	64	Yes
ELLXT971ABE.A4	A4	TPBGA	64	Yes

Figure 49 shows an order matrix with sample information for ordering an LXT971A Transceiver.

Figure 49. Order Matrix for Intel® LXT971A Transceiver - Sample



Pb-Free	Package	Leaded
WJ	LQFP	DJ
BJ	LQFP	FA
JA	TQFP	FA
EL	TPBGA	FL
EL	PBGA	FL
PR	BGA	FW
PR	PBGA	FW
LU	PBGA	GD
EW	BGA	GW
WB	HQFP	HB
WD	PQFP	HD
WF	CBGA	HF
WG	QFN	HG
JP	FCBGA	HL
RU	BGA	HZ
QU	PQFP	KU
UB	QFN	LB
EE	PLCC	NL
EE	PLCC	NS
EP	SSOP	PA
UC	PDIP	PD
PC	MMAP	RC
EG	PQFP	SL
EG	HQFP	SL
EG	PQFP	SL
SC	TPBGA	TL