LXT983/983A

LXT983/983A Dual Speed, 5-Port Fast Ethernet Repeater

Datasheet

General Description

The LXT983 is a 5-port 10/100 Class II Repeater that is fully compliant with IEEE 802.3 standards. Four ports directly support 100BASE-TX/10BASE-T copper media and also support 100BASE-FX fiber media via pseudo-ECL (PECL) interfaces. The fifth port, a 10- or 100-Mbps Media Independent Interface (MII), connects to Media Access Controllers (MACs) for bridge/switch applications. At 100 Mbps, the MII can also be configured to interface to another PHY device, such as the LXT970. This data sheet applies to all LXT983 products (LXT983, LXT983A, and any subsequent variants), except as specifically noted.

The LXT983 provides auto-negotiation with parallel detection for the four PHY ports. These ports can also be configured by the user. The LXT983 provides two internal repeater state machines—one operating at 10 Mbps and one at 100 Mbps. Once configured, the LXT983 automatically connects each port to the appropriate repeater.

The LXT983 provides two Inter-Repeater Backplanes (IRBs) for expansion—one operating at 10 Mbps and one at 100 Mbps. Up to 240 ports can be logically combined into one repeater.

Product Features

- Four 10/100 ports include:
- Complete twisted-pair PHYs with integrated filters.
- 100BASE-FX PECL interfaces.
- 10/100 MII port connection to either MAC or PHY.
- Independent segments for 10 and 100 Mbps operation.
- Cascadable IRBs.
- Integrated per-port LED drivers with user-selectable modes.
- Integrated per-segment LED drivers for collisions and activity.
- Available in 208-pin QFP package.
- Case Temperature Range: 0-115°C.

As of January 15, 2001, this document replaces the Level One document *LXT983/983A — Dual Speed, 5-Port Fast Ethernet Repeater.*

Order Number: 249112-001
January 2001

Datasheet

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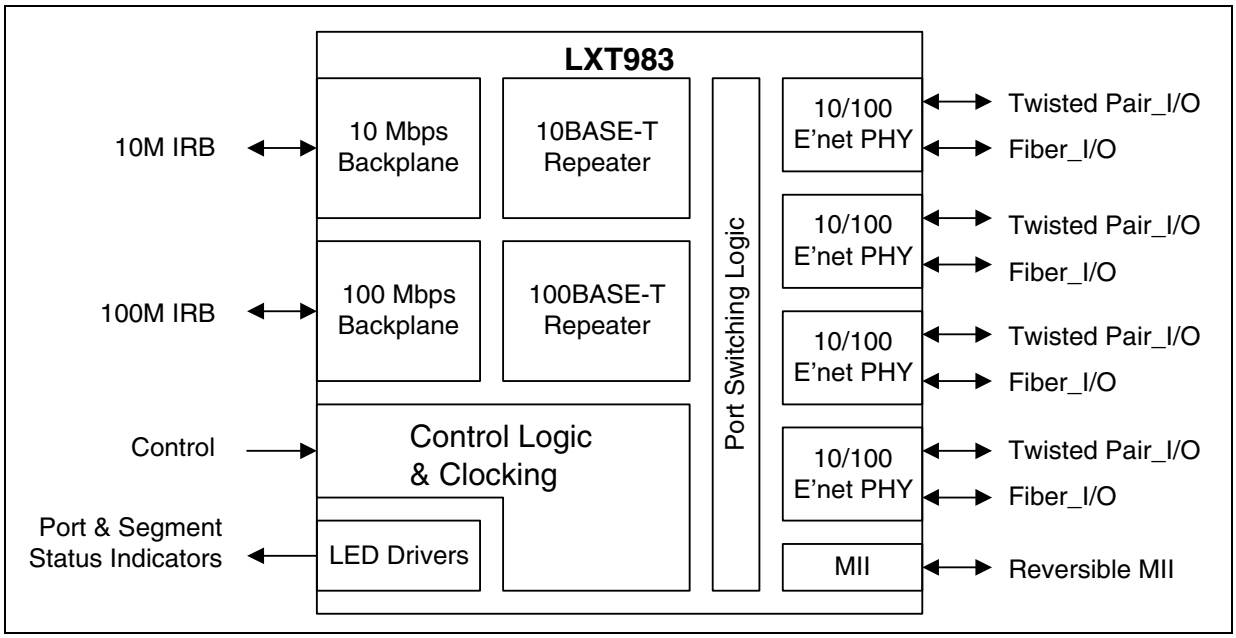
Revision History

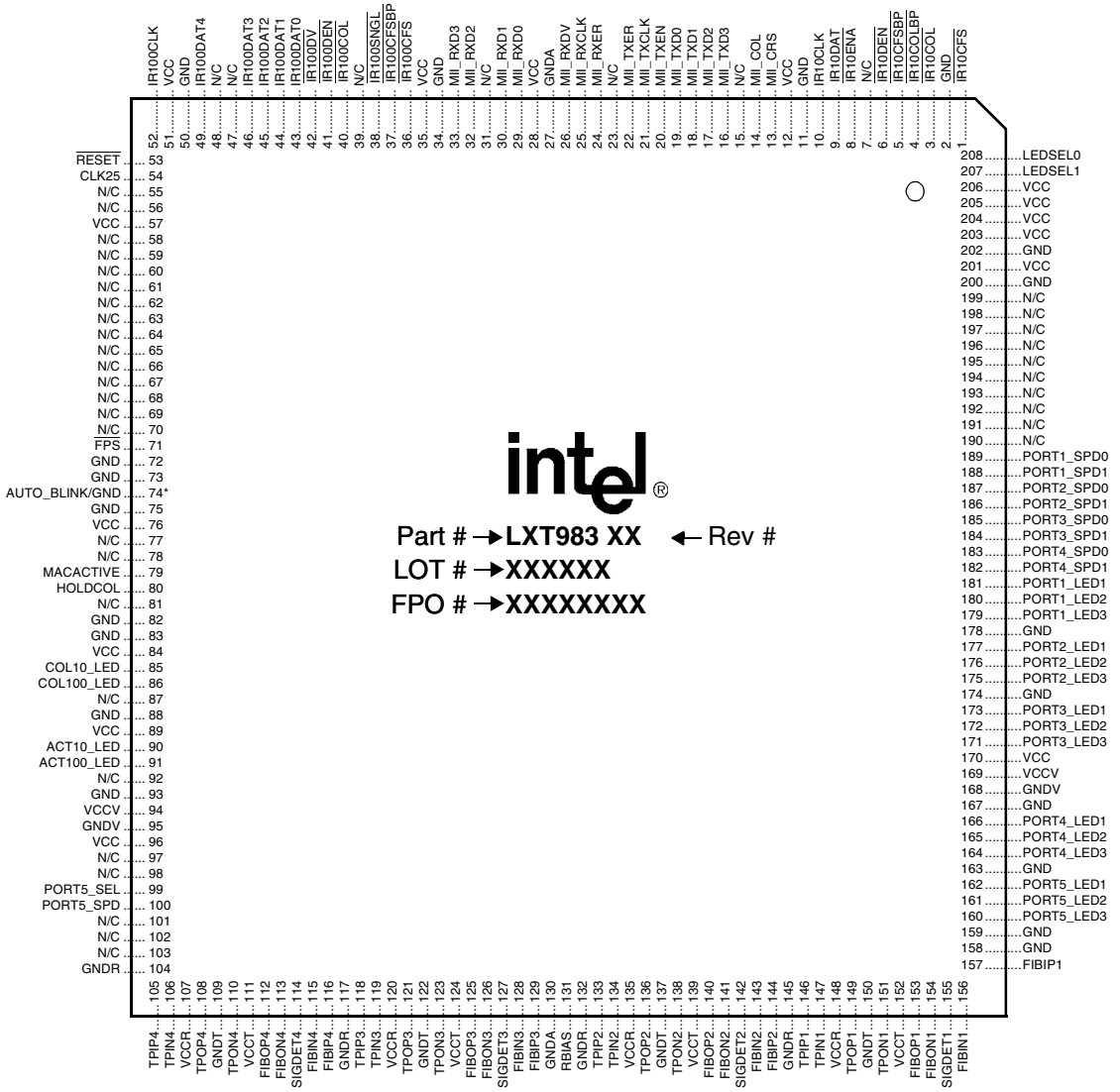
Revision	Date	Description

Figure 1. LXT983/983A Block Diagram



1.0 Pin Assignments and Signal Descriptions

Figure 2. LXT983 Pin Assignments



***Note:** For Pin 74 Signal Description, see Table 8 on page 14 (**LXT983**) and Table 9 on page 15 (**LXT983A**).

Package Topside Markings

Marking	Definition
Part #	LXT983 is the unique identifier for this product family.
Rev #	Identifies the particular silicon “stepping” (Refer to Specification Update for additional stepping information.)
Lot #	Identifies the batch.
FPO #	Identifies the Finish Process Order.

Table 1. Mode Control Signal Descriptions

Pin	Symbol	Type[1]	Description
189 188	PORT1_SPD0 PORT1_SPD1	TTL Input, Latched on reset, PU	**Speed Select - Ports 1 through 4.** These pins configure the associated port as follows:
187 186	PORT2_SPD0 PORT2_SPD1		SPD1 / SPD0 / Mode 0 / 0 / Allow 10/100 Auto-Negotiation/Parallel Detection. 0 / 1 / Force 10BASE-T. 1 / 0 / Force 100BASE-FX. 1 / 1 / Force 100BASE-TX.
185 184	PORT3_SPD0 PORT3_SPD1		
183 182	PORT4_SPD0 PORT4_SPD1		
100	PORT5_SPD	TTL Input, PU	**Speed Select - Port 5.** Selects operating speed of the MII (MAC) interface. Also selects on which segment statistics are kept. High = 100 Mbps, Low = 10 Mbps. (Port 5 speed of 10 Mbps is available when PHY mode is selected.)
99	PORT5_SEL	Input	**Mode Select - Port 5.** Selects operating mode of the MII interface. Pin is monitored at power-up and reset. Subsequent changes have no effect. High = PHY Mode (LXT983 acts as PHY side of the MII). Low = MAC Mode (LXT983 acts as MAC side of the MII).

1. PU = Input contains pull-up.
   TTL = Transistor-Transistor Logic.

Table 2. Twisted-Pair Port Signal Descriptions

Pin	Symbol	Type	Description
149, 151 136, 138 121, 123 108, 110	TPOP1, TPON1 TPOP2, TPON2 TPOP3, TPON3 TPOP4, TPON4	Analog Output	**Twisted-Pair Outputs - Ports 1 through 4.** These pins are the positive and negative outputs from the respective ports twisted-pair line drivers. These pins may be left open when not used.
146, 147 133, 134 118, 119 105, 106	TPIP1, TPIN1 TPIP2, TPIN2 TPIP3, TPIN3 TPIP4, TPIN4	Analog Input	**Twisted-Pair Inputs - Ports 1 through 4.** These pins are the positive and negative inputs to the respective ports twisted-pair receivers. These pins may be left open when not used.

Table 3. Fiber Port Signal Descriptions

Pin	Symbol	Type	Description
153, 154 140, 141 125, 126 112, 113	FIBOP1, FIBON1 FIBOP2, FIBON2 FIBOP3, FIBON3 FIBOP4, FIBON4	PECL Output	**Fiber Outputs - Ports 1 through 4.** These pins are the positive and negative outputs from the respective ports PECL drivers. These pins may be left open when not used.
157, 156 144, 143 129, 128 116, 115	FIBIP1, FIBIN1 FIBIP2, FIBIN2 FIBIP3, FIBIN3 FIBIP4, FIBIN4	PECL Input	**Fiber Inputs - Ports 1 through 4.** These pins are the positive and negative inputs to the respective ports PECL receivers. These pins may be left open when not used.
155 142 127 114	SIGDET1 SIGDET2 SIGDET3 SIGDET4	PECL Input	**Signal Detect - Ports 1 through 4.** Signal detect for the fiber ports. These pins may be left open when not used.

Table 4. PHY Mode MII Signal Descriptions

Pin	Symbol	Type[1]	Description
29 30 32 33	MII_RXD0 MII_RXD1 MII_RXD2 MII_RXD3	Output TTL	**Receive Data.** The LXT983 transmits received data to the controller on these outputs. Data is driven on the falling edge of MII_RXCLK.
26	MII_RXDV	Output TTL	**Receive Data Valid.** Active High signal, synchronous to MII_RXCLK, indicates valid data on MII_RXD<3:0>.
25	MII_RXCLK	Output TTL	**Receive Clock.** MII receive clock for expansion port. This is a 2.5 or 25 MHz clock derived from the CLK25 input (refer to Table 9).
24	MII_RXER	Output TTL	**Receive Error.** Active High signal, synchronous to MII_RXCLK, indicates invalid data on MII_RXD<3:0>.
22	MII_TXER	Input TTL	**Transmit Error.** This is a 100M-only signal. The MAC asserts this input when an error has occurred in the transmit data stream. The LXT983 responds by sending 'Invalid Code Symbols' on the line.
21	MII_TXCLK	Output TTL	**Transmit Clock.** 2.5 or 25 MHz continuous output derived from the 25 MHz input clock.
20	MII_TXEN	Input TTL	**Transmit Enable.** External controllers drive this input High to indicate that data is being transmitted on the MII_TXD<3:0> pins. Tie this input Low if it is unused.
19 18 17 16	MII_TXD0 MII_TXD1 MII_TXD2 MII_TXD3	Input TTL	**Transmit Data.** External controllers use these inputs to transmit data to the LXT983. The device samples MII_TXD<3:0> on the rising edge of MII_TXCLK, when MII_TXEN is High.
14	MII_COL	Output TTL	**Collision.** The LXT983 drives this signal High to indicate that a collision has occurred.
13	MII_CRS	Output TTL	**Carrier Sense.** Active High signal indicates that the LXT983 is transmitting or receiving.

1. MII interface pins reverse direction based on PHY/MAC mode. Direction listed is for PHY mode.

Table 5. MAC Mode MII Signal Descriptions

Pin	Symbol	Type[1]	Description
29 30 32 33	MII_RXD0 MII_RXD1 MII_RXD2 MII_RXD3	**Input TTL**	**Receive Data.** The LXT983 receives data from the PHY on these pins. Data is sampled on the rising edge of MII_RXCLK.
26	MII_RXDV	**Input TTL**	**Receive Data Valid.** The PHY asserts this active High signal, synchronous to MII_RXCLK, to indicate valid data on MII_RXD<3:0>.
25	MII_RXCLK	**Input TTL**	**Receive Clock.** MII receive clock for expansion port. This is a 25 MHz clock.
24	MII_RXER	**Input TTL**	**Receive Error.** The PHY asserts this active High signal, synchronous to MII_RXCLK, to indicate invalid data on MII_RXD<3:0>.
22	MII_TXER	**Output TTL**	**Transmit Error.** The LXT983 asserts this signal when an error has occurred in the Transmit data stream.
21	MII_TXCLK	Input TTL	**Transmit Clock.** 25 MHz continuous input clock. Must be supplied from same source as CLK25 system clock.

1. MII interface pins reverse direction based on PHY/MAC mode. Direction listed is for MAC mode.

Table 5. MAC Mode MII Signal Descriptions (Continued)

Pin	Symbol	Type[1]	Description
20	MII_TXEN	Output TTL	**Transmit Enable.** The LXT983 drives this output High to indicate that data is being transmitted on the MII_TXD<3:0> pins.
19 18 17 16	MII_TXD0 MII_TXD1 MII_TXD2 MII_TXD3	Output TTL	**Transmit Data.** The LXT983 drives these outputs to transmit data to the PHY. The device drives MII_TXD<3:0> on the rising edge of MII_TXCLK, when MII_TXEN is High.
14	MII_COL	Input TTL	**Collision.** The PHY asserts this active High signal to notify the LXT983 that a collision has occurred.
13	MII_CRS	Input TTL	**Carrier Sense.** The PHY asserts this active High signal to notify the LXT983 that the PHY is transmitting or receiving.

1. MII interface pins reverse direction based on PHY/MAC mode. Direction listed is for MAC mode.

Table 6. Inter-Repeater Backplane Signal Descriptions

Pin	Symbol	Type[1]	Description[2]
		100 Mbps IRB Signals	
43 44 45 46 49	IR100DAT0 IR100DAT1 IR100DAT2 IR100DAT3 IR100DAT4	Tri-state Schmitt CMOS I/O, PU	**100 Mbps IRB Data.** These bidirectional signals carry data on the 100 Mbps IRB. Data is driven on the falling edge and sampled on the rising edge of IR100CLK. These signals can be buffered between boards.
52	IR100CLK	Tri-state Schmitt CMOS I/O, PD	**100 Mbps IRB Clock.** This bidirectional, non-continuous, 25 MHz clock is recovered from received network traffic. Schmitt triggering is used to increase noise immunity. This signal must be pulled to VCC when idle. One 1 kΩ pull-up resistor on both sides of a ‘245 buffer is recommended.
41	IR100DEN	TTL Output, OD	**100 Mbps IRB Driver Enable.** This output provides directional control for an external bidirectional transceiver (‘245) used to buffer the 100 Mbps IRB in multi-board applications. It must be pulled up by a 330Ω resistor. When there are multiple devices on one board, tie all $\overline{\text{IR100DEN}}$ outputs together. If $\overline{\text{IR100DEN}}$ is tied directly to the DIR pin on a ‘245, attach the on-board IR100DAT, IR100CLK and $\overline{\text{IR100DV}}$ signals to the “B” side of the ‘245, and connect the off-board signals to the “A” side of the ‘245.
42	$\overline{\text{IR100DV}}$	Schmitt CMOS I/O, OD, PU	**100 Mbps IRB Data Valid.** This active Low signal indicates repeater port activity. $\overline{\text{IR100DV}}$ frames the clock and data of the packet on the backplane. This signal must be pulled up by a 120Ω resistor.
36	$\overline{\text{IR100CFS}}$	Analog I/O	**100 Mbps IRB Collision Force Sense.** This three-level signal determines the number of active ports on the “logical repeater”. The High level (5V) indicates no ports active; Mid-level (approx. 2.8V) indicates one port active; Low level (0V) indicates more than one port active, resulting in a collision. $\overline{\text{IR100CFS}}$ connects between chips on the same board. Do not connect between boards. This signal requires a 240Ω pull-up resistor.

1. NC = No Clamp. Pad will not clamp input in the absence of power.
   PU = Input contains pull-up.
   PD = Input contains pull-down.
   I/O = Input / Output.
   OD = Open Drain
   TTL = Transistor-Transistor Logic.
2. Even if the IRB is not used, required pull-up resistors must be installed as listed above.

Table 6. Inter-Repeater Backplane Signal Descriptions (Continued)

Pin	Symbol	Type[1]	Description[2]
37	IR100CFSBP	Analog I/O NC	**100 Mbps IRB Collision Force Sense - Backplane.** IR100CFSBP functions the same as IR100CFS; however, IR100CFSBP connects between chips with ChipID = 0, on different boards. This signal requires a single 91 Ω pull-up resistor on each stack.
38	IR100SNGL	Schmitt CMOS I/O, PU	**100 Mbps Single Driver State.** This active Low signal is asserted by the device with ChipID = 000 when a packet is being received from one or more ports. It should not be connected between boards.
40	IR100COL	Schmitt MOS I/O, PU	**100 Mbps Multiple Driver State.** This active Low signal is asserted by the device with ChipID = 000 when a packet is being received from more than one port (collision). It should not be connected between boards.
		10 Mbps IRB Signals	
9	IR10DAT	CMOS I/O OD, PD	**10 Mbps IRB Data.** This bidirectional signal carries data on the corresponding IRB. Data is driven and sampled on the rising edge of the corresponding IRCLK. This signal must be pulled up by a 330Ω resistor. Between boards, this signal can be buffered.
10	IR10CLK	Tri-state Schmitt CMOS I/O, PD	**10 Mbps IRB Clock.** This bidirectional, non-continuous, 10 MHz clock is recovered from received network traffic. During idle periods, the output is tri-stated. Schmitt triggering is used to increase noise immunity.
6	IR10DEN	TTL Output, OD	**10 Mbps IRB Driver Enable.** This output provides directional control for an external bidirectional transceiver (‘245) used to buffer the IRBs in multi-board applications. It must be pulled up by a 330Ω resistor. When there are multiple devices on one board, tie all IR10DEN outputs together. If IR10DEN is tied directly to the DIR pin on a ‘245, attach the on-board IR10DAT, IR10CLK, and IR10ENA signals to the “B” side of the ‘245, and connect the off-board signals to the “A” side of the ‘245.
8	IR10ENA	CMOS I/O OD, PU	**10 Mbps IRB Enable.** This active Low output indicates carrier presence on the IRB. A 330Ω pull-up resistor is required to pull the IR10ENA output High when the IRB is idle. When there are multiple devices, tie all IR10ENA outputs together. This signal may be buffered between boards.
3	IR10COL	CMOS I/O OD, PU	**10 Mbps IRB Collision.** This output is driven Low to indicate that a collision has occurred on the 10 Mbps segment. A 330Ω resistor is required in each box to pull this signal High when there is no collision. This signal should not be connected between boards and it may not be buffered.
4	IR10COLBP	CMOS I/O OD, NC	**10 Mbps IRB Collision - Backplane.** This active Low output has the same function as IR10COL, but is used between boards. Attach this signal only from the device with ChipID = 0 to the backplane or connector, **without buffering**. The output must be pulled up by one 330Ω resistor per system.
1	IR10CFS	Analog I/O, OD	**10 Mbps IRB Collision Force Sense.** This three-state analog signal indicates transmit collision when driven Low. It requires a 680Ω, 1% resistor. Do not connect between boards, and do not buffer.

1. NC = No Clamp. Pad will not clamp input in the absence of power.
   PU = Input contains pull-up.
   PD = Input contains pull-down.
   I/O = Input / Output.
   OD = Open Drain
   TTL = Transistor-Transistor Logic.
2. Even if the IRB is not used, required pull-up resistors must be installed as listed above.

Table 6. Inter-Repeater Backplane Signal Descriptions (Continued)

Pin	Symbol	Type[1]	Description[2]
5	IR10CFSBP	Analog I/O OD, NC	**10 Mbps IRB Collision Force Sense - Backplane.** This signal functions the same as IR10CFS, but connects between boards. Attach this signal only from the device with ChipID = 0 to the backplane or connector, **without buffering**. This signal requires one 330Ω, 1% pull-up resistor per system.
79	MACACTIVE	TTL Input PD	**MAC Active.** A TTL-level signal to which an external MAC's transmit enable can be attached. Use of Macactive allows the repeater—not the MAC—to drive the three-level IRCFS pin. Active High input allows external ASICs to connect with 10 Mbps IRB. Driving data onto the IRB requires the external ASIC to assert MACACTIVE High for one clock cycle, and then assert IR10ENA Low. ASIC monitors IR10COL (active Low) for collisions. (See "MAC IRB Access" on page 26.)
80	HOLDCOL	TTL I/O PD	**Hold Collision for 10 Mbps Mode.** This active High signal is driven by the device with FPS = Low to extend a non-local transmit collision to other devices on the same board. The HOLDCOL signals from different boards should *not* be attached together.

1. NC = No Clamp. Pad will not clamp input in the absence of power.
   PU = Input contains pull-up.
   PD = Input contains pull-down.
   I/O = Input / Output.
   OD = Open Drain
   TTL = Transistor-Transistor Logic.
2. Even if the IRB is not used, required pull-up resistors must be installed as listed above.

Table 7. LED Signal Descriptions

Pin	Symbol	Type	Description
208 207	LEDSEL0 LEDSEL1	TTL Input PD	**LED Mode Select**. Must be static. 00 = Mode 1, 01 = Mode 2, 10 = Mode 3
181 177 173 166 162	PORT1_LED1 PORT2_LED1 PORT3_LED1 PORT4_LED1 PORT5_LED1	TTL Output	**LED Driver 1 - Ports 1 through 5.** Programmable LED driver. Active Low. See "Port LEDs" on page 24.
180 176 172 165 161	PORT1_LED2 PORT2_LED2 PORT3_LED2 PORT4_LED2 PORT5_LED2	TTL Output	**LED Driver 2 - Ports 1 through 5.** Programmable LED driver. Active Low. See "Port LEDs" on page 24.
179 175 171 164 160	PORT1_LED3 PORT2_LED3 PORT3_LED3 PORT4_LED3 PORT5_LED3	TTL Output	**LED Driver 3 - Ports 1 through 5.** Programmable LED driver. Active Low. See "Port LEDs" on page 24.
85	COL10_LED	TTL Output	**10 Mbps Collision LED Driver.** Active Low indicates collision on 10M segment.

1. PD = Input contains pull-down.
   TTL = Transistor-Transistor Logic.

Table 7. LED Signal Descriptions (Continued)

Pin	Symbol	Type	Description
86	COL100_LED	TTL Output	**100 Mbps Collision LED Driver.** Active Low indicates collision on 100M segment.
90	ACT10_LED	TTL Output	**10 Mbps Activity LED Driver.** Active Low indicates activity on 10M segment.
91	ACT100_LED	TTL Output	**100 Mbps Activity LED Driver.** Active Low indicates activity on 100M segment.
1. PD = Input contains pull-down. TTL = Transistor-Transistor Logic.			

Table 8. Power Supply and Indication Signal Descriptions

Pin	Symbol	Type	Description
12, 28, 35, 51, 57, 76, 84, 89, 96, 170, 201, 203-206	VCC	Digital	**Power Supply Inputs.** Each of these pins must be connected to a common +5 VDC power supply. A de-coupling capacitor to ground should be supplied for every one of these pins.
2, 11, 34, 50, 72, 73, 75, 82, 83, 88, 93, 158, 159, 163, 167, 174, 178, 200, 202	GND	Digital	**Ground.** Connect each of these pins to ground. If using an LXT983 in an LXT980-based design, LXT983 Chip ID 1 and Chip ID 2 do not have to be tied to ground.
74	GND (**LXT983**)	Digital	**Ground.** Connect this pin to digital ground. **Note:** For LXT983A, refer to Table 9 on page 15.
94, 169	VCCV	Analog	**VCO Supply Inputs.** Each of these pins must be connected to a common +5 VDC power supply. A de-coupling capacitor to GNDV should be supplied for every one of these pins
95, 168	GNDV	Analog	**VCO Ground**.
111, 124, 139, 152	VCCT	Analog	**Transmitter Supply Inputs.** Each of these pins must be connected to a common +5 VDC power supply. A de-coupling capacitor to GNDT should be supplied for every one of these pins.
109, 122, 137, 150	GNDT	Analog	**Transmitter Ground.**
107, 120, 135, 148	VCCR	Analog	**Receiver Supply Inputs.** Each of these pins must be connected to a common +5 VDC power supply. A de-coupling capacitor to GNDR should be supplied for every one of these pins
104, 117, 132, 145,	GNDR	Analog	**Receiver Ground.**
131	RBIAS	Analog	**RBIAS.** Provides bias current for internal circuitry. The 100 µA bias current is provided through an external 22.1 kΩ, 1% resistor to GNDA.
27, 130	GNDA	Analog	**Analog Ground.**

Table 9. Miscellaneous Signal Descriptions

Pin	Symbol	Type[1]	Description
53	$\overline{\text{RESET}}$	Schmitt, CMOS Input, NC	**Reset.** This active Low input causes internal circuits and state machines to reset. On power-up, devices should not be brought out of reset until the power supply has stabilized and reached 4.5 V. When there are multiple devices, it is recommended that all be supplied by a common reset that is driven by an 'LS14 or similar device.
54	CLK25	Schmitt CMOS Input	**25 MHz system clock.** Drive with MOS levels.
71	$\overline{\text{FPS}}$	TTL Input	**First Position Select.** In multi-chip configurations, this pin identifies one device on each board that will drive the HOLDCOL signal to extend non-local collisions to other devices on the board. Set Low for first device on PCB. Set High for all other devices on PCB. If using a LXT983 in an LXT980-based design, Chip ID 0 of the LXT980 must be renamed $\overline{\text{FPS}}$ in the LXT983. LXT983 Chip ID 1and Chip ID 2 do not have to be tied to ground.
74	AUTO_BLINK (**LXT983A**)	TTL Input, PD	Auto_Blink. Setting this pin High disables the Blink indication (used to show a "No Link" condition) for LED Mode 1, Port*n*LED3. Note: For LXT983, refer to Table 8 on page 14.
7, 15, 23, 31, 39, 47, 48, 55, 56, 58-70, 77, 78, 81, 87, 92, 97, 98, 101, 102, 103, 190-199	N/C	-	**No Connects.** Leave these pins unconnected.

1. NC = No Clamp. Pad will not clamp input in the absence of power.
   PD = Pull Down
   TTL = Transistor-Transistor Logic

2.0 Functional Description

2.1 Introduction

As a fully integrated IEEE 802.3 repeater capable of 10 Mbps and 100 Mbps functionality, the LXT983 is a very versatile device allowing great flexibility in Ethernet design solutions. Figure 3 and Figure 4 show some typical applications, and Figure 5 shows a more complete I/O circuit. Refer to "Application Information" on page 31 for specific circuit implementations.

This multi-port repeater provides four 10BASE-T/100BASE-TX/100BASE-FX ports. In addition, there is a bidirectional Media Independent Interface (MII) expansion port which may be connected to either a 10/100 MAC, or to a 100 Mbps PHY.

The LXT983 provides two repeater state machines and two Inter-Repeater Backplanes (IRB) on a single chip—one for 10 Mbps operation and one for 100 Mbps operation. The 100 Mbps repeater fully meets IEEE 802.3 Class II requirements. Each port's operating speed may be selected independent of the other ports. The auto-negotiation capability of the LXT983 allows it to poll connected nodes and configure itself accordingly.

The segmented backplane simplifies dual-speed operation, and allows multiple devices to be stacked and function as one logical repeater.

2.1.1 TP/FX Port Configuration

The LXT983 reads the hardware configuration pins at power-up, hardware reset, or software reset (but not at repeater reset), to determine operating conditions for each of its twisted-pair (TP) and fiber (FX) ports. Each of the four media ports has its own configuration pins so that it can be individually configured. There are four possible configurations for each of the four media ports. The four possible configurations are summarized in Table 10.

Table 10. Manual Speed Selection

SPD1	SPD0	Speed Selection
0	0	Allow 10/100 auto-negotiation/parallel detection on copper media
0	1	Force port to 10BASE-T mode
1	0	Force port to 100BASE-FX mode
1	1	Force port to 100BASE-TX mode

2.1.1.1 Forced Operation

A port can be directly configured to operate in one of three modes—100FX, 100TX, or 10T. When a port is configured for forced operation, it immediately begins operating in the selected mode. Forced operation is the only way to enable 100FX operation. All links are established as half-duplex only. As a repeater, the LXT983 cannot support full-duplex operation.

2.1.1.2 Auto-Negotiation

Any port can be configured to establish its link via auto-negotiation. The port and its link partner establish link conditions by exchanging Fast Link Pulse (FLP) bursts. When auto-negotiation is enabled, the capabilities advertised by the LXT983 are predetermined and cannot be changed. The LXT983 always advertises 100 half-duplex and 10 half-duplex. It never advertises 10 or 100 full-duplex.

If the link partner does not support auto-negotiation, the LXT983 determines link state by listening for 100 Mbps IDLE symbols or 10 Mbps link pulses. If it detects either of these signals, it configures the port and updates the status registers appropriately.

2.1.1.3 Link Establishment and TP Port Connection

Once a TP port establishes link, the LXT983 automatically connects it to the appropriate repeater state machine. If link loss is detected and auto-negotiation is enabled, the port returns to the auto-negotiation state.

2.1.2 MII Port Configuration

At power-up or reset, the MII is configured via external pins to one of the three modes of operation:

- 100 Mbps, PHY side of interface—or interfacing to 100 Mbps MAC.
- 10 Mbps, PHY side of interface—for interfacing to 10 Mbps MAC.
- 100 Mbps, MAC side of interface—to drive fifth 100 Mbps port via an LXT970 or other MII-compliant PHY. In this mode, the external PHY must be configured as either a 100TX or 100FX connection.

Figure 3. Typical Managed Repeater Architectures

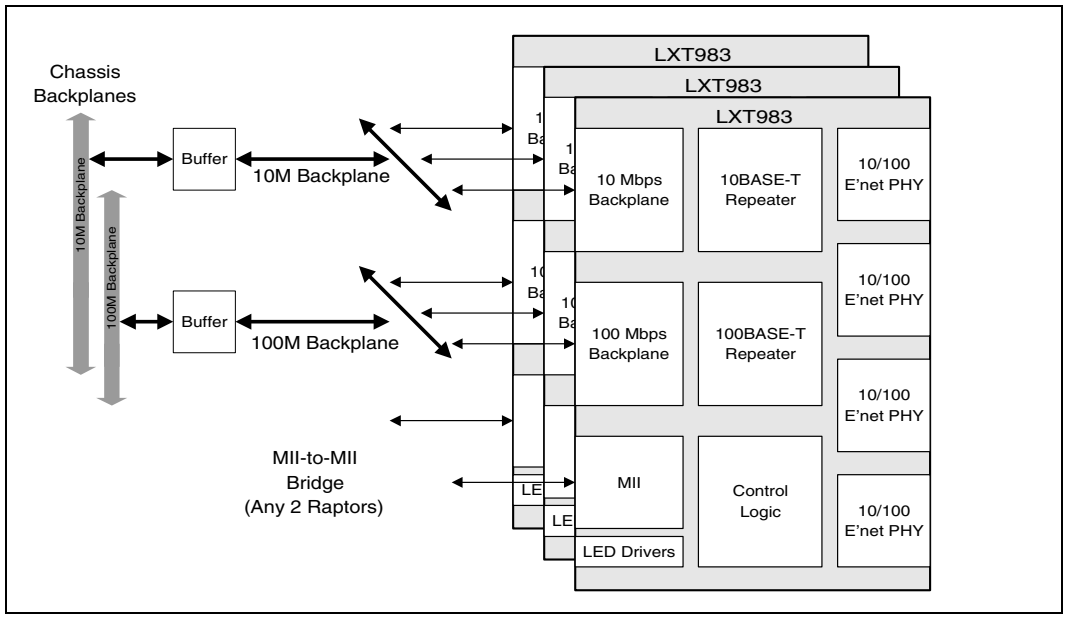
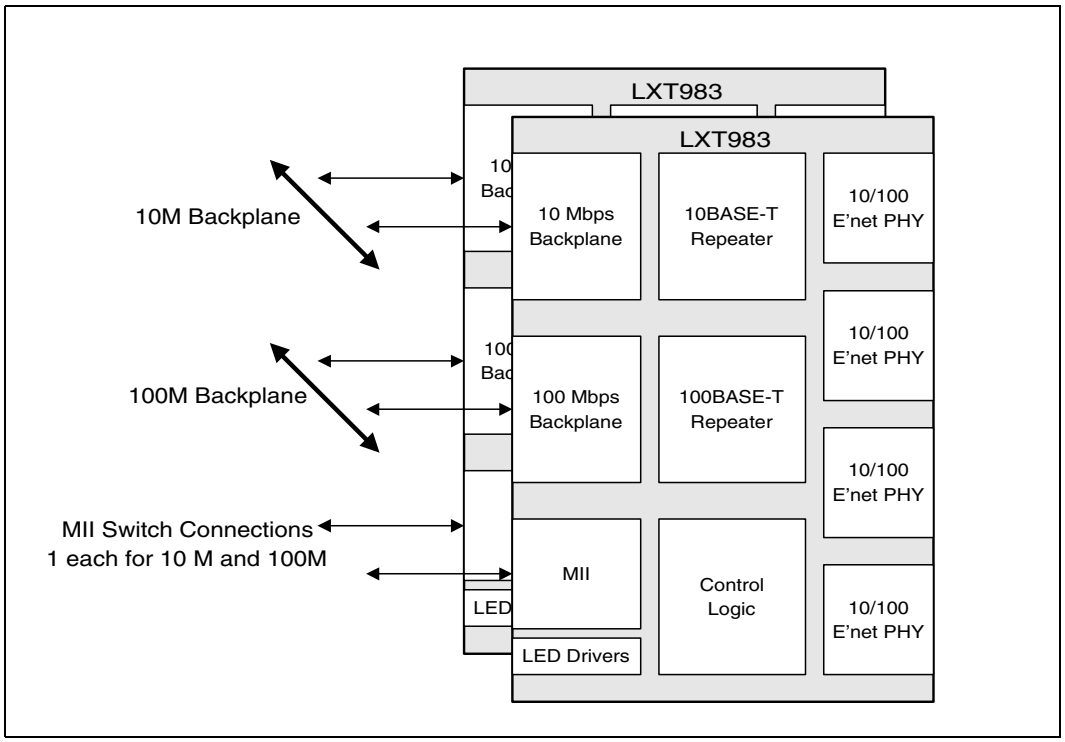


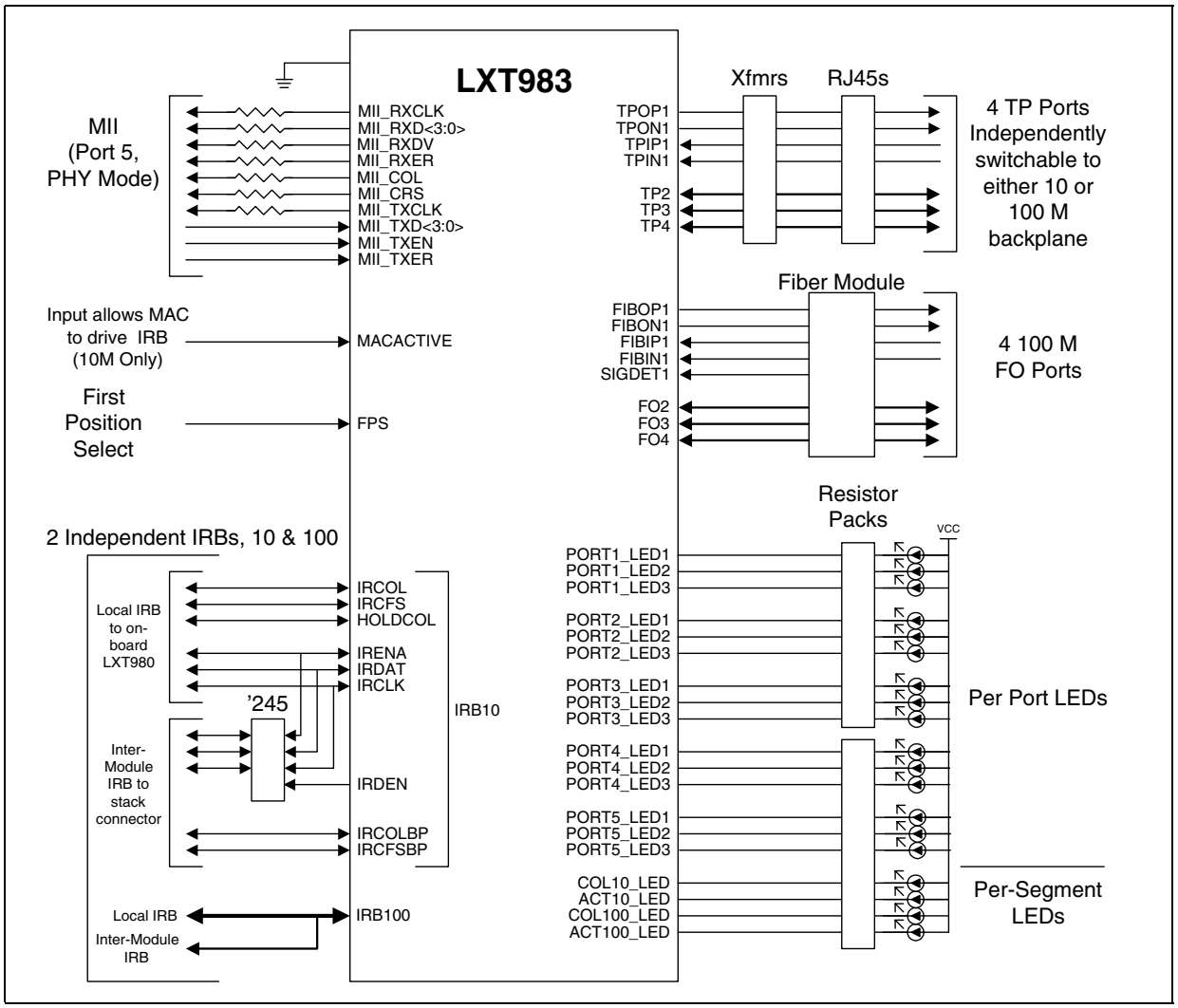
Figure 4. Typical Hybrid Switch/Repeater Application



2.1.3 Interface Descriptions

The LXT983 provides four network interface ports. Each port provides both a twisted-pair and a fiber interface. The twisted-pair interface directly supports 100BASE-TX (100TX) and 10BASE-T (10T) Ethernet applications. A common termination circuit is used for both media types. The fiber interface indirectly supports 100BASE-FX (100FX) media through a PECL connection to an external fiber-optic transceiver. Both interfaces fully comply with IEEE 802.3 standards

Figure 5. Typical Application Block Diagram



2.1.3.1 Twisted-Pair Interface

The twisted-pair interface for each port consists of two differential signal pairs—one for transmit and one for receive. The transmit signal pair is TPOP/TPON, the receive signal pair is TPIP/TPIN. The twisted-pair interface for a given port is enabled when the port configuration is set to auto-negotiate, forced 10T or forced 100TX operation. The twisted-pair interface is disabled when 100FX is selected.

The transmitter is current driven and requires magnetics with 2:1 turns ratio. A 400Ω resistive load should be placed across the TPOP/N pair, in parallel with the magnetics. The center tap of the primary side of the transmit winding must be tied to a quiet VCC for proper operation. When the twisted-pair interface is disabled, the transmitter outputs are tri-stated.

The receiver requires magnetics with a 1:1 turns ratio, and a load of 100Ω. When the twisted-pair port is enabled, the receiver actively biases its inputs to approximately 2.8 V. When the twisted-pair interface is disabled, no biasing is provided. A 4 kΩ load is always present across the TPIP/TPIN pair.

When used in 100TX applications, the LXT983 sends and receives a continuous, scrambled 125 Mbaud MLT-3 waveform. In the absence of data, IDLE symbols are sent and received to keep the link up.

When used in 10T applications, the LXT983 sends and receives a non-continuous, 10 Mbaud Manchester-encoded waveform. To maintain link during idle periods, the LXT983 sends link pulses every 16 ms, and expects to receive them every 10 to 20 ms. Each 10BASE-T port automatically detects and sends link pulses, and disables its transmitter if link pulses are not detected. Each receiver can also be configured to ignore link pulses, and leave its transmitter enabled all the time (link pulse transmission cannot be disabled). Each 10BASE-T port can detect and automatically correct for polarity reversal on the TPIP/N inputs. The 10BASE-T interface provides integrated filters using Intel's patented filter technology, which facilitate low-cost system designs meeting EMI requirements. In applications where the twisted-pair interface is not used, the inputs and outputs may be left unconnected.

2.1.3.2 Fiber Interface

Each fiber interface consists of the FIBOP/FIBON (transmit) and FIBIP/FIBIN (receive) signal pair. Each interface also provides a Signal Detect input that can be tied to the corresponding output on the fiber transceiver to determine signal presence and quality.

The transmit pair is biased to approximately 1.5V and generally must be AC-coupled to the transceiver. The receive pair will accommodate an input bias in the 2V- 5V range, and can be DC-coupled to the transceiver. Refer to Figure 13 on page 37 for a typical circuit.

The fiber interface for each port is enabled when the speed select is set to 100FX, and is disabled in all other cases. When disabled, its outputs are pulled to ground, and its inputs are tri-stated. The input and output pins on unused fiber ports may be left unconnected.

Each fiber port transmits and receives a continuous, 1V peak-to-peak, non-scrambled, NRZI waveform. The LXT983 does not support scrambling or auto-negotiation on the fiber interface.

Remote Fault Reporting

The SD pin detects signal quality and reports a remote fault if the signal quality starts to degrade. Loss of signal quality will also block any further data from being received and causes loss of the link. The remote fault code consists of 84 consecutive 1s followed by a single 0, and is transmitted at least three times. The LXT983 transmits the remote fault code and sets the associated interrupts when both of the following conditions are true:

- Fiber mode is selected.
- Signal Detect indicates no signal, or the receive PLL cannot lock.

2.1.3.3 Media Independent Interface

The LXT983 supports a standard Media Independent Interface (MII) interface. This interface can be programmed to operate as either the PHY or the MAC side of the interface.

When the MII is operating as the MAC side of the interface (MAC mode), it always operates at 100 Mbps. When the MII is operating as the PHY side of the interface (PHY mode), it can be programmed to operate either at 10 Mbps or at 100 Mbps. Once the MII is configured, the LXT983 automatically connects it to the corresponding internal repeater.

On the LXT983, the MII always operates as a nibble-wide (4B) interface. Symbol mode (5B interface) is not supported on the LXT983 MII.

Note: The MII does not auto-negotiate, auto speed select, or partition.

2.1.4 Repeater Operation

The LXT983 contains two internal repeater state machines —one operating at 10 Mbps and the other at 100 Mbps. The LXT983 automatically switches each port to the correct repeater, once the operational state of that port has been determined. Each repeater connects all ports configured to the same speed (including the MII), and the corresponding Inter-Repeater Backplane. Both repeaters perform the standard jabber, partition, and isolate functions as required.

2.1.4.1 100 Mbps Repeater Operation

The LXT983 contains a complete 100 Mbps Repeater State Machine (100RSM) that is fully IEEE 802.3 Class II compliant. Any port configured for 100 Mbps operation is automatically connected to the 100 Mbps repeater. This includes any of the four media ports if they are configured for 100TX or 100FX operation, and the MII port if it is configured for 100 Mbps operation.

The 100RSM has its own Inter-Repeater Backplane (100IRB). Multiple LXT983s can be cascaded on the 100IRB and operate as one repeater segment. Data from any port will be forwarded to any other port in the cascade. The 100IRB is a 5-bit symbol-mode interface and is designed to be stackable.

The LXT983 performs the following 100 Mbps repeater functions:

- Signal amplification, wave-shape restoration, and data-frame forwarding.
- Handling of received code violations. The LXT983 will substitute the “H” symbol for all invalid received codes.
- SOP, SOJ, EOP, EOJ delay <46BT (class II compliant).
- Collision Enforcement. During a 100M collision, the LXT983 drives a 1010 jam signal (encoded as Data 5 on TX links) to all ports until the collision ends. There is no minimum enforcement time.
- Partition. The LXT983 partitions any port participating in excess of 60 consecutive collisions or one collision approximately 575.2 µs long. Once partitioned, the LXT983 continues monitoring and transmitting to the port, but does not repeat data received from the port until it properly unpartitions.
- Un-partition. The LXT983 un-partitions a port only when data can be transmitted to the port for 450-560 bit times without a collision on that port.
- Isolate. The LXT983 will isolate any port that transmit more than two successive false carrier events. A false carrier event is defined as a packet that does not start with a /J/K symbol pair. Note: this is not the same function as the 100IRB isolate function, which involves segmenting the backplane.

- Un-isolate. The LXT983 will un-isolate a port that remains in the IDLE state for 33000 +/- 25% BT or that receives a valid frame at least 450-500BT in length.
- Jabber. The LXT983 ignores any receiver remaining active more than 57,500 bit times. The LXT983 exits this state when all jabbering receivers return to the idle condition.

The isolate and symbol error functions do not apply to the MII port.

2.1.4.2 10 Mbps Repeater Operation

The LXT983 contains a complete 10 Mbps Repeater State Machine (10RSM) that is fully IEEE 802.3 compliant. Any port configured for 10 Mbps operation is automatically connected to the 10 Mbps repeater. This includes any of the four media ports if they are configured for 10BT operation, and the MII port if it is configured for 10 Mbps operation.

The 10RSM has its own Inter-Repeater Backplane (10IRB). Multiple LXT983s can be cascaded on the 10IRB and operate as one repeater segment. Data from any port will be forwarded to any other port in the cascade. The 10IRB is 1-bit wide and runs at 10MHz. It is designed to be stackable.

The LXT983 performs the following 10 Mbps repeater functions:

- Signal amplification, wave-shape restoration, and data-frame forwarding.
- Preamble regeneration. All outgoing packets will have a minimum of 56 bits of preamble and 8 bits of SFD.
- SOP, SOJ, EOP, EOJ delays meet requirements of IEEE 802.3 section 9.5.5 and 9.5.6.
- Collision Enforcement. During a 10M collision, the LXT983 drives a jam signal (“1010”) to all ports for a minimum of 96 bit times and until the collision ends.
- Partition. The LXT983 will partition any port that participates in excess of 32 consecutive collisions. Once partitioned, the LXT983 will continue monitoring and transmitting to the port, but will not repeat data received from the port until it properly un-partitions.
- Un-partition. The LXT983 un-partitions a port when data can be either received or transmitted from the port for 450-560 bit times without a collision on that port.
- Jabber. The LXT983 will assert a minimum-IFG idle period when any port remains actively transmitting for longer than 40,000 to 75,000 bit times.

2.2 Requirements

2.2.1 Power

The LXT983 has four types of +5V power supply input pins: VCC, VCCV, VCCR, and VCCT. These inputs may be supplied from a single power supply although ferrites should be used to filter the analog and digital power planes. As a matter of good practice, these supplies should be as clean as possible. Specific operating recommendations are shown in the Test Specifications section, Table 19 on page 40.

Each supply input should be decoupled to its respective ground. Refer to Table 8 for power and ground pin assignments, and to “General Design Guidelines” on page 31 for layout guidelines.

2.2.2 Clock

A stable, external 25 MHz system clock source (CMOS) is required by the LXT983. This is connected to the CLK25 pin. Refer to Test Specifications, Table 20 on page 40, for clock input requirements.

2.2.3 Bias Current

The LXT983 requires a 22.1 kΩ, 1% resistor connecting its RBIAS input to ground.

2.2.4 Reset

At power-up, the reset input must be held Low until VCC reaches at least 4.5V. An ‘LS14 or equivalent should be used to drive reset if there are multiple LXT983 devices.

2.2.5 IRB Bus Pull-ups

Even when the LXT983 is used in a stand-alone configuration, pull-up resistors are required on the IRB signals listed below. See Figure 15 and Figure 16 for sample circuits.

100M IRB	10M IRB
IR100CFS	IR10DAT
IR100CFSBP	IR10ENA
IR100DV	IR10COL
IR100CLK	IR10CFS
	IR10COLBP
	IR10CFSBP

2.3 LED Operation

The LXT983 provides two types of LED indicators: port and segment (refer to Table 7 on page 13). Three user-selectable LED modes determine which conditions are indicated on which pins, and how particular conditions are indicated. The LED mode is selected via the LEDSEL<1:0> pins. In addition to On and Off states, some LED drivers provide a blink state output.

2.3.1 Power-Up and Reset Conditions

During reset or power-up, all LEDs turn on steady and remain on for approximately 2 seconds after reset is cleared.

2.3.2 Port LEDs

Port LEDs provide status for the four twisted-pair ports and the MII port. The LXT983 has 3 LED driver pins for each port as described in Table 7. These pins can drive standard LEDs. Three user-selectable modes are provided for the port LEDs. Port LED states are also affected by port speed and auto-negotiation status. The information conveyed by the port LED states in each mode is listed in Table 11 through Table 13.

2.3.2.1 Link Loss

During link loss, the Speed LED indicates 10M, and the Partition LED indicates "No Partition," regardless of actual partition status.

2.3.3 Segment LEDs

These outputs can directly drive LEDs to indicate activity and collision status on a per segment basis. They are not affected by LED mode selection. Pulse stretchers are used to extend the on-time for these LEDs.

2.3.3.1 Collision LEDs

The collision LEDs turn on for approximately 120 µs when the LXT983 detects a collision on the respective 10M or 100M segment. During the time that the collision LED is on, any additional collisions are ignored by the collision LED logic.

2.3.3.2 Activity LEDs

The activity LEDs turn on for approximately 4 ms when the LXT983 detects any activity on the respective 10M or 100M segment. During the time that the activity LED is on, any additional activity is ignored by the activity LED logic.

Table 11. LED Mode 1 Indications

LED	Operating Mode	On	Blink	Off
PORT*n*LED1	10 Mbps operation	Link up, not partitioned	N/A	Any other state
	100 Mbps operation	Link up, not partitioned, not isolated	N/A	Any other state
PORT*n*LED2	10 Mbps operation	N/A	N/A	Any other state
	100 Mbps operation	Link up, partitioned, or isolated	N/A	Any other state
PORT*n*LED3	Auto-neg enabled	100Mbps link up	No link (0.4s blink rate)[1]	Any other state
	Auto-neg disabled	100 Mbps link selected, link up or down	N/A	Any other state

1. Setting AUTO_BLINK (Pin 74) High disables blink (**LXT983A only**).

Table 12. LED Mode 2 Indications

LED	Operating Mode	Hardware Control		
		On	Blink	Off
PORT*n*LED1	Any	**10M:** Port enabled, link up, not partitioned **100M:** Port enabled, link up, not partitioned, and not isolated	**10M:** Port enabled, link up, and partitioned **100M:** Port enabled, link (partitioned or isolate) (slow blink)	Any other state
PORT*n*LED2 **(LXT983)**	Any	N/A	N/A	Always off
PORT*n*LED2 **(LXT983A)**	10 or 100 Mbps ops	Receive activity (20 ms pulse)	N/A	Any other state
PORT*n*LED3	Auto-neg enabled	100 Mbps link up	No link (0.4s blink rate)[1]	10 Mbps link up
	Auto-neg disabled	100 Mbps selected, link may be up or down	N/A	10 Mbps selected, link may be up or down

1. Setting AUTO_BLINK (Pin 74) High disables blink (**LXT983A only**).

Table 13. LED Mode 3 Indications

LED	Operating Mode	On	Blink	Off
PORT*n*LED1	10 Mbps operation	Link up, not partitioned	N/A	Any other state
	100 Mbps operation	Link up, not partitioned, not isolated	N/A	Any other state
PORT*n*LED2	10 or 100 Mbps operation	Receive activity (20 ms pulse)	N/A	Any other state
PORT*n*LED3	Auto-neg enabled	100M link up	No link (0.4s blink rate)[1]	10M link up
	Auto-neg disabled	100M link selected, link may be up or down	N/A	10M link selected, link may be up or down

1. Setting AUTO_BLINK (Pin 74) High disables blink (**LXT983A only**).

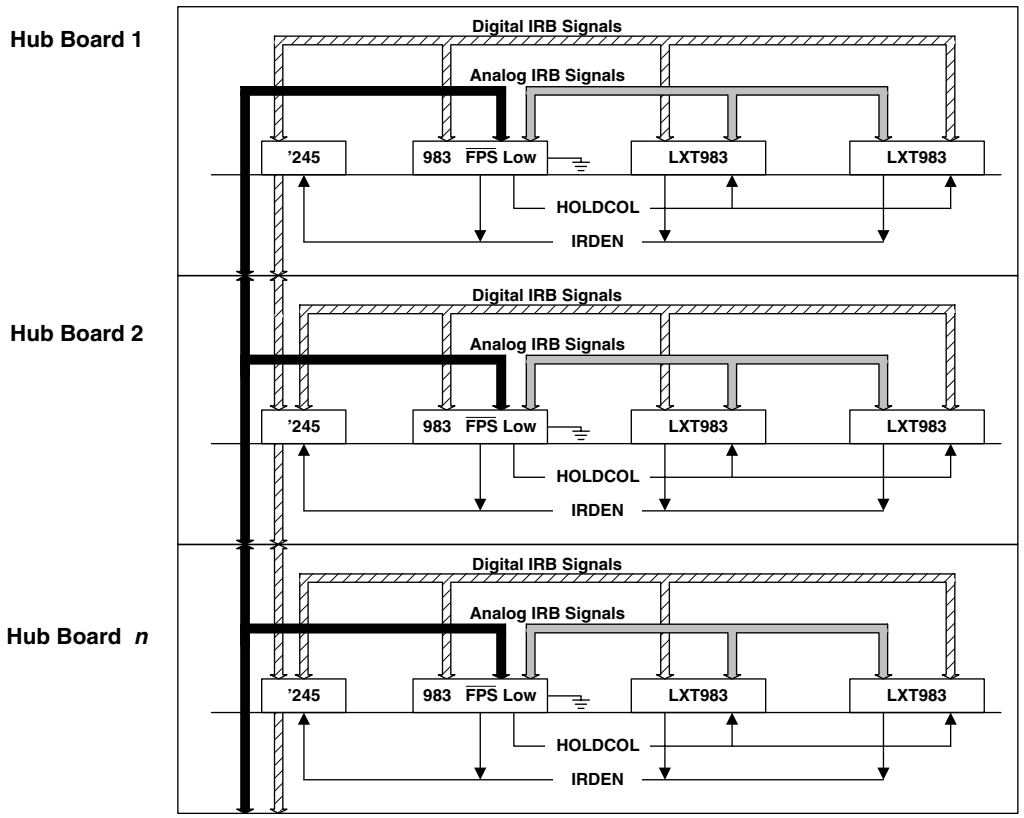
2.4 IRB Operation

The Inter Repeater Backplane (IRB) allows multiple devices to operate as a single logical repeater, exchanging data collision status information. Each segment on the LXT983 has its own complete, independent IRB. This backplane uses a combination of digital and analog signals. IRB signals can be characterized by connection type as Local (connected between devices on the same board), Stack (connected between boards) or Full (connected between devices on the same board *and* between different boards). Refer to Table 14 on page 27 and Table 15 on page 27 for details on buffering and pull-up requirements, and to Figure 15 on page 39 and Figure 16 on page 39 for application circuitry.

2.4.1 MAC IRB Access

The MACACTIVE pin allows an external MAC or other digital ASIC to interface directly to the 10 Mbps IRB. When the MACACTIVE pin is asserted, the LXT983 will drive the $\overline{\text{IR10CFS}}$ and $\overline{\text{IR10CFSBP}}$ signals on behalf of the external device, allowing it to participate in collision detection functions.

Figure 6. IRB Block Diagram



This diagram shows a single IRB. The LXT983 actually has two independent IRBs, one per speed/segment.

- Digital IRB signals include IRnDAT, IR1nDEN, IRnENA and IRnCLK.
- Local Analog IRB signals include IR100SNGL, IRnCOL and IRnCFS.
- Inter-Board Analog IRB signals include IRnCOLBP and IRnCFSBP.

  HOLDCOL is used on the 10Mbps IRB Only.

Table 14. IRB Signal Types

Connection Type	Connections Between Devices (same board)	Connections Between Boards
Full	Connect all	Connect using buffers
Local	Connect all	Do not connect
Stack	For devices with $\overline{\text{FPS}}$ High, pull-up at each device and do not interconnect.	Connect devices with $\overline{\text{FPS}}$ Low between boards. Use one pull-up resistor per stack.

Table 15. IRB Signal Details

Name	Pad Type	Buffer	Pull-up	Connection Type
100 Mbps IRB Signals				
IR100DAT<4:0>	Digital	Yes	No	Full
IR100CLK	Digital	Yes	1 kΩ	Full
$\overline{\text{IR100DV}}$	Digital, Open Drain	Yes	120Ω	Full
$\overline{\text{IR100CFS}}$	Analog	No	240Ω, 1%	Local
$\overline{\text{IR100CFSBP}}$	Analog	No	91Ω, 1%[2]	Stack
$\overline{\text{IR100COL}}$	Digital	No	No	Local
$\overline{\text{IR100SNGL}}$	Digital	No	No	Local
$\overline{\text{IR100DEN}}$	Digital, Open Drain	N/A[1]	330Ω	Local
10 Mbps IRB Signals				
IR10DAT	Digital, Open Drain	Yes	330Ω	Full
IR10CLK	Digital	Yes	No	Full
$\overline{\text{IR10ENA}}$	Digital, Open Drain	Yes	330Ω	Full
$\overline{\text{IR10CFS}}$	Analog	No	680Ω, 1%	Local
$\overline{\text{IR10CFSBP}}$	Analog	No	330Ω, 1%	Stack
$\overline{\text{IR10COL}}$	Analog	No	330Ω, 1%	Local
$\overline{\text{IR10COLBP}}$	Analog	No	330Ω, 1%	Stack
$\overline{\text{IR10DEN}}$	Digital, Open Drain	N/A[1]	330Ω	Local

1. Driver Enable signals are provided to control an external bidirectional transceiver.
2. 91Ω resistors provide greater noise immunity. Systems using 91Ω resistors are backwards stackable with systems using 100Ω resistors.

2.5 MII Port Operation

The LXT983 MII allows a MAC or PHY to directly connect into the repeater environment. The MII port (Port 5) can operate at either 10 or 100 Mbps. Utilizing two LXT983s allows the user to have a MAC interface to both the 10 and 100 Mbps segments. The LXT983 MII does *not* provide MDIO/MDC capability.

The LXT983 can emulate either the PHY (PHY Mode) or MAC (MAC Mode) side of the MII as shown in Figure 7. Mode and speed control is provided via PORT5_SPD and PORT5_SEL pins as listed in Table 16.

2.5.1 PHY Mode Operation

PHY Mode is available at both 10 and 100 Mbps. It allows the LXT983 to interface to a 10 or 100 Mbps MAC. When operating at 100 Mbps, the LXT983 passes the full 56 bits of preamble through before sending the SFD. When operating at 10 Mbps, the LXT983 sends data across the MII starting with the 8-bit SFD (no preamble bits).

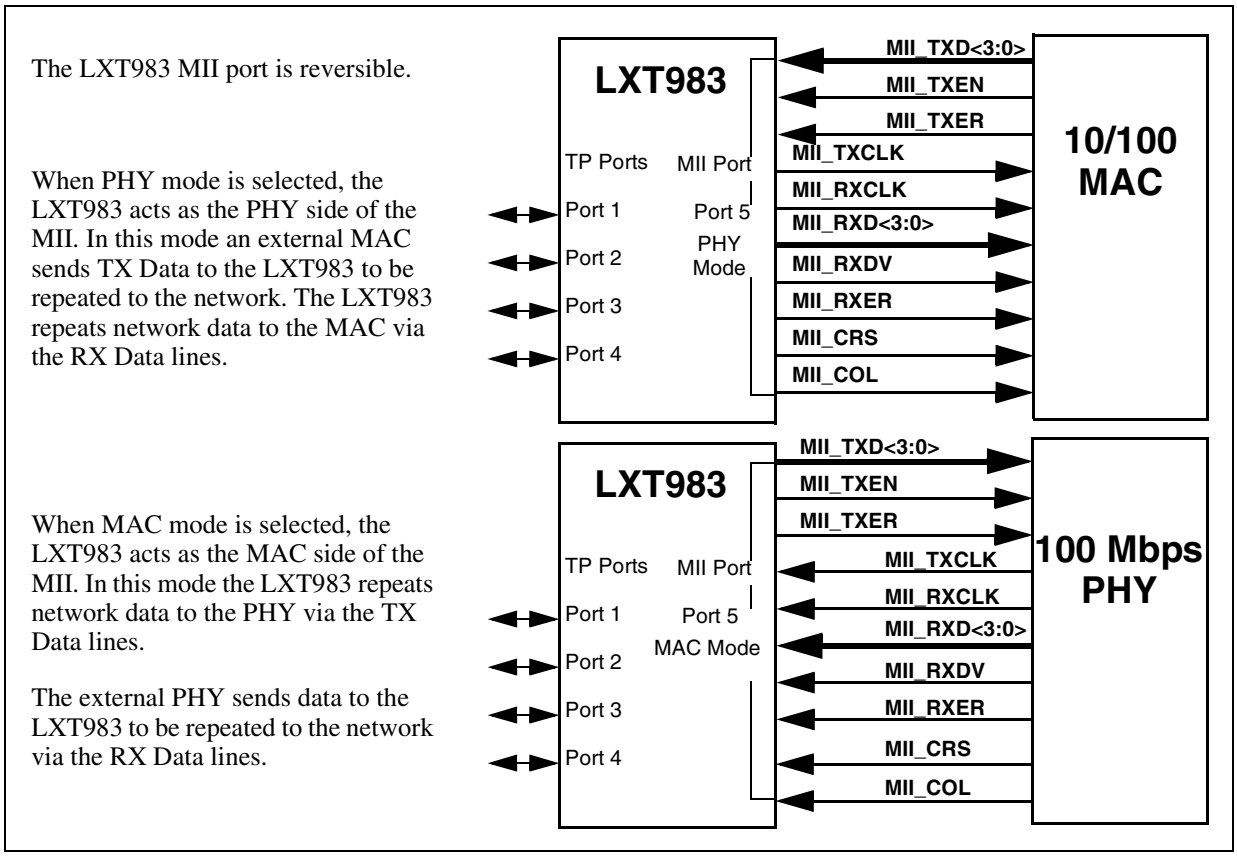
2.5.2 MAC Mode Operation

MAC Mode (available at 100 Mbps only) allows the user to attach an additional PHY to the LXT983. In this mode the PHY provides both MII_TXCLK and MII_RXCLK. The MII_TXCLK clock must be frequency-locked to the 25 MHz oscillator used by the LXT983. The LXT983 does not provide an elasticity buffer to compensate for frequency differences. When operating in MAC mode, the LXT983 generates the full 56 bits of preamble before sending the SFD across the MII.

Table 16. MII (Port 5) Mode & Speed Control

PORT5_SPD	PORT5_SEL	Speed	Mode
High	Low	100 Mbps	MAC
Low	High	10 Mbps	PHY
High	High	100 Mbps	PHY

Figure 7. MII (Port 5) Operation



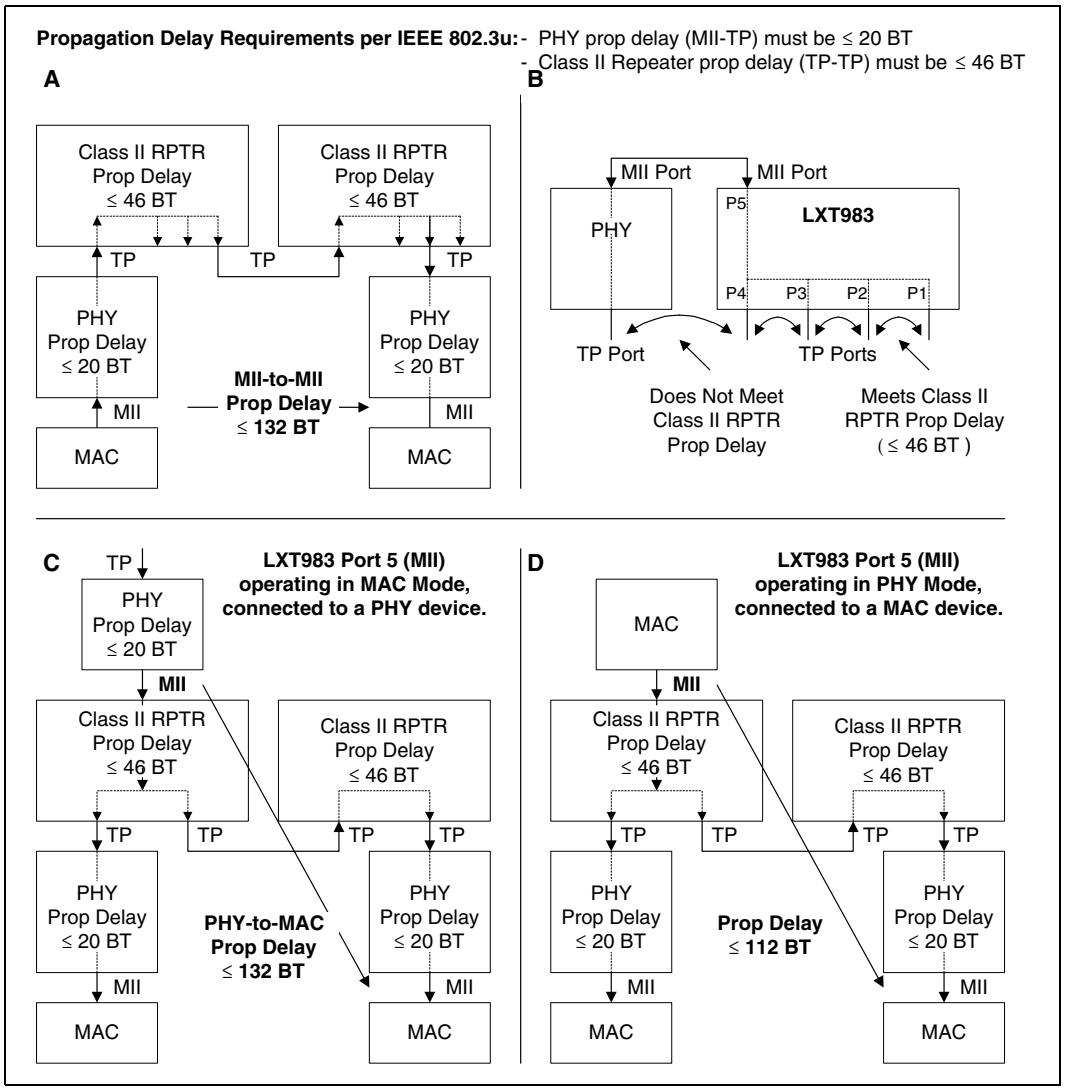
2.5.3 MII Port Timing Considerations

The IEEE 802.3u specification provides propagation delay constraints for standard PHY devices in Section 24.6, and for repeater devices in Section 27. The LXT983 MII port is a hybrid that does not fit either of these categories. The critical specification that applies to the LXT983 MII port is the overall end-to-end system propagation delay (132 bit times maximum). The LXT983 supports this requirement. Figure 8 summarizes the propagation delay issues relevant to the LXT983 MII port.

The LXT983 architecture treats the MII port as a fifth repeater port. The timing delay (latency) from the MII port to any other port meets the requirements for a Class II repeater (≤ 46 BT). It does not meet the requirements for a standard MII-PHY interface (20 - 24 BT). When operating in MAC mode with a PHY connected to the LXT983 MII port (Figure 8B), the fifth TP port does not have the latency characteristics of a Class II repeater with respect to the other ports.

With a MAC connected to the LXT983 MII port (Figure 8D), the maximum latency to any other MAC is 112 bit times (not including cable delay). The MAC connected to the LXT983 has an advantage relative to other MACs because it has one less transceiver delay.

Figure 8. MII Timing Issues



3.0 Application Information

3.1 Design Recommendations

The LXT983 has been designed to comply with IEEE requirements and to provide outstanding receive BER and long-line-length performance. Lab testing has shown that the LXT983 can perform well beyond the required distance of 100m. As with any finely crafted device, reaping the full benefits of the LXT983 requires attention to detail and good design practice.

3.1.1 General Design Guidelines

Adherence to generally accepted design practices is essential to minimize noise levels on power and ground planes. Up to 50 mV of noise is considered acceptable. 50 to 80 mV of noise is considered marginal. High-frequency switching noise can be reduced, and its effects can be eliminated, by following these simple guidelines throughout the design:

- Fill in unused areas of the signal planes with solid copper and attach them with vias to a VCC or ground plane that is not located adjacent to the signal layer.
- Use ample bulk and decoupling capacitors throughout the design (a value of. 01 µF is recommended for decoupling caps).
- Provide ample power and ground planes.
- Provide termination on all high-speed switching signals and clock lines.
- Provide impedance matching on long traces to prevent reflections.
- Route high-speed signals next to a continuous, unbroken ground plane.
- Filter and shield DC-DC converters, oscillators, etc.
- Do not route any digital signals between the LXT983 and the RJ-45 connectors at the edge of the board.
- Do not extend any circuit power or ground plane past the center of the magnetics or to the edge of the board. Use this area for chassis ground, or leave it void.

3.1.2 Power Supply Filtering

Power supply ripple and digital switching noise on the VCC plane can cause EMI problems and degrade line performance. It is generally difficult to predict in advance the performance of any design, although certain factors greatly increase the risk of having these problems:

- Poorly-regulated or over-burdened power supplies.
- Wide data busses (>32-bits) running at a high clock rate.
- DC-to-DC converters.

Many of these issues can be improved just by following good general design guidelines. In addition, Intel also recommends filtering between the power supply and the analog VCC pins of the LXT983. Filtering has two benefits. First, it keeps digital switching noise out of the analog circuitry inside the LXT983, which helps line performance. Second, if the VCC planes are laid out correctly, it keeps digital switching noise away from external connectors, reducing EMI problems.

The recommended implementation is to divide the VCC plane into two sections. The digital section supplies power to the digital VCC pin and to the external components. The analog section supplies power to VCCH, VCCT, and VCCR pins of the LXT983. The break between the two planes should run under the device. In designs with more than one LXT983, a single continuous analog VCC plane can be used to supply them all.

The digital and analog VCC planes should be joined at one or more points by ferrite beads. The beads should produce at least a 100Ω impedance at 100 MHz. The beads should be placed so that current flow is evenly distributed. The maximum current rating of the beads should be at least 150% of the current that is actually expected to flow through them. Each LXT983 draws a maximum of 500 mA from the analog supply so beads rated at 750 mA should be used. A bulk cap (2.2 -10 µF) should be placed on each side of each ferrite bead to stop switching noise from traveling through the ferrite.

In addition, a high-frequency bypass cap (.01 µf) should be placed near each analog VCC pin.

3.1.2.1 Ground Noise

The best approach to minimize ground noise is strict use of good general design guidelines and by filtering the VCC plane.

3.1.3 Power and Ground Plane Layout Considerations

Great care needs to be taken when laying out the power and ground planes. The following guidelines are recommended:

- Follow the guidelines in the *LXT980 Design and Layout Guide* for locating the split between the digital and analog VCC planes.
- Keep the digital VCC plane away from the TPOP/N and TPIP/N signals, away from the magnetics, and away from the RJ-45 connectors.
- Place the layers so that the TPOP/N and TPIP/N signals can be routed near or next to the ground plane. For EMI reasons, it is more important to shield TPOP and TPIP/N.

3.1.3.1 Chassis Ground

For ESD reasons, it is a good design practice to create a separate chassis ground that encircles the board and is isolated via moats and keep-out areas from all circuit-ground planes and active signals. Chassis ground should extend from the RJ-45 connectors to the magnetics, and can be used to terminate unused signal pairs (‘Bob Smith’ termination). In single-point grounding applications, provide a single connection between chassis and circuit grounds with a 2kV isolation capacitor. In multi-point grounding schemes (chassis and circuit grounds joined at multiple points), provide 2kV isolation to the Bob Smith termination.

3.1.4 MII Terminations

Series termination resistors are recommended on all MII signals driven by the LXT983. The proper value = nominal trace impedance minus 13Ω. If the nominal trace impedance is not known, use 55Ω.

3.1.5 The RBIAS Pin

The LXT983 requires a 22.1 kΩ, 1% resistor directly connected between the RBIAS pin and ground. Place the RBIAS resistor as close to the RBIAS pin as possible. Run an etch directly from the pin to the resistor, and sink the other side of the resistor to ground. Surround the RBIAS trace with ground; do not run high-speed signals next to RBIAS.

3.1.6 The Twisted-Pair Interface

Because the LXT983 transmitter uses 2:1 magnetics, system designers must take extra precautions to minimize parasitic shunt capacitance in order to meet return loss specifications. These steps include:

- Use compensating inductor in the output stage (Figure 14).
- Place magnetics as close as possible to the LXT983.
- Keep transmit pair traces short.
- Do not route transmit pair adjacent to a ground plane. If possible, eliminate planes under the transmit traces completely. Otherwise, keep planes 3-4 layers away.
- Some magnetic vendors are producing magnetics with higher than average return loss performance. Use of these improved magnetics increases the return loss budget available to the system designer.
- Improve EMI performance by filtering the output centertap. A single ferrite bead may be used to supply centertap current to all four ports.

In addition, follow all the standard guidelines for a twisted-pair interface:

- Route the signal pairs differentially, close together. Allow nothing to come between them.
- Keep distances as short as possible; both traces should have the same length.
- Avoid vias and layer changes as much as possible.
- Keep the transmit and receive pairs apart to avoid cross-talk.
- If possible, place entire receive termination network on one side and transmit on the other.
- Keep termination circuits close together and on the same side of the board.
- Always put termination circuits close to the source end of any circuit.
- Bypass common-mode noise to ground on the in-board side of the magnetics using 0.01 µF capacitors.

3.1.7 The Fiber Interface

The fiber interface consists of a pseudo-ECL (PECL) transmit and receive pair to an external fiber optic transceiver. The transmit pair should be AC coupled to the transceiver, and biased to 3.7V with a 50Ω equivalent impedance. The receive pair can be DC-coupled, and should be biased to 3.0V with a 50Ω equivalent impedance. Figure 13 on page 37 shows the correct bias networks to achieve these requirements.

3.1.8 Magnetics Information

The LXT980 requires a 1:1 ratio for the receive transformers and a 2:1 ratio for the transmit transformers. The transformer isolation voltage should be rated at 2 kV to protect the circuitry from static voltages across the connectors and cables. Refer to Table 17 for transformer specifications and *Magnetic Manufacturers for Networking Product Applications* (Application Note 73) for a reference list of compatible magnetic components. Before committing to a specific component, designers should test and validate the magnetics in the specific application to verify that system requirements are met.

Table 17. Magnetics Specifications

Parameter	Min	Nom	Max	Units	Test Condition
Rx turns ratio	–	1 : 1	–	–	
Tx turns ratio	–	2 : 1	–	–	
Insertion loss	0.0	–	1.1	dB	80 MHz
Primary inductance	350	–	–	µH	
Transformer isolation	–	2	–	kV	
Differential to common mode rejection	–	–	-40	dB	.1 to 60 MHz
	–	–	-35	dB	60 to 100 MHz
Return Loss - standard	–	–	-16	dB	30 MHz
	–	–	-10	dB	80 MHz
Return Loss - improved	–	–	-20	dB	30 MHz
	–	–	-15	dB	80 MHz

3.2 Typical Application Circuitry

Figure 9 and Figure 10 are simplified block diagrams showing typical applications. Figure 14 through Figure 17 show application circuitry details.

Figure 9. Unmanaged 10/100 Repeater Stack

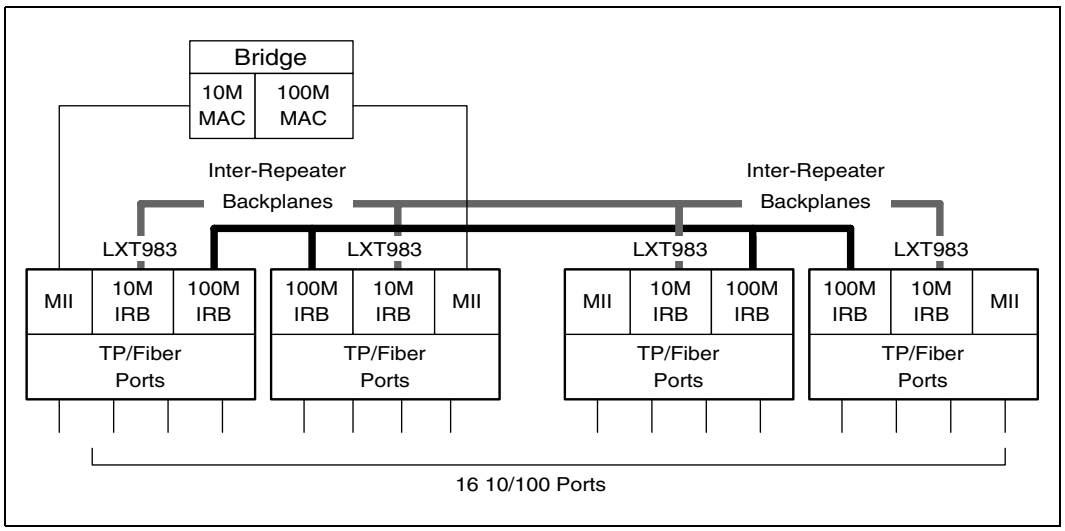


Figure 10. Hybrid Switch/Repeater Application - for Balanced 10/100 Performance

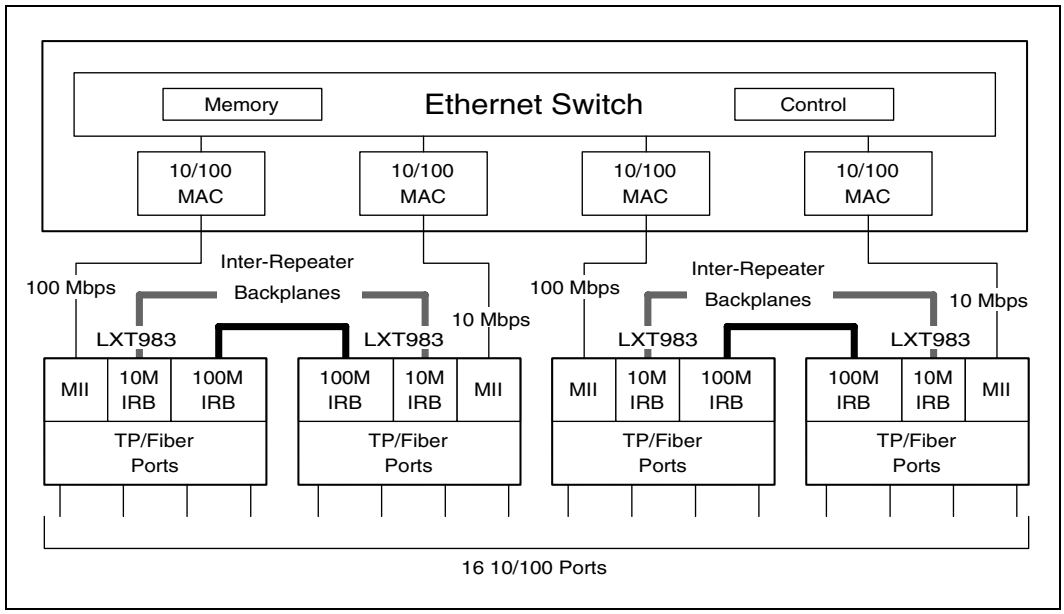


Figure 11. Hybrid Switch/Repeater Application - Weighted Toward 100M Performance

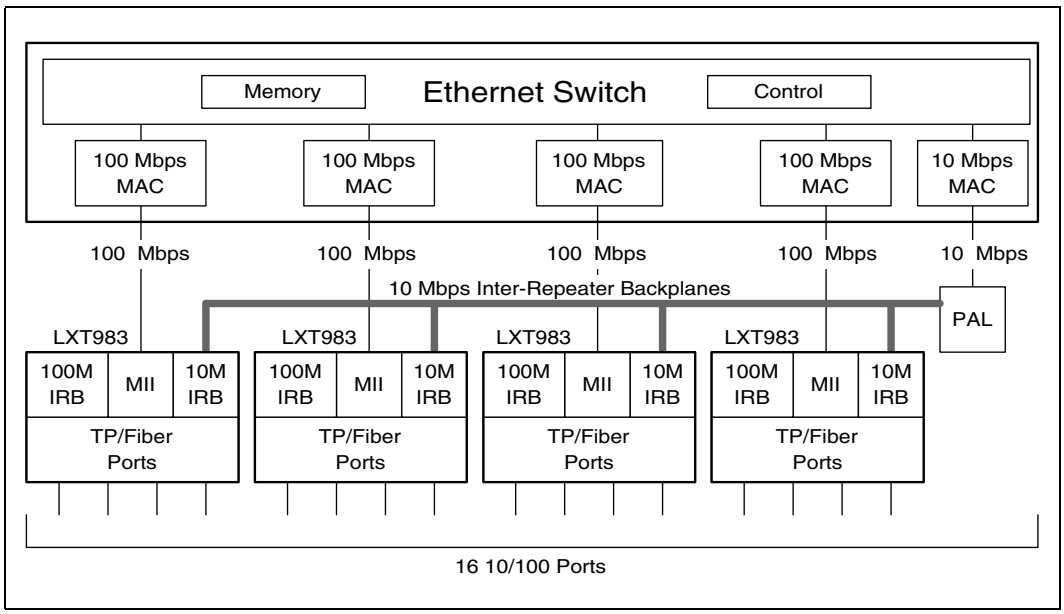


Figure 12. Power and Ground Connections

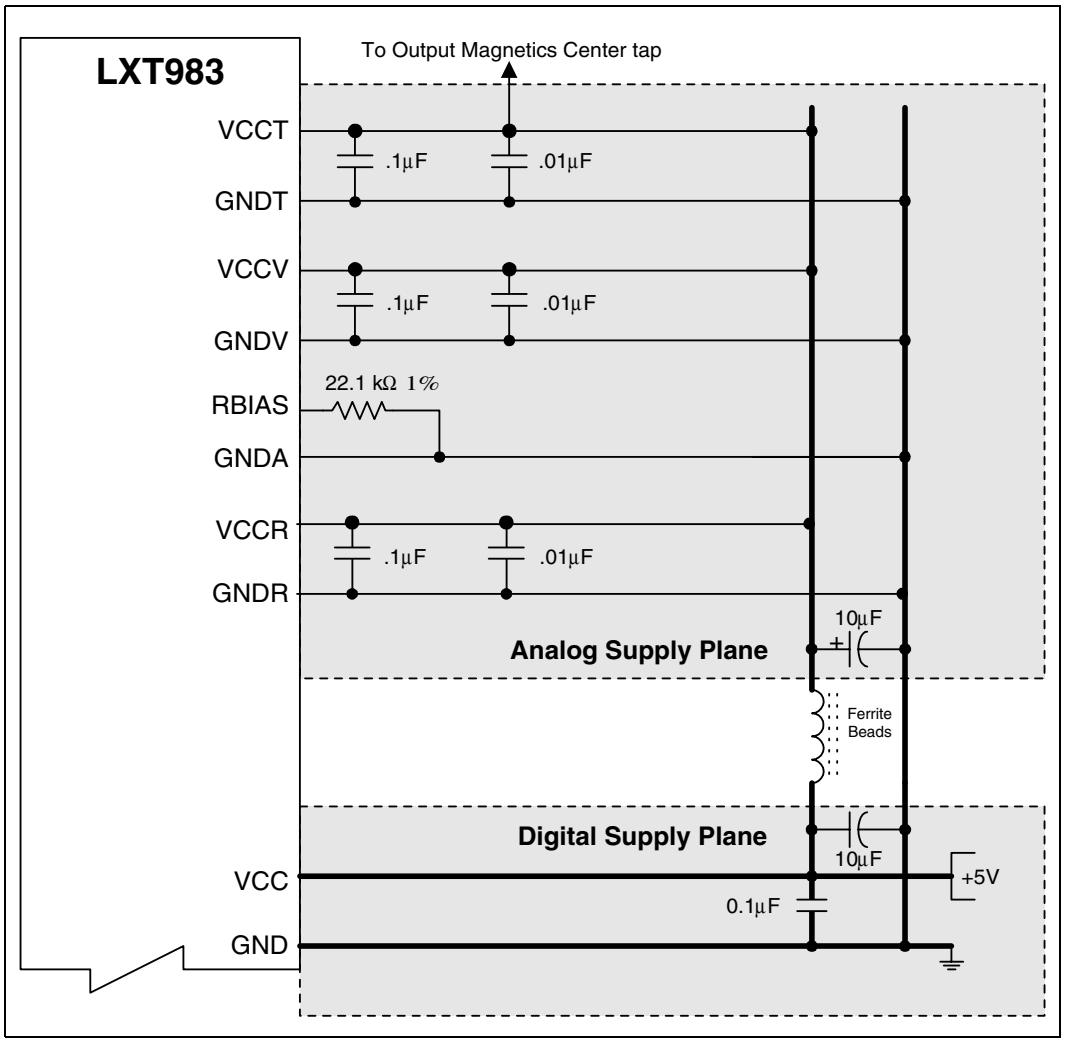


Figure 13. Typical Fiber Port Interface

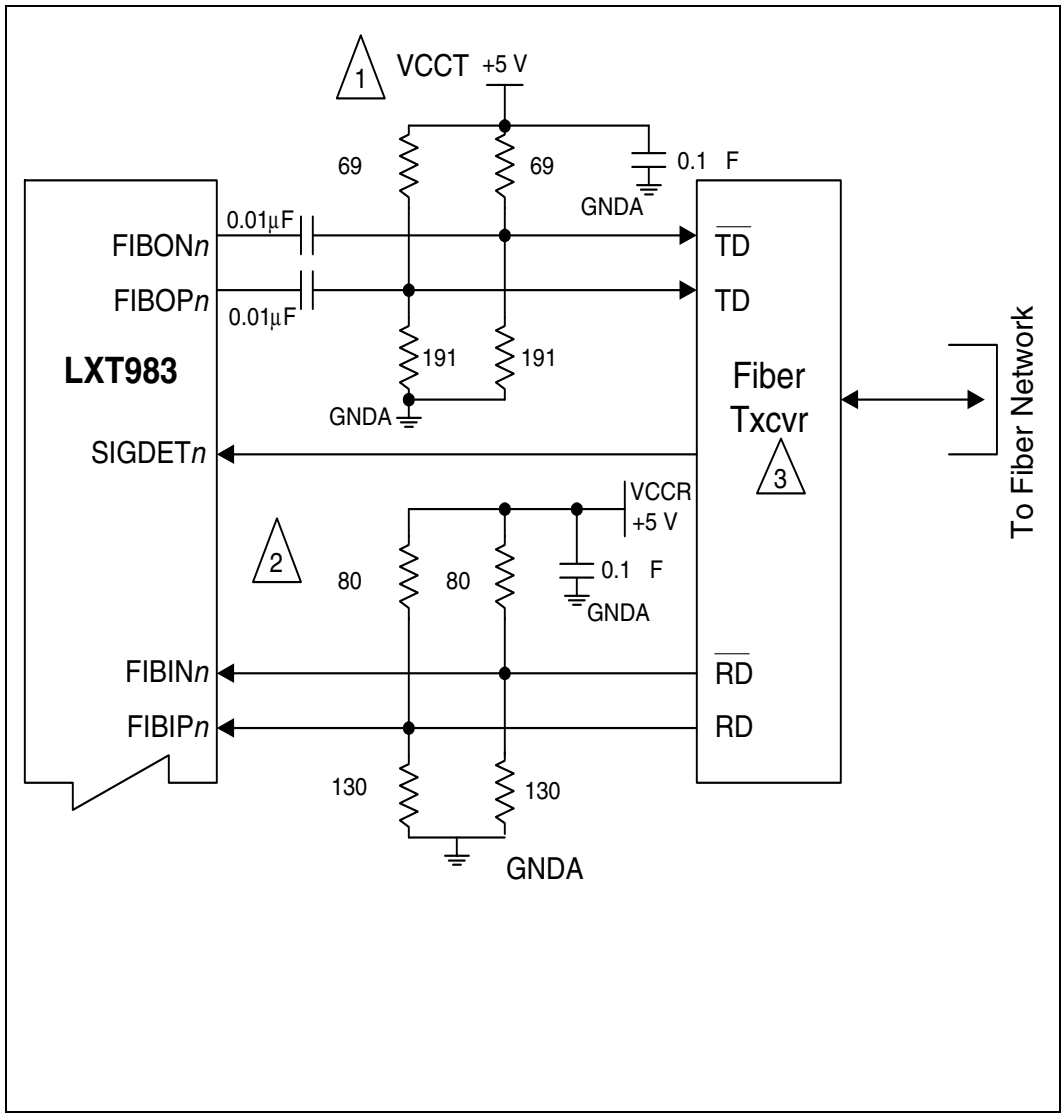
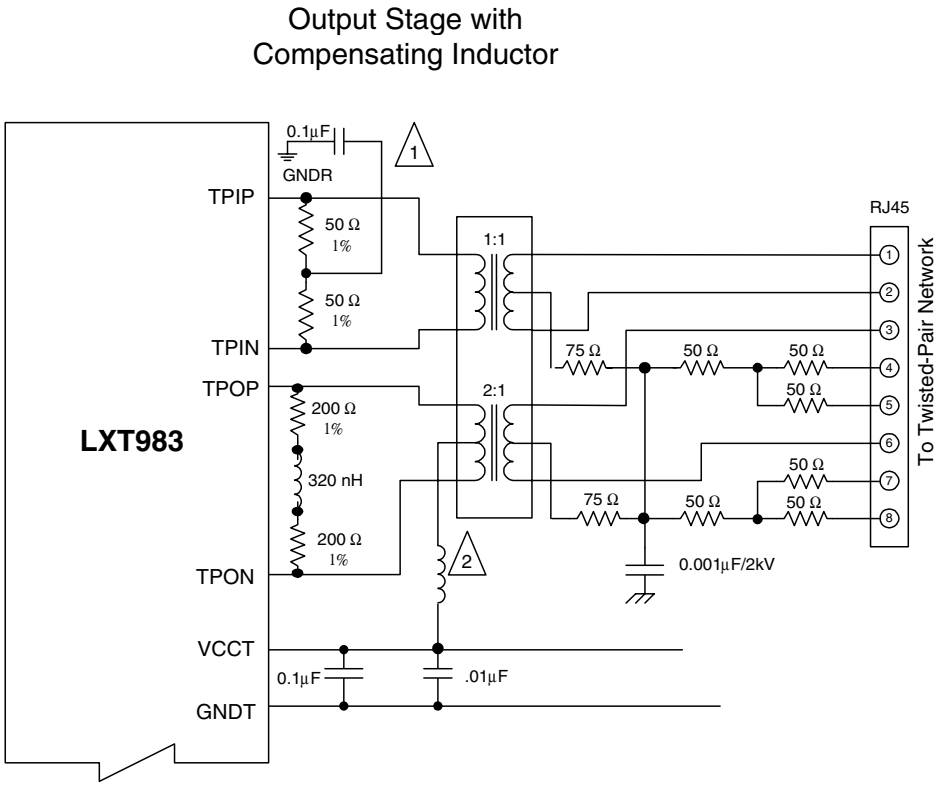
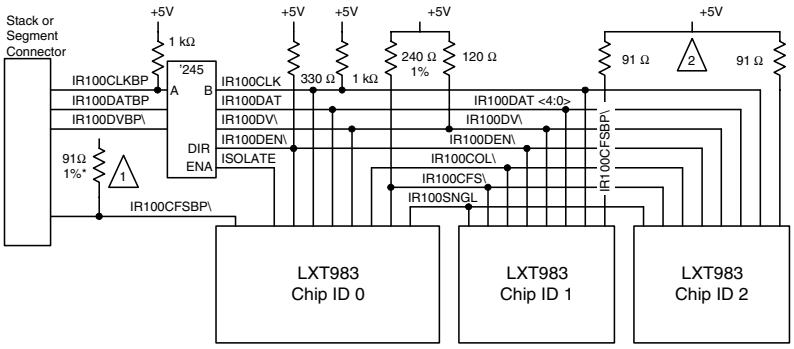


Figure 14. Typical Twisted-Pair Port Interface



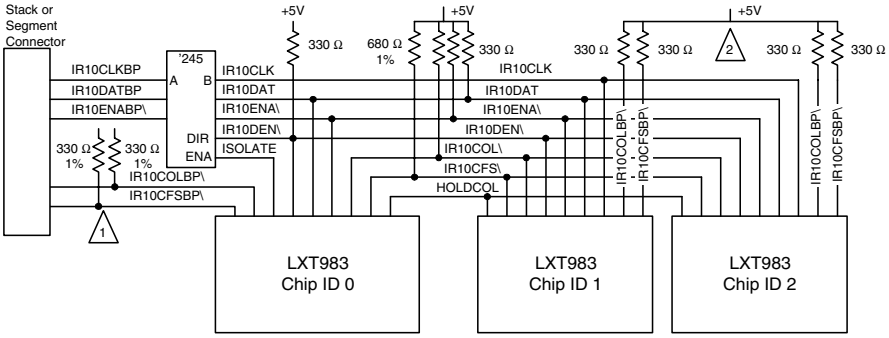
1. Receiver common mode bypass cap may improve BER performance in systems with noisy power supplies.
2. A single ferrite bead may be used to supply center tap current to all 4 ports.

Figure 15. Typical 100 Mbps IRB Implementation



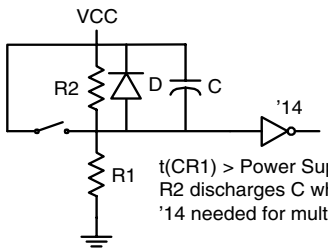
1. In stacked configurations, all devices with ChipID = 0 are tied together at $\overline{\text{IR100CFSBP}}$. The entire stack must be pulled up by only one resistor per signal. Pull-up resistor is installed in the base board only.
2. All devices with ChipID ≠ 0 require individual pull-up resistors at $\overline{\text{IR100CFSBP}}$. 91Ω resistors provide greater noise immunity. Systems using 91Ω resistors are backwards stackable with systems using 100Ω resistors.

Figure 16. Typical 10 Mbps IRB Implementation



1. In stacked configurations, all devices with ChipID = 0 are tied together at $\overline{\text{IR100CFSBP}}$ and $\overline{\text{IR10CFSBP}}$. The entire stack must be pulled up by only one resistor per signal. Pull-up resistor is installed in the base board only.
2. All devices with ChipID ≠ 0 require individual pull-up resistors at $\overline{\text{IR100CFSBP}}$ and $\overline{\text{IR10CFSBP}}$.

Figure 17. Typical Reset Circuit (983reset.vsd)



t(CR1) > Power Supply Ramp Up Time
R2 discharges C when supply goes away
'14 needed for multiple LXT983 devices.

4.0 Test Specifications

Table 18 through Figure 40 and Figure 18 through Figure 31 represent the performance specifications of the LXT983/983A. These specifications are guaranteed by test except where noted "by design." Minimum and maximum values listed in Table 20 through Table 40 apply over the recommended operating conditions specified in Table 19.

Table 18. Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Units
Supply voltage		VCC	-0.3	6	V
Operating temperature	Ambient	TOPA	-15	+80	ºC
	Case	TOPC	–	+130	ºC
Storage temperature		TST	-65	+150	ºC

Caution: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 19. Operating Conditions

Parameter		Sym	Min	Typ	Max	Units
Recommended supply voltage		VCC	4.75	5.0	5.25	V
		VCCV	4.75	5.0	5.25	V
		VCCR	4.75	5.0	5.25	V
		VCCT	4.75	5.0	5.25	V
Recommended operating temperature	Ambient	TOPA	0	–	70	°C
	Case	TOPC	0	–	115	°C
Power consumption	100BASE-TX, 4 ports active	Pc	–	–	3.5	W
	100BASE-FX, 4 ports active	Pc	–	–	3.0	W

Table 20. Input Clock Requirements

Parameter[1]	Min	Typ[2]	Max	Units
Frequency	–	25	–	MHz
Frequency Tolerance	–	–	±100	ppm
Duty Cycle	40	–	60	%

1. This table lists requirements which apply to the external clock supplied to the LXT983, not to LXT983 test specifications.
2. Typical values are at 25°C and are for design aid only. Not guaranteed and not subject to production testing.

Table 21. I/O Electrical Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Input Low voltage	VIL	–	–	0.8	V	TTL inputs
		–	–	30	% VCC	CMOS inputs [2]
		–	–	1.0	V	Schmitt triggers [3]
Input High voltage	VIH	2.0	–	–	V	TTL inputs
		70	–	–	% VCC	CMOS inputs [2]
		VCC-1.0	–	–	V	Schmitt triggers [3]
Hysteresis voltage	–	1.0	–	–	V	Schmitt triggers [3]
Output Low voltage	VOL	–	–	0.4	V	IOL = 1.6 mA
Output Low voltage (LED)	VOLL	–	–	1.0	V	IOLL = 10 mA
Output High voltage	VOH	2.4	–	–	V	IOH = 40 µA
Input Low current	IIL	-100	–	–	µA	–
Input High current	IIH	–	–	100	µA	–
Output rise / fall time	–	–	3	10	ns	CL = 15 pF

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Does not apply to IRB pins. Refer to Table 22 and Table 23 for IRB I/O characteristics.
3. Applies to RESET and CLK25 pins only.

Table 22. 100 Mbps IRB Electrical Characteristics

Parameter		Symbol	Min	Typ[1]	Max	Units	Test Conditions
Output Low voltage		VOL	–	.3	.7	V	RL = 330 Ω
Output rise or fall time		TRF	–	4	10	ns	CL = 15 pF
Input High voltage		VIH	VCC - 2.0	–	–	V	CMOS inputs
			VCC - 1.0	–	–	V	IR100CLK (Schmitt trigger)
Input Low voltage		VIL	–	–	2.0	V	CMOS inputs
			–	–	1.0		IR100CLK (Schmitt trigger)
Hysteresis voltage		–	1.0	–	–	V	IR100CLK (Schmitt trigger)
$\overline{\text{IRCFS}}$ current	single drive	–	7.0	–	9.0	mA	4. RL = 240Ω
	collision	–		–	20.5	mA	RL = 240Ω
$\overline{\text{IRCFSBP}}$ current	single drive	–	20.0	–	25.0	mA	RL = 91Ω[2]
	collision	–		–	55.0	mA	RL = 91Ω[2]
$\overline{\text{IRCFSBP}}$ voltage	single drive	–	3.4	–	4.35	V	–
	collision	–	1.4	–	1.9	V	–

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.
2. 91Ω resistors provide greater noise immunity. Systems using 91Ω resistors are backwards stackable with systems using 100Ω resistors.

Table 23. 10 Mbps IRB Electrical Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Output Low voltage	VOL	0	.1	.4	V	RL = 330 Ω
Output rise or fall time	TRF	–	4	10	ns	CL = 15 pF
Input High voltage	VIH	VCC - 2.0	–	–	V	CMOS inputs
		VCC - 2.0	–	–	V	IR10CLK (Schmitt trigger)
Input Low voltage	VIL	–	–	2.0	V	CMOS inputs
		–	–	1.0	V	IR10CLK (Schmitt trigger)
Hysteresis voltage	–	0.5	–	–	V	IR10CLK (Schmitt trigger)
$\overline{\text{IRCFS}}$ current	–	2.6	3.3	4.0	mA	RL = 680 Ω
$\overline{\text{IRCFSBP}}$ current	–	5.4	6.7	8.3	mA	RL = 330 Ω

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.

Table 24. 100BASE-TX Transceiver Electrical Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Peak differential output voltage	VP	0.95	1.0	1.05	V	Note 2
Signal amplitude symmetry	–	98	–	102	%	Note 2
Signal rise/fall time	Trf	3.0	–	5.0	ns	Note 2
Rise/fall time symmetry	Trfs	–	–	0.5	ns	Note 2
Duty cycle distortion	–	–	–	+/- 0.5	ns	Offset from 8 ns pulse width at 50% of pulse peak,
Overshoot	Vo	–	–	5	%	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Measured at line side of the transformer, line replaced by 100Ω (±1%) resistor.

Table 25. 100BASE-FX Transceiver Electrical Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Transmitter						
Peak differential output voltage (single ended)	VOP	0.6	–	1.0	V	–
Signal rise/fall time	TRF	–	–	1.6	ns	10 <-> 90 %, 2.0 pF load
Jitter (measured differentially)	–	–	–	1.3	ns	–
Receiver						
Peak differential input voltage	VIP	0.55	–	1.5	V	–
Common mode input range	VCMIR	2.25	–	VCC - 0.5	V	–
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.						

Table 26. 10BASE-T Transceiver Electrical Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Transmitter						
Peak differential output voltage	VP	2.2	2.5	2.8	V	Measured at line side of the transformer, line replaced by 100Ω (± 1%) resistor
Transmit timing jitter addition[2]	–	–	±6.4	±10	ns	0 line length for internal MAU
Transmit timing jitter added by the MAU and PLS sections[2, 3]	–	–	±3.5	±5.5	ns	After line model specified by IEEE 802.3 for 10BASE-T internal MAU
Receiver						
Receive input impedance	ZIN	–	3.4	–	kW	Between TPIP/TPIN
Differential Squelch Threshold	VDS	300	420	585	mV	5 MHz square wave input, 750 mVpp
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing. 2. Parameter is guaranteed by design; not subject to production testing. 3. IEEE 802.3 specifies maximum jitter additions at 1.5 ns for the AUI cable, 0.5 ns from the encoder, and 3.5 ns from the MAU.						

Figure 18. 100 Mbps Port-to-Port Delay Timing

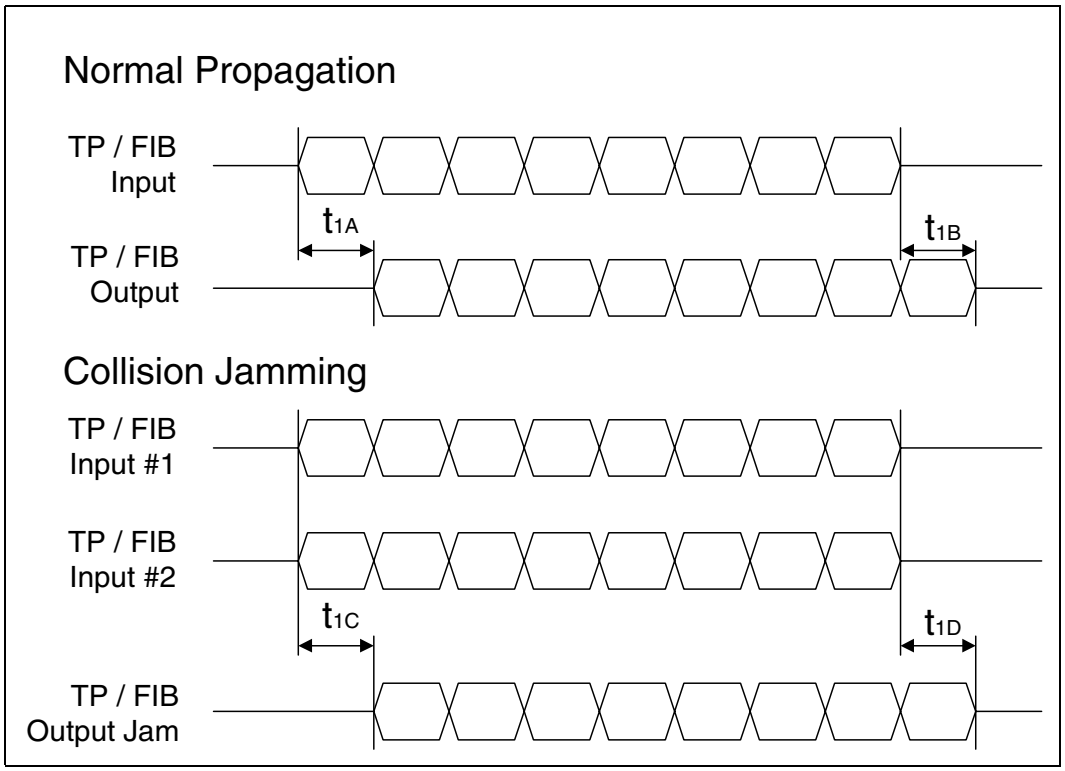


Table 27. 100 Mbps Port-to-Port Delay Timing Parameters

Parameter	Sym	Min	Typ	Max	Units[1]	Test Conditions
TPIP/N or FIBIP/N to TPOP/N or FIBOP/N, start of transmission	t_{1A}	–	–	46	BT	–
TPIP/N or FIBIP/N to TPOP/N or FIBOP/N, end of transmission	t_{1B}	–	–	46	BT	–
TPIP/N or FIBIP/N collision to TPOP/N or FIBOP/N, start of jam	t_{1C}	–	–	46	BT	–
TPIP/N or FIBIP/N idle to TPOP/N or FIBOP/N, end of jam	t_{1D}	–	–	46	BT	–

1. Bit time (BT) is defined as the duration of one bit as transferred to and from the MAC and is the reciprocal of the bit rate. The BT for 100BASE-T = 10^{-8} sec. or 10 ns.

Figure 19. 100BASE-TX Transmit Timing - PHY Mode MII

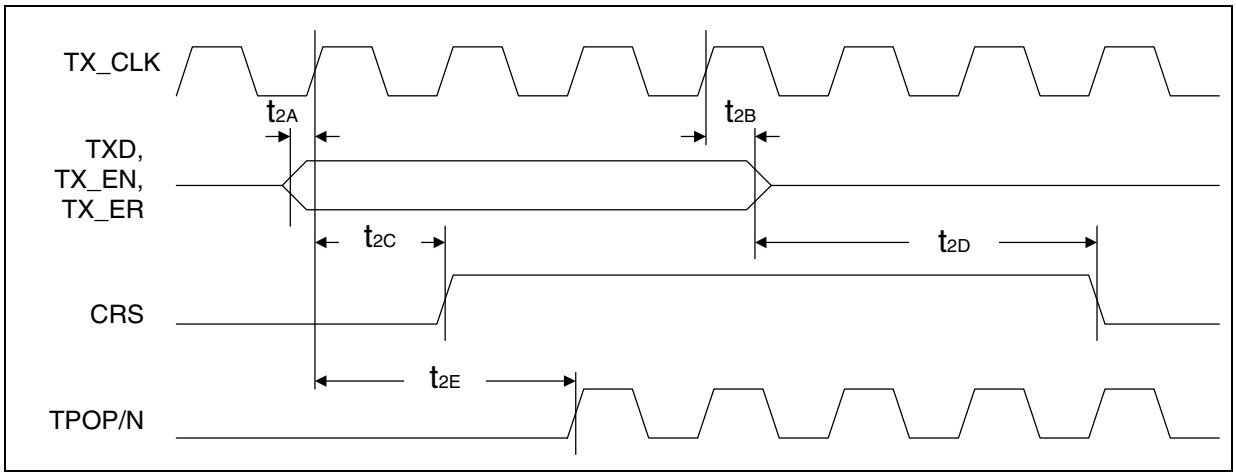


Table 28. 100BASE-TX Transmit Timing Parameters - PHY Mode MII

Parameter	Sym	Min	Typ	Max	Units[1]	Test Conditions
TXD, TX_EN, TX_ER Setup to TX_CLK High	t_{2A}	10	–	–	ns	–
TXD, TX_EN, TX_ER Hold from TX_CLK High	t_{2B}	5	–	–	ns	–
TX_EN sampled to CRS asserted	t_{2C}	0	–	4	BT	–
TX_EN sampled to CRS de-asserted	t_{2D}	0	–	16	BT	–
TX_EN sampled to TPOP/N active (Tx latency)	t_{2E}	–	–	46	BT	–

1. Bit time (BT) is defined as the duration of one bit as transferred to and from the MAC and is the reciprocal of the bit rate. The BT for 100BASE-T = 10^{-8} sec. or 10 ns.

Figure 20. 100BASE-TX Receive Timing - PHY Mode MII

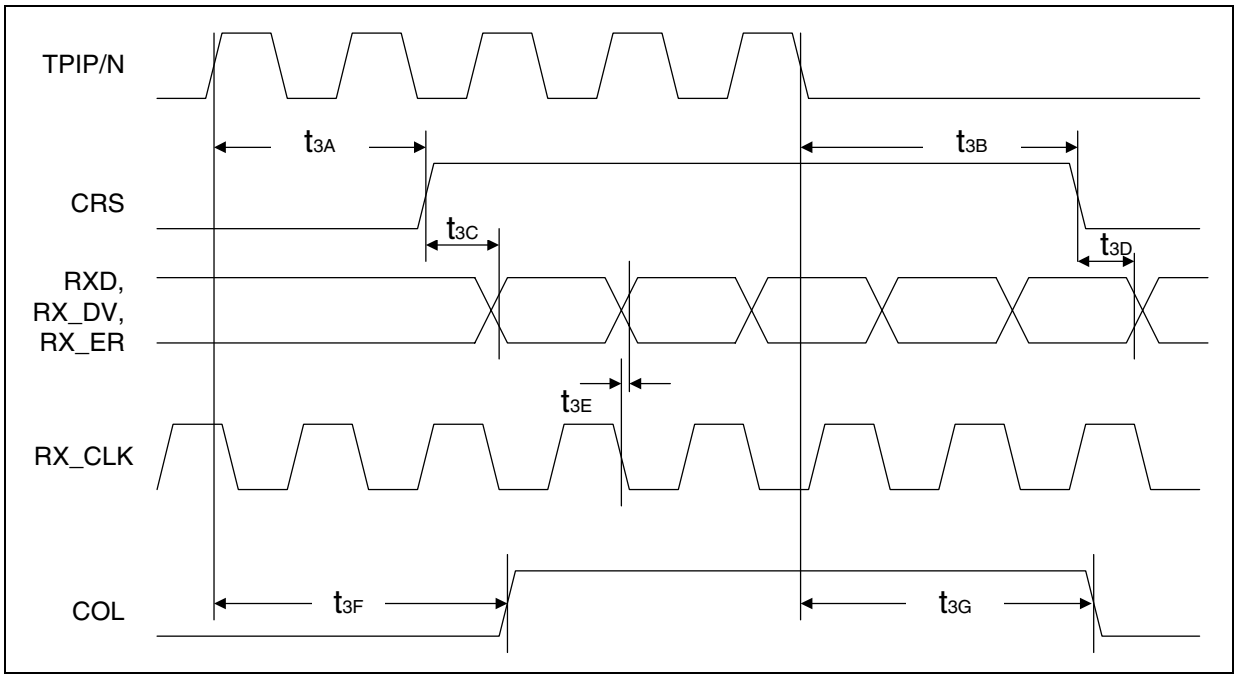


Table 29. 100BASE-TX Receive Timing Parameters - PHY Mode MII

Parameter	Sym	Min	Typ	Max	Units[1]	Test Conditions
TPIP/N in to CRS asserted	t_{3A}	–	–	46	BT	–
TPIP/N quiet to CRS de-asserted	t_{3B}	–	–	46	BT	–
CRS asserted to RXD, RX_DV, RX_ER	t_{3C}	1	–	4	BT	–
CRS de-asserted to RXD, RX_DV, RX_ER de-asserted	t_{3D}	–	–	3	BT	–
RX_CLK falling edge to RXD, RX_DV, RX_ER valid	t_{3E}	–	–	10	ns	–
TPIP/N in to COL asserted	t_{3F}	–	–	46	BT	–
TPIP/N quiet to COL de-asserted	t_{3G}	–	–	46	BT	–

1. Bit time (BT) is defined as the duration of one bit as transferred to and from the MAC and is the reciprocal of the bit rate. The BT for 100BASE-T = 10^{-8} sec. or 10 ns.

Figure 21. 100BASE-TX Transmit Timing - MAC Mode MII

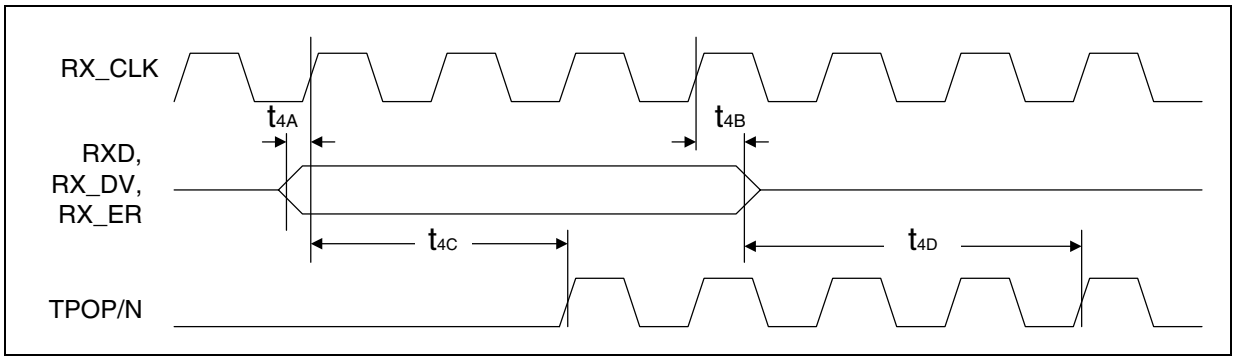


Table 30. 100BASE-TX Transmit Timing Parameters - MAC Mode MII

Parameter	Sym	Min	Typ	Max	Units[1]	Test Conditions
RXD, RX_DV, RX_ER Setup to RX_CLK High	t_{4A}	10	–	–	ns	
RXD, RX_DV, RX_ER Hold from RX_CLK High	t_{4B}	5	–	–	ns	
RXD sampled to TPO asserted	t_{4C}	–	–	46	BT	
RXD sampled to TPO de-asserted	t_{4D}	–	–	46	BT	

1. Bit time (BT) is defined as the duration of one bit as transferred to and from the MAC and is the reciprocal of the bit rate. The BT for 100BASE-T = 10^{-8} sec. or 10 ns.

Figure 22. 100BASE-TX Receive Timing - MAC Mode MII

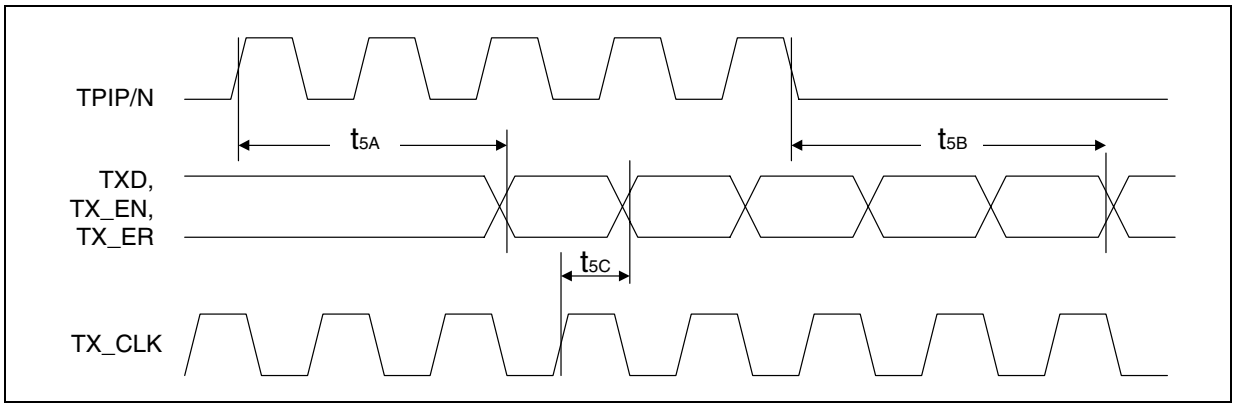


Table 31. 100BASE-TX Receive Timing - MAC Mode MII

Parameter	Sym	Min	Typ	Max	Units[1]	Test Conditions
TPIP/N in to TXD, TX_EN, TX_ER	t_{5A}	–	–	46	BT	–
TPIP/N quiet to TXD de-asserted	t_{5B}	13	–	46	BT	–
TX_CLK rising edge to TXD, TX_EN, TX_ER valid	t_{5C}	0	–	25	ns	–

1. Bit time (BT) is defined as the duration of one bit as transferred to and from the MAC and is the reciprocal of the bit rate. The BT for 100BASE-T = 10^{-8} sec. or 10 ns.

Figure 23. 100BASE-FX Transmit Timing - PHY Mode MII

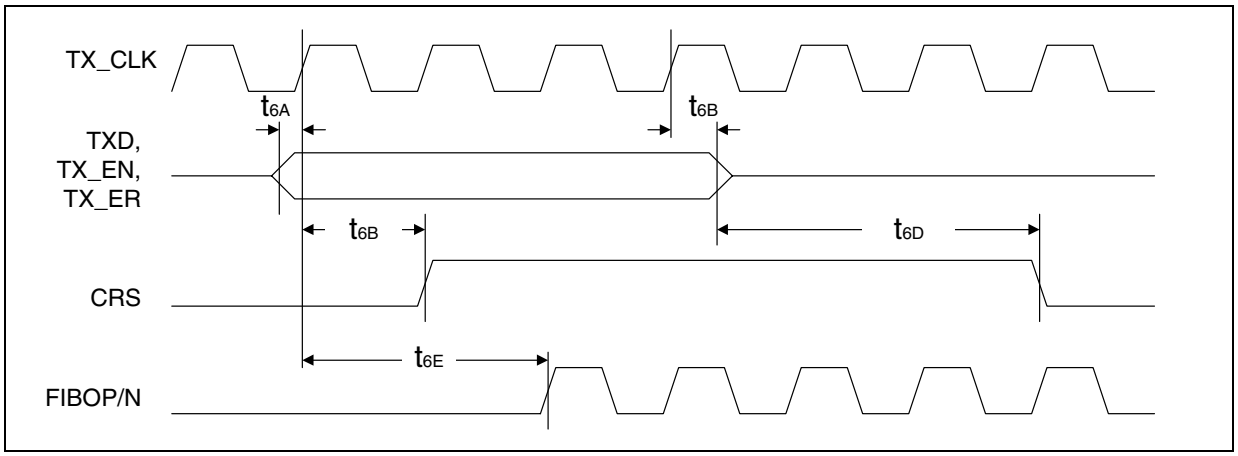


Table 32. 100BASE-FX Transmit Timing Parameters - PHY Mode MII

Parameter	Sym	Min	Typ	Max	Units[1]	Test Conditions
TXD, TX_EN, TX_ER Setup to TX_CLK High	t6A	10	–	–	ns	–
TXD, TX_EN, TX_ER Hold from TX_CLK High	t6B	5	–	–	ns	–
TX_EN sampled to CRS asserted	t6C	0	–	4	BT	–
TX_EN sampled to CRS de-asserted	t6D	0	–	16	BT	–
TX_EN sampled to FIBOP/N out (Tx latency)	t6E	–	–	46	BT	–

1. Bit time (BT) is defined as the duration of one bit as transferred to and from the MAC and is the reciprocal of the bit rate. The BT for 100BASE-T = 10^{-8} sec. or 10 ns.

Figure 24. 100BASE-FX Receive Timing - PHY Mode MII

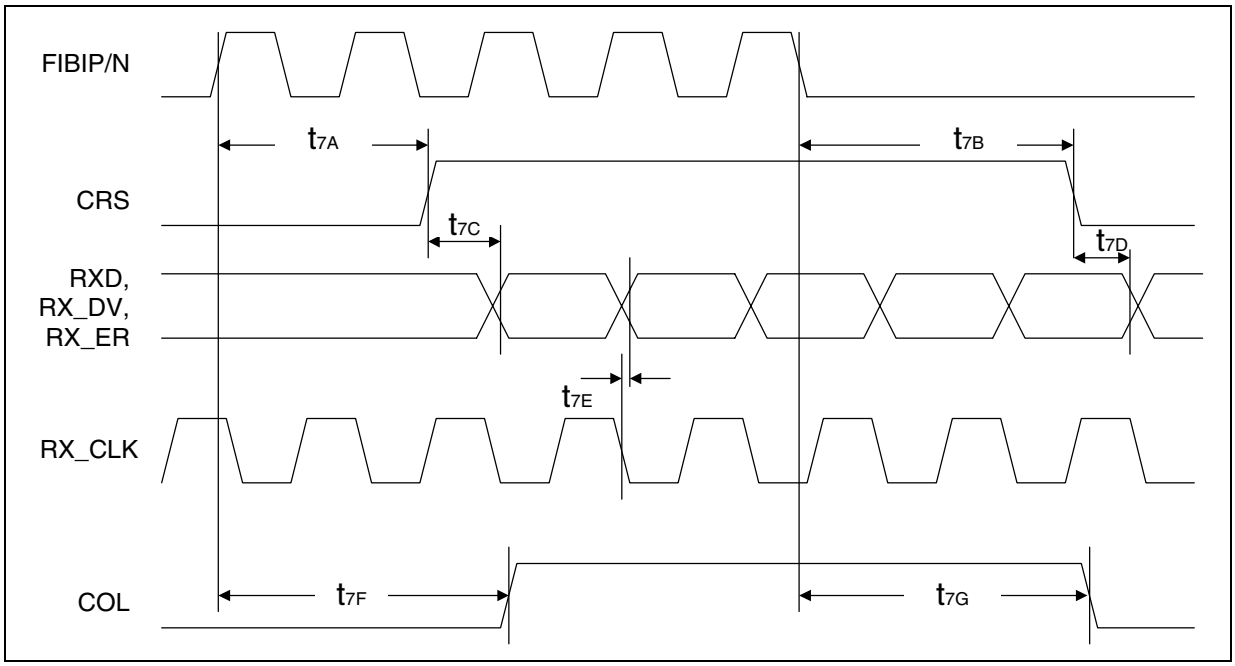


Table 33. 100BASE-FX Receive Timing - PHY Mode MII

Parameter	Sym	Min	Typ	Max	Units[1]	Test Conditions
FIBIP/N in to CRS asserted	t_{7A}	–	–	46	BT	–
FIBIP/N quiet to CRS de-asserted	t_{7B}	–	–	46	BT	–
CRS asserted to RXD, RX_DV, RX_ER	t_{7C}	1	–	4	BT	–
CRS de-asserted to RXD, RX_DV, RX_ER de-asserted	t_{7D}	–	–	3	BT	–
RX_CLK falling edge to RXD, RX_DV, RX_ER valid	t_{7E}	–	–	10	ns	–
FIBIP/N in to COL asserted	t_{7F}	–	–	46	BT	–
FIBIP/N quiet to COL de-asserted	t_{7G}	–	–	46	BT	–

1. Bit time (BT) is defined as the duration of one bit as transferred to and from the MAC and is the reciprocal of the bit rate. The BT for 100BASE-T = 10^{-8} sec. or 10 ns.

Figure 25. 100BASE-FX Transmit Timing - MAC Mode MII

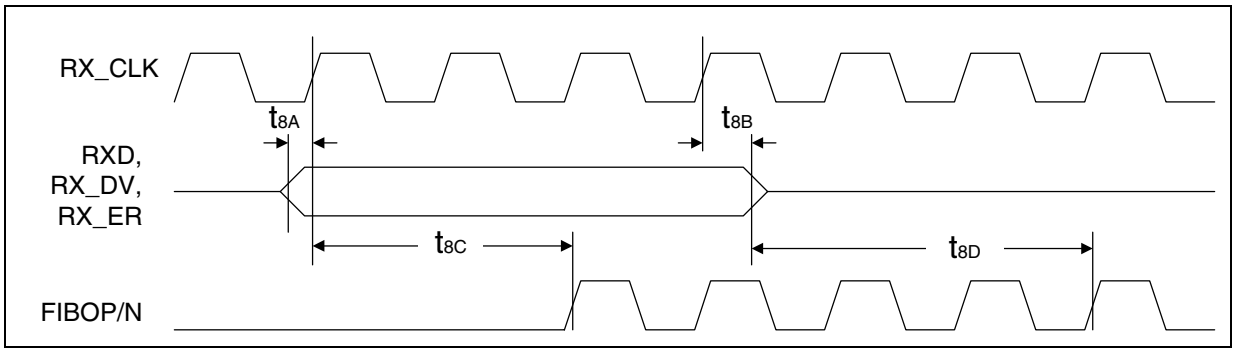


Table 34. 100BASE-FX Transmit Timing - MAC Mode MII

Parameter	Sym	Min	Typ	Max	Units[1]	Test Conditions
RXD, RX_DV, RX_ER Setup to RX_CLK High	t8A	10	–	–	ns	–
RXD, RX_DV, RX_ER Hold from RX_CLK High	t8B	5	–	–	ns	–
RXD sampled to FIBOP/N asserted	t8C	–	–	46	BT	–
RXD sampled to FIBOP/N de-asserted	t8D	–	–	46	BT	–

1. Bit time (BT) is defined as the duration of one bit as transferred to and from the MAC and is the reciprocal of the bit rate. The BT for 100BASE-T = 10^{-8} sec. or 10 ns.

Figure 26. 100BASE-FX Receive Timing - MAC Mode MII

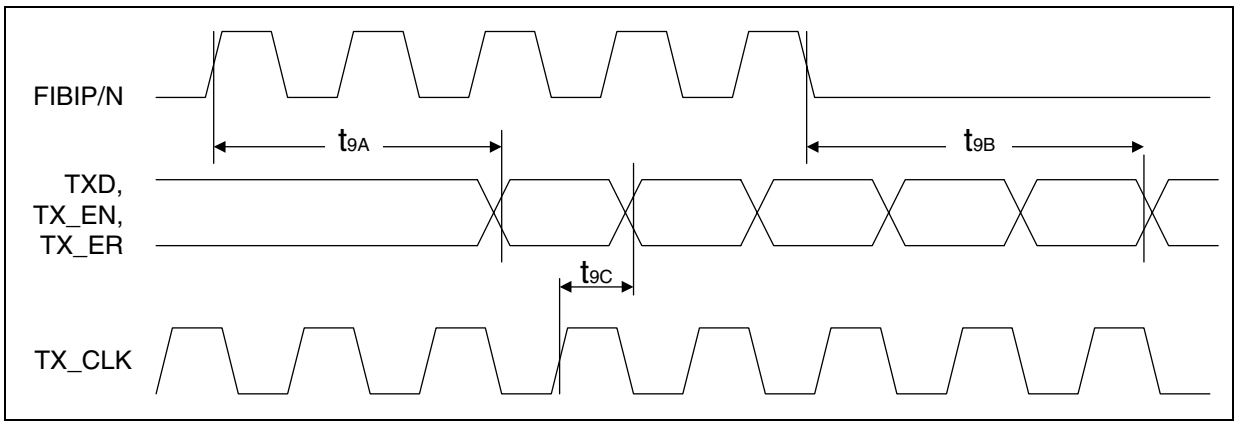


Table 35. 100BASE-FX Receive Timing - MAC Mode MII

Parameter	Sym	Min	Typ	Max	Units[1]	Test Conditions
FIBIP/N in to TXD, TX_EN, TX_ER	t9A	–	–	46	BT	–
FIBIP/N quiet to TXD de-asserted	t9B	–	–	46	BT	–
TX_CLK rising edge to TXD, TX_EN, TX_ER valid	t9C	0	–	25	ns	–

1. Bit time (BT) is defined as the duration of one bit as transferred to and from the MAC and is the reciprocal of the bit rate. The BT for 100BASE-T = 10^{-8} sec. or 10 ns.

Figure 27. 10BASE-T Transmit Timing - PHY Mode MII

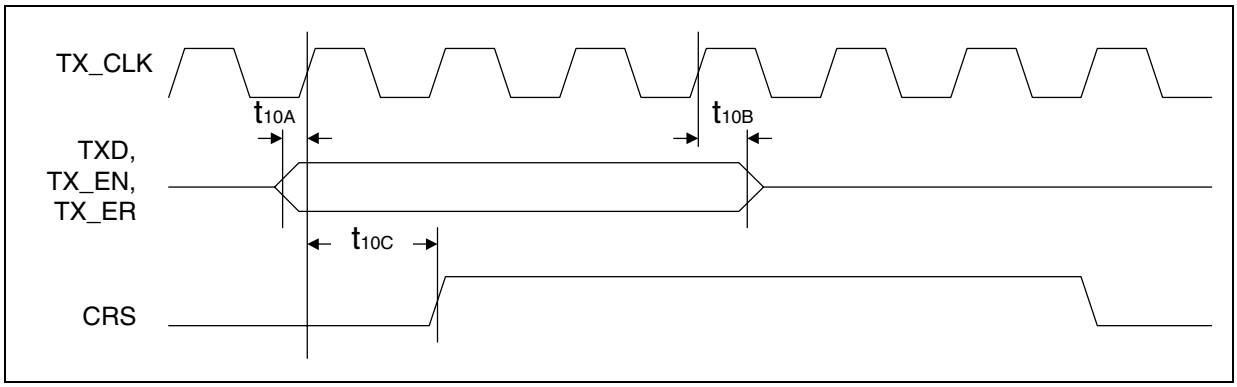


Table 36. 10BASE-T Transmit Timing Parameters - PHY Mode MII

Parameter	Sym	Min	Typ[1]	Max	Units[2]	Test Conditions
Note: TXD, TX_EN, TX_ER Setup to TX_CLK High	t_{10A}	10	–	–	ns	–
Note: TXD, TX_EN, TX_ER Hold from TX_CLK High	t_{10B}	5	–	–	ns	–
Note: TX_EN sampled to CRS asserted	t_{10C}	0	.9	2	BT	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit time (BT) is defined as the duration of one bit as transferred to and from the MAC and is the reciprocal of the bit rate. For 10BASE-T, the bit time is 10^{-7} sec. or 100 ns.

Figure 28. 10BASE-T Receive Timing - PHY Mode MII

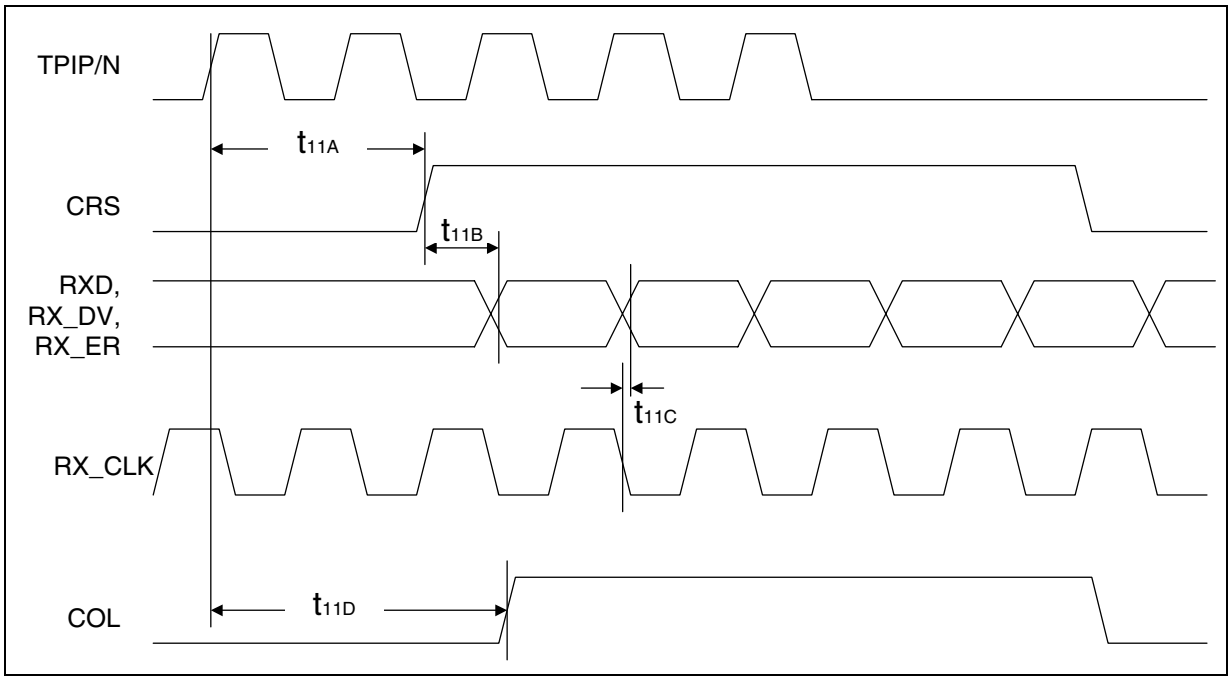


Table 37. 10BASE-T Receive Timing Parameters - PHY Mode MII

Parameter	Sym	Min	Typ[1]	Max	Units[2]	Test Conditions
TPIP/N in to CRS asserted	t_{11A}	5	6.6	8	BT	–
CRS asserted to RXD, RX_DV, RX_ER	t_{11B}	70	76	84	BT	–
RX_CLK falling edge to RXD, RX_DV, RX_ER valid	t_{11C}	–	–	10	ns	–
TPIP/N in to COL asserted	t_{11D}	6	7.4	9	BT	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit time (BT) is defined as the duration of one bit as transferred to and from the MAC and is the reciprocal of the bit rate. For 10BASE-T, the bit time is 10^{-7} sec. or 100 ns.

Figure 29. 100 Mbps IRB Timing

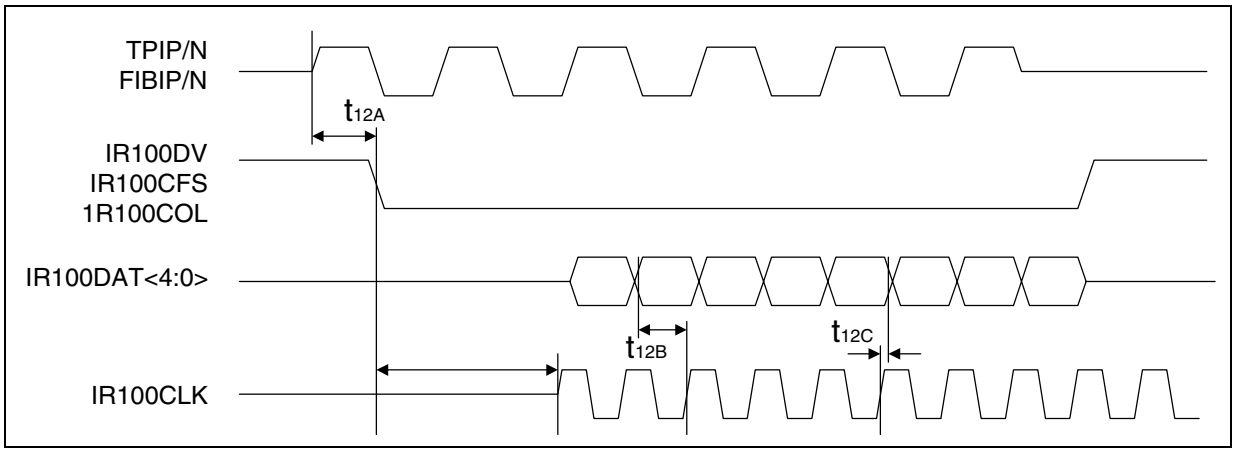


Table 38. 100 Mbps IRB Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units[2]	Test Conditions
TPIP/N or FIBP/N to $\overline{\text{IR100DV}}$ Low	t_{12A}	18	24	30	BT	–
IR100DAT to IR100CLK setup time.	t_{12B}	–	10	–	ns	–
IR100DAT to IR100CLK hold time.	t_{12C}	–	0	–	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit time (BT) is defined as the duration of one bit as transferred to and from the MAC and is the reciprocal of the bit rate. For 100BASE-T, the bit time is 10^{-8} sec. or 10 ns.

Figure 30. 10 Mbps IRB Receive Timing

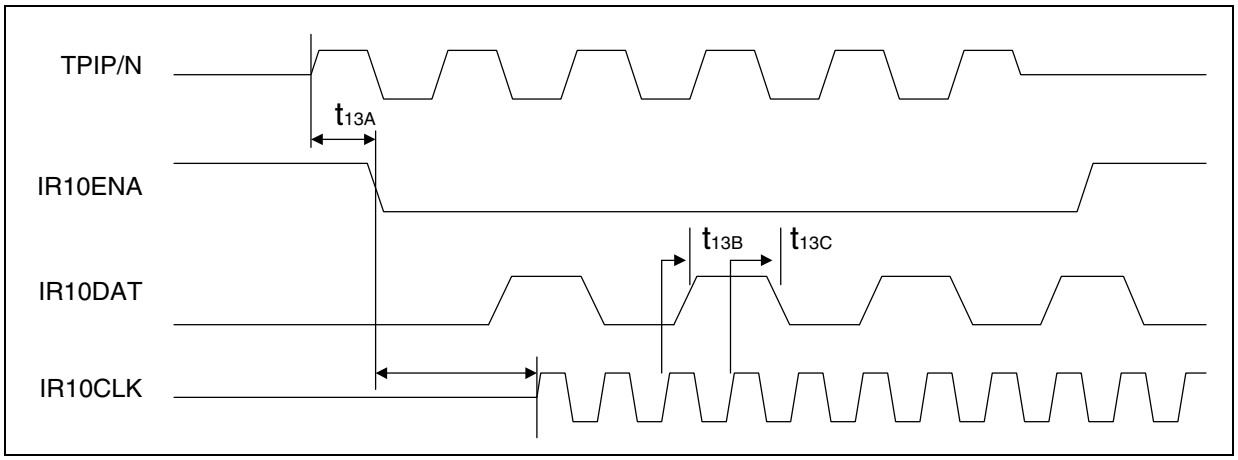


Table 39. 10 Mbps IRB Receive Timing Parameters[1]

Parameter	Symbol	Min	Typ[2]	Max	Units[4]	Test Conditions
TPIP/N to $\overline{\text{IR10ENA}}$ Low	t_{13A}	3	5.1	7	BT	–
IR10CLK rising edge to IR10DAT rising edge.[3]	t_{13B}	25	-	55	ns	330 Ω pullup, 150 pF load on IR10DAT. 1 kΩ pullup, 150 pF load on IRCLK. All measurements at 2.5V.
IR10CLK rising edge to IR10DAT falling edge.	t_{13C}	5	20	–	ns	

1. This table contains propagation delays from the TP ports to the IRB for normal repeater operation. All values in this table are output timings.
2. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
3. There is a delay of approximately 13 to 16 bit times between the assertion of $\overline{\text{IR10ENA}}$ and the assertion of IR10CLK and IR10DAT. This delay does not affect repeater operation because downstream devices begin generating preamble as soon as $\overline{\text{IR10ENA}}$ is asserted.
4. Bit time (BT) is defined as the duration of one bit as transferred to and from the MAC and is the reciprocal of the bit rate. For 10BASE-T, the bit time is 10^{-7} sec. or 100 ns.

Figure 31. 10 Mbps IRB Transmit Timing

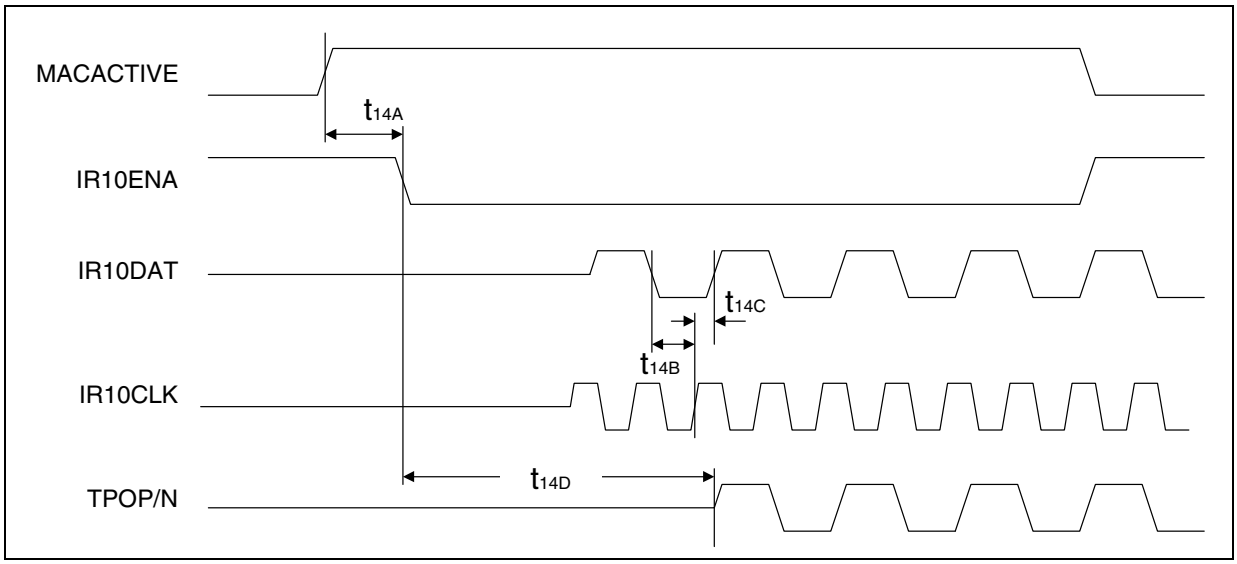


Table 40. 10 Mbps IRB Transmit Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units[2]	Test Conditions
MACACTIVE to $\overline{\text{IR10ENA}}$ assertion delay [3]	t_{14A}	–	100	–	ns	MACACTIVE High to $\overline{\text{IR10ENA}}$ Low [4]
IR10DAT (input) to IR10CLK setup time	t_{14B}	–	20	–	ns	IR10DAT valid to IR10CLK rising edge[4]
IR10CLK to IR10DAT (input) hold time	t_{14C}	–	0	–	ns	IR10CLK rising edge to IR10DAT change [4]
$\overline{\text{IR10ENA}}$ asserted to TPOP/N active	t_{14D}	5	5.1	6	BT	–

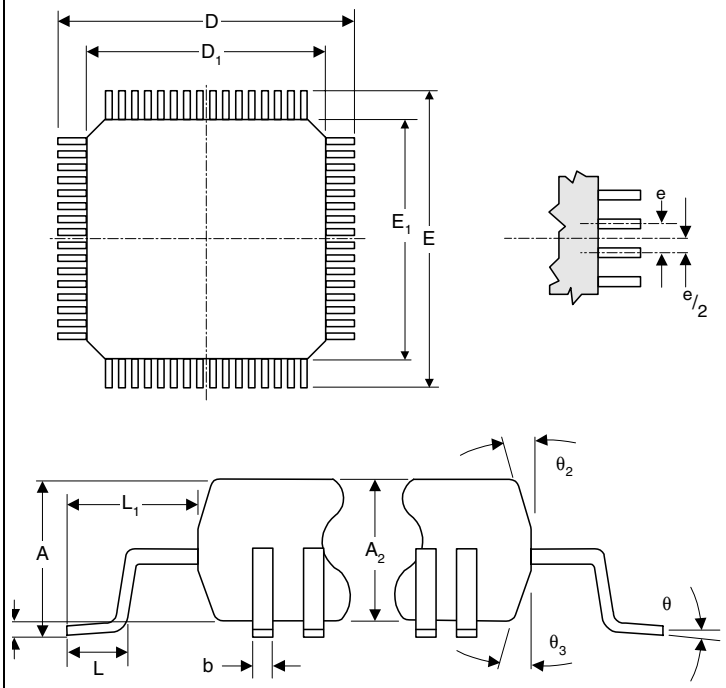
1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.
2. Bit time (BT) is defined as the duration of one bit as transferred to and from the MAC and is the reciprocal of the bit rate. For 10BASE-T, the bit time is 10^{-7} sec. or 100 ns.
3. External devices should allow at least one 10 MHz clock cycle (10 ns) between assertion of MACACTIV and $\overline{\text{IR10ENA}}$.
4. Input

5.0 Mechanical Specifications

Figure 32. LXT983 Package Specifications

208-Pin Plastic Quad Flat Package

- Part Number
  - LXT983QC
  - LXT983AHC
- Commercial Temperature Range (0°C to 70°C)



Dim	Millimeters	
	Min	Max
A	-	4.10
A1	0.25	-
A2	3.20	3.60
b	0.17	0.27
D	30.30	30.90
D_1	27.70	28.30
E	30.30	30.90
E_1	27.70	28.30
e	.50 BASIC	
L	0.50	0.75
L_1	1.30 REF	
q	0°	7°
θ_2	5°	16°
θ_3	5°	16°