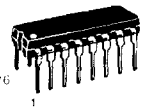
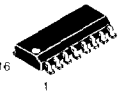
MC26C31

Product Preview

Quad EIA-422-A Line Driver
CMOS



P SUFFIX
PLASTIC DIP
CASE 648



D SUFFIX
SOG PACKAGE
CASE 751B

ORDERING INFORMATION

MC26C31P	Plastic DIP
MC26C31D	SOG Package

The MC26C31 is a quad differential line driver designed for digital data transmission over balanced lines. The MC26C31 meets all the requirements of standard EIA-422-A while retaining the low-power characteristics of CMOS.

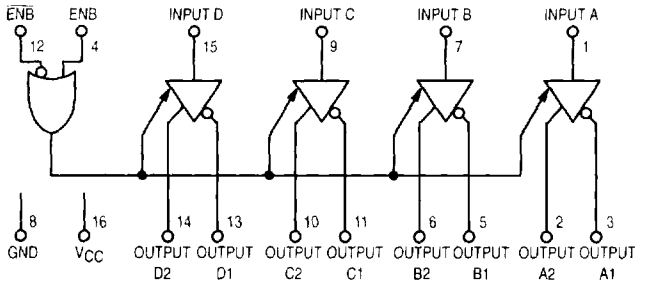
The MC26C31 accepts TTL or CMOS input levels and translates these to EIA-422-A output level. This part uses special output circuitry that enables the individual drivers to power down without loading down the bus. The MC26C31 also includes special circuitry which will set the outputs to a high impedance mode during power up or down, preventing spurious glitches. This device has enable and disable circuitry common for all four drivers.

The MC26C31 is pin compatible with the AM26LS31.

All pins are protected against damage due to electrostatic discharges.

- Maximum Supply Current: 3 mA
- 2000 V ESD Protection on the Inputs and Outputs
- TTL/CMOS Input Compatible
- Typical Propagation Delay: 6 ns
- Typical Output Skew: 1 ns
- Meets V_O = 6.0 V (and V_O = 0.25 V), V_{CC} = 0 V, I_O < 100 μA Requirement
- Meets the Requirements of Standard EIA-422-A
- Operation from Single 5 V Supply
- High Impedance Mode for Outputs Connected to System Buses

BLOCK DIAGRAM



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

REV 3
1993

TRUTH TABLE

Control Inputs E/$\overline{E}$	Input	Non-Inverting Output	Inverting Output
L/H	X	Z	Z
All other combinations of enable inputs	H	H	L
	L	L	H

X = Don't Care
Z = High Impedance
H = High Logic State
L = Low Logic State

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7	V
DC Input Voltage	V_{in}	− 1.5 to V_{CC} + 1.5	V
DC Output Voltage*	V_{out}	− 0.5 to V_{CC} + 0.5	V
DC Output Current, per Pin	I_{out}	150	mA
DC V_{CC} or GND Current, per Pin	I_{DD}	150	mA
Storage Temperature	T_{stg}	− 65 to + 150	°C
Power Dissipation	P_D	500	mW
ESD (Human Body Model)		2000	V

* Power−on conditions.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages to this high impedance circuit.

For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$. Reliability of operation is enhanced if unused inputs are tied to and appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

OPERATING CONDITIONS

Rating	Symbol	Min	Max	Unit
Power Supply Voltage	V_{CC}	4.5	5.5	V
DC Input Voltage	V_{in}	0	V_{CC}	V
Operating Temperature Range	T_A	− 40	+ 85	°C
Input Rise and Fall Time	t_r, t_f	—	500	ns

DC CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = − 40 to + 85 °C, unless otherwise stated)

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage (Low Logic State)	V_{IL}	—	—	0.8	V
Input Voltage (High Logic State)	V_{IH}	2.0	—	—	V
Output Voltage (Low Logic State) I_{sink} = 20 mA	V_{OL}	—	0.3	0.5	V
Output Voltage (High Logic State) I_{source} = 20 mA	V_{OH}	2.5	2.8	—	V
Output Differential Voltage R_L = 100 Ω (Note 1)	V_{OD}	2.0	—	—	V
Output Differential Voltage Difference R_L = 100 Ω (Note 1)	$D(V_{OD})$	—	—	± 0.4	V
Output Offset Voltage R_L = 100 Ω (Note 1)	V_{OS}	—	—	3.0	V
Output Offset Voltage Difference R_L = 100 Ω (Note 1)	$D(V_{OS})$	—	—	± 0.4	V
Input Current V_{IH} = V_{CC}, GND, V_{IH} or V_{IL}	I_{in}	—	—	± 1.0	μA
Quiescent Supply Current I_{out} = 0 μA	I_{CC}	—	—	3.0	mA
Output Short Circuit Current (Note 2)	I_{OS}	− 30	− 100	− 150	mA
Output Leakage Current (High−Z State) V_{out} = V_{CC} or GND	$I_{O(Z)}$	—	—	± 1.0	μA
Input Leakage Current (Power Off) V_{out} = 6 V	I_{oxh}	—	—	100	μA
V_{out} = − 0.25 V	I_{oxl}	—	—	− 100	

NOTES:
1. See EIA specifications EIA−422 A for exact test conditions.
2. Only one output may be shorted at a time.

AC CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = – 40 to + 85°C, unless otherwise stated)

Parameter	Symbol	Min	Typ	Max	Unit
Propagation Delay Input to Output (S1 Open)	t_{PLH} t_{PHL}	—	6	12	ns
Output Skew (S1 Open)*	Skew	—	1.0	4	ns
Differential Output Rise Time Fall Time (S1 Open)	$t_{(TLH)}$ $t_{(THL)}$	—	4	8	ns
Output Enable Time (S1 Closed)	t_{PZH} t_{PZL}	— —	16 15	— —	ns
Output Disable Time (S1 Closed)	t_{PHZ} t_{PLZ}	— —	6 9	— —	ns

* Skew: difference in propagation delays between complementary outputs.

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AC TEST CIRCUIT AND SWITCHING TIME WAVEFORMS

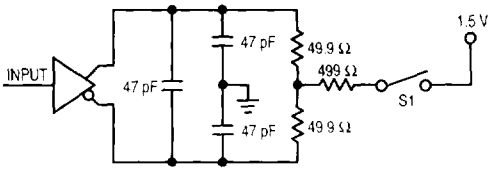

Figure 1. AC Test Circuit

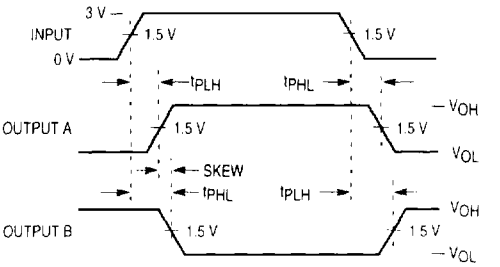

Figure 2. Propagation Delays and Skew Waveforms

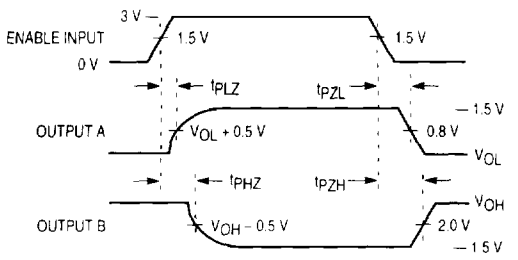

Figure 3. Enable and Disable Times

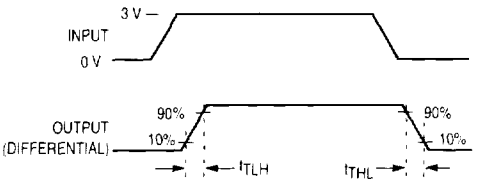

Figure 4. Differential Rise and Fall Times

TYPICAL APPLICATIONS

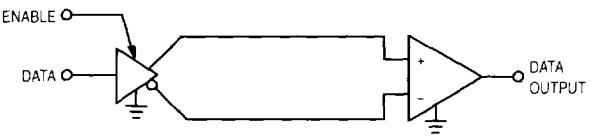

Figure 5. Two–Wire Balanced Systems (EIA–422–A)